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MICROCOMPUTER MN103S

MN103SA7D/A7G

LSI User's Manual

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Panasonic

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About This Manual

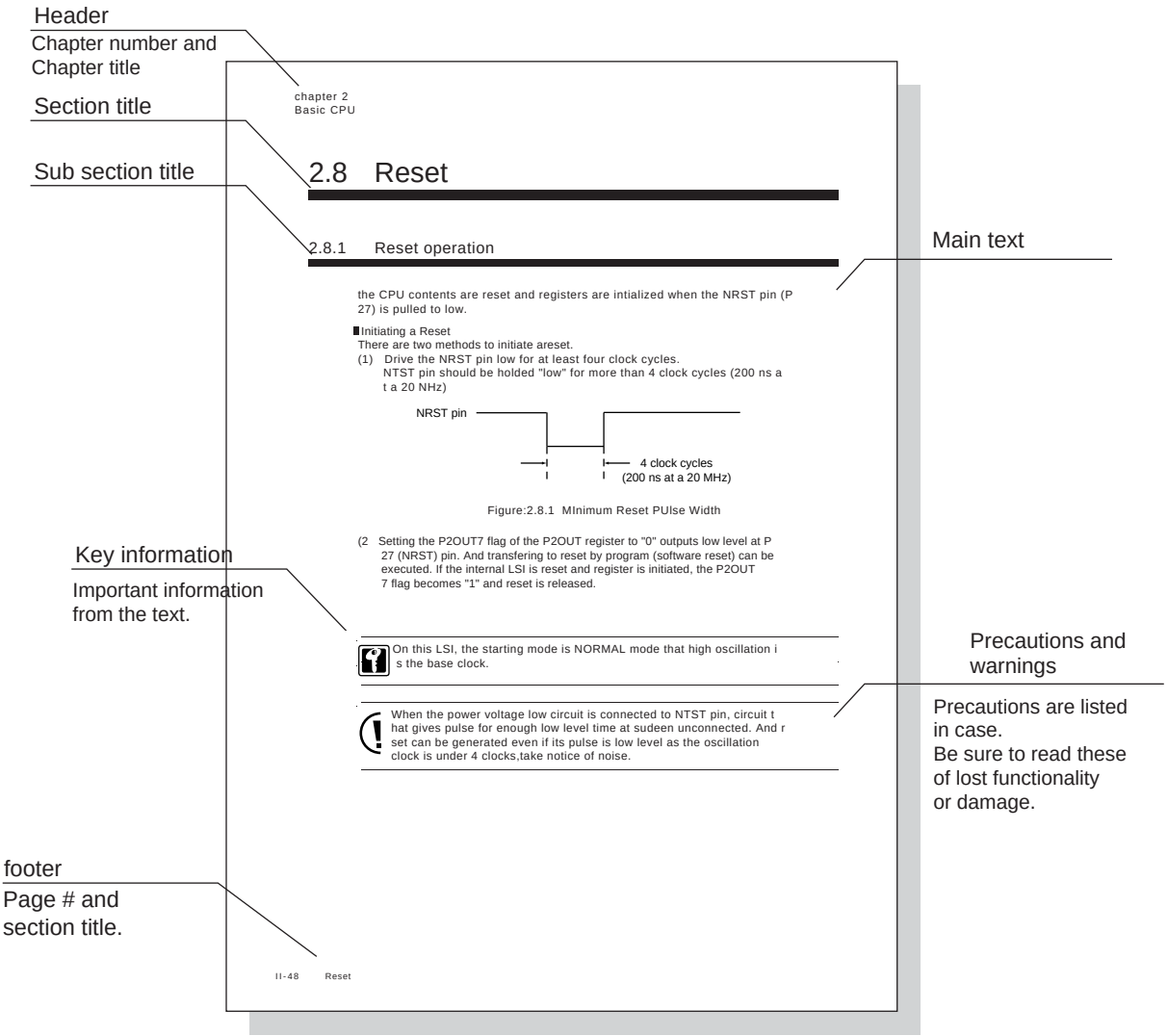
■Organization

This LSI manual describes the features of the MN103SA7 Series, which begins with an overview, followed by information in the order of CPU basic, interrupt, port, timer, serial, and other peripheral hardware functions.

Each section consists of brief functional information, block diagrams, and the details of control registers including operation methods and setting examples.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.The layout and definition of each section are shown below.



Note: The example on this page is for explanation. It differs from an actual page.

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

1.Consult the index at the front of the manual to locate the beginning of each section.

2.Consult the table of contents at the front of the manual to locate desired titles.

3.A chapter number and its chapter title are located at the top corner of each page, and section titles are located at the bottom corner of each page.

■Related Manuals

Note that the following related documents are available.

- "MN103S Series Instruction Manual"
  <Describes the instruction set.>
- "MN103S Series Cross-assembler User's Manual"
  <Describes the assembler syntax and notation.>
- " Series C Compiler User's Manual: Usage Guide"
  <Describes the installation, the commands, and options of the C Compiler.>
- "MN103S Series C Compiler User's Manual: Language Description"
  <Describes the syntax of the C Compiler.>
- "MN103S Series C Compiler User's Manual: Library Reference"
  <Describes the standard library of the C Compiler.>
- "MN103S Series C Source Code Debugger User's Manual"
  <Describes the use of C source code debugger.>
- "MN103S Series Installation Manual"
  <Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

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Chapter 1 Overview

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1.1 Overview

1.1.1 Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on chip for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

1.1.2 Product Summary

This manual describes the following model of MN103SA7. These model have same functions and MN103SA7D/A7G is primarily described in this manual.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification
MN10SA7D	64K	4K	Mask ROM version
MN10SA7G	128K	4K	Mask ROM version
MN10SFA7K	256K	8K	Flash EEPROM version

1.2 Hardware Functions

CPU Core	MN103S core 4 GB of linear address space (for instructions / data) LOAD/STORE architecture with 5-stage pipeline 46 basic instructions + 30 extension instructions 6 addressing modes Instruction set of 1 byte in word length Extension arithmetic unit incorporated (high-speed multiply, multiply and accumulate and saturation operation instructions) Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiply) Operation mode: Normal mode
Oscillation Circuit	Self-excited/externally excited oscillation
ROM Collection	Maximum 4 parts in a program
Internal Memory	MN103SA7D ROM 64Kbytes RAM 4Kbytes MN103SA7G ROM 128Kbytes RAM 4Kbytes MN103SFA7K ROM 256Kbytes RAM 8Kbytes
Interrupts	Internal interrupts: 47 interrupts Watchdog timer overflow interrupts System error interrupts <Timer Interrupts> Timer 0 underflow interrupts Timer 1 underflow interrupts Timer 2 underflow interrupts Timer 3 underflow interrupts Timer 4 underflow interrupts Timer 5 underflow interrupts Timer 6 underflow interrupts Timer 7 underflow interrupts Timer 8 overflow/underflow interrupts Timer 8 compare/capture A interrupts Timer 8 compare/capture B interrupts Timer 9 overflow/underflow interrupts Timer 9 compare/capture A interrupts Timer 9 compare/capture B interrupts Timer 10 overflow/underflow interrupts Timer 10 compare/capture A interrupts Timer 10 compare/capture B interrupts Timer 11 overflow/underflow interrupts Timer 11 compare/capture A interrupts Timer 11 compare/capture B interrupts Timer 12 overflow/underflow interrupts Timer 12 compare A interrupts Timer 12 compare B interrupts Timer 13 overflow/underflow interrupts Timer 13 compare A interrupts Timer 13 compare B interrupts Timer 14 underflow interrupts Timer 15 underflow interrupts

Timer 16 underflow interrupts
Timer 17 underflow interrupts

<Serial Interface>
Serial 0 reception interrupts
Serial 0 transmission interrupts
Serial 1 reception interrupts
Serial 1 transmission interrupts
Serial 2 reception interrupts
Serial 2 transmission interrupts

<PWM>
PWM0 overflow interrupts of PWM cycle
PWM0 underflow interrupts
PWM1 overflow interrupts of PWM cycle
PWM1 underflow interrupts

<A/D interrupt>
A/D 0 conversion complete interrupt
A/D 0 conversion complete B interrupt
A/D 1 conversion complete interrupt
A/D 1 conversion complete B interrupt
A/D 2 conversion complete interrupt

External interrupts: 9 interrupts
IRQ0: Edge, both edges, level interrupts, noise filter connectable
IRQ1: Edge, both edges, level interrupts, noise filter connectable
IRQ2: Edge, both edges, level interrupts, noise filter connectable
IRQ3: Edge, both edges, level interrupts, noise filter connectable
IRQ4: Edge, both edges, level interrupts, noise filter connectable
IRQ5: Edge, both edges, level interrupts, noise filter connectable
IRQ6: Edge, both edges, level interrupts, noise filter connectable
IRQ7: Edge, both edges, level interrupts, noise filter connectable
IRQ8: Edge, both edges, level interrupts, noise filter connectable

Timer Counter

8-bit timer for general use 12 sets
16-bit timer for general use 6 sets

Timer 0 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 1 underflow, Timer 2 underflow

Timer 1 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function (connected to Timer 0)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 0 underflow, Timer 2 underflow

Timer 2 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count, Cascade connection function (connected to Timer 1)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow, TM2IO pin input

Timer 3 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
  Cascade connection function (connected to Timer 2)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 0 underflow,
  Timer 1 underflow, Timer 2 underflow, TM3IO pin input

Timer 4 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 5 underflow,
  Timer 6 underflow, TM4IO pin input

Timer 5 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
  Cascade connection function (connected to Timer 4)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 4 underflow,
  Timer 6 underflow, TM5IO pin input

Timer 6 (8-bit timer for general use)
- Interval timer
  Cascade connection function (connected to Timer 5)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 4 underflow,
  Timer 5 underflow

Timer 7 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
  Cascade connection function (connected to Timer 6)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 4 underflow,
  Timer 5 underflow, Timer 6 underflow, TM7IO pin input

Timer 8 (16-bit timer for general use)
- Interval timer, Event count, up/down count,
  timer output, PWM output, input capture, one-shot output,
  external trigger start
- Count clock source
  IOCLK, IOCLK/8, IOCLK/64, Timer 2 underflow,
  TM8BIO pin input

Timer 9 (16-bit timer for general use)
- Interval timer, Event count, up/down count,
  timer output, PWM output, input capture, one-shot output,
  external trigger start
- Count clock source
  IOCLK, IOCLK/8, IOCLK/64, Timer 3 underflow,
  TM9BIO pin input

Timer 10 (16-bit timer for general use)
- Interval timer, Event count, up/down count,
  timer output, PWM output, input capture, one-shot output,
  external trigger start

- Count clock source
  IOCLK, IOCLK/8, Timer 0 underflow, Timer 1 underflow,
  TM10BIO pin input

Timer 11 (16-bit timer for general use)
- Interval timer, Event count, up/down count,
  timer output, PWM output (output to 6 ports all at once is possible),
  input capture, one-shot output, external trigger start
- Count clock source
  IOCLK, IOCLK/8, Timer 4 underflow, Timer 5 underflow,
  TM11IO1 pin input

Timer 12 (16-bit timer for general use)
- Interval timer, up/down count, trigger start 3-phase PWM,
  AD conversion start
- Count clock source
  MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 6 underflow,
  Timer 7 underflow

Timer 13 (16-bit timer for general use)
- Interval timer, up/down count, trigger start 3-phase PWM,
  AD conversion start
- Count clock source
  MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 6 underflow,
  Timer 7 underflow

Timer 14 (8-bit timer for general use)
- Interval timer, Baud rate timer
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 15 underflow,
  Timer 16 underflow

Timer 15 (8-bit timer for general use)
- Interval timer, Baud rate timer,
  Cascade connection function (connected to Timer 14)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 14 underflow,
  Timer 16 underflow

Timer 16 (8-bit timer for general use)
- Interval timer, Baud rate timer,
  Cascade connection function (connected to Timer 15)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 14 underflow,
  Timer 15 underflow

Timer 17 (8-bit timer for general use)
- Interval timer, Timer pulse output, Event count,
  Cascade connection function (connected to Timer 16)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, Timer 14 underflow,
  Timer 15 underflow, Timer 16 underflow, TM17IO pin input

Watchdog Timer	Detection time	6.55 ms to 1677.72 ms (oscillation frequency 10 MHz)
	Generates non-maskable interrupts at detection	

A /D Converter
- Minimum conversion time 1.0 msec
- 16 channels × 3 converters
- Use of 3 converters allows simultaneous sampling of 3 phases
- A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

Complementary 3-phase PWM output 2 channels
- Min. resolution: 33.3 nsec
- Triangular and saw-tooth waves output
- Incorporates a dead time insertion circuit
- Can overwrite registers by double buffer during PWM operation
- PWM output protection circuit supporting external interrupts
  (PWM brought to a high impedance state by hardware means.)

Serial Interface 3 channels

Serial 0 (Full duplex UART/synchronous serial interface)

Synchronous serial interface
- Parity error, overrun error detection
- Transfer clock source
  1/2 and 1/16 of timer 14 underflow, 1/2 and 1/16 of timer 15 underflow, and 1/2 and 1/16 of timer 16 underflow, SBT0 pin
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Maximum transfer rate: 3.0 Mbps

Full duplex UART
- Parity error, overrun error, and flaming error detection
- Transfer size 7 to 8 bits can be selected.
- Transfer clock source
  1/16 of timer 14 underflow, 1/16 of timer 15 underflow, and 1/16 of timer 16 underflow,
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Maximum transfer rate: 375 Kbps

Serial 1 (Full duplex UART/synchronous serial interface)

Synchronous serial interface
- Parity error, Overrun error detection
- Transfer clock source
  1/2 and 1/16 of timer 14 underflow, 1/2 and 1/16 of timer 15 underflow, and 1/2 and 1/16 of timer 16 underflow, SBT1 pin
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Maximum transfer rate: 3.0 Mbps

Full duplex UART
- Parity error, overrun error, and flaming error detection
- Transfer clock source
  1/16 of timer 14 underflow, 1/16 of timer 15 underflow, and 1/16 of timer 16 underflow,
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Maximum transfer rate: 375 Kbps

Serial 2 (Full duplex UART/synchronous serial interface)

Synchronous serial interface
- Overrun error detection

- Transfer clock source
  1/2, 1/4, 1/16, and 1/64 of timer 14 underflow,
  1/2, 1/4, 1/16, and 1/64 of timer 15 underflow,
  1/2, 1/4, 1/16, and 1/64 of timer 16 underflow,
  IOCLK/2, IOCLK/4, SBT2 pin
- Can be selected as the first bit to be transferred,
  Any transfer size from 1 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 5.0 Mbps

Full duplex UART

- Parity error, overrun error and flaming error detection
- Transfer clock source
  1/32, 1/64, 1/256, and 1/1024 of timer 14 underflow,
  1/32, 1/64, 1/256, and 1/1024 of timer 15 underflow,
  1/32, 1/64, 1/256, and 1/1024 of timer 16 underflow,
  IOCLK/32, IOCLK/64
- Can be selected as the first bit to be transferred,
  Any transfer size from 7 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 300 Kbps

Regulator: incorporates regulator, and use of 5 V power supply is possible

Power Supply Detection

Detection level 3.6 V to 4.5 V

When power supply voltage is under detection level, reset is generated.

Port / pins	I/O ports	61 pins
	Motor control output	12 pins
	External interrupt	9 pins
	A/D input	16 pins
	Special pins	17 pins
	Reset input pin	1 pin
	Oscillation pin	2 pins
	Test pin	3 pins
	Power pin	11 pins

Package: LQFP80 (14 mm square, 0.65 mm pitch)

Code name: LQFP080-P-1414A

1.3 Pin Description

1.3.1 Pin Configuration

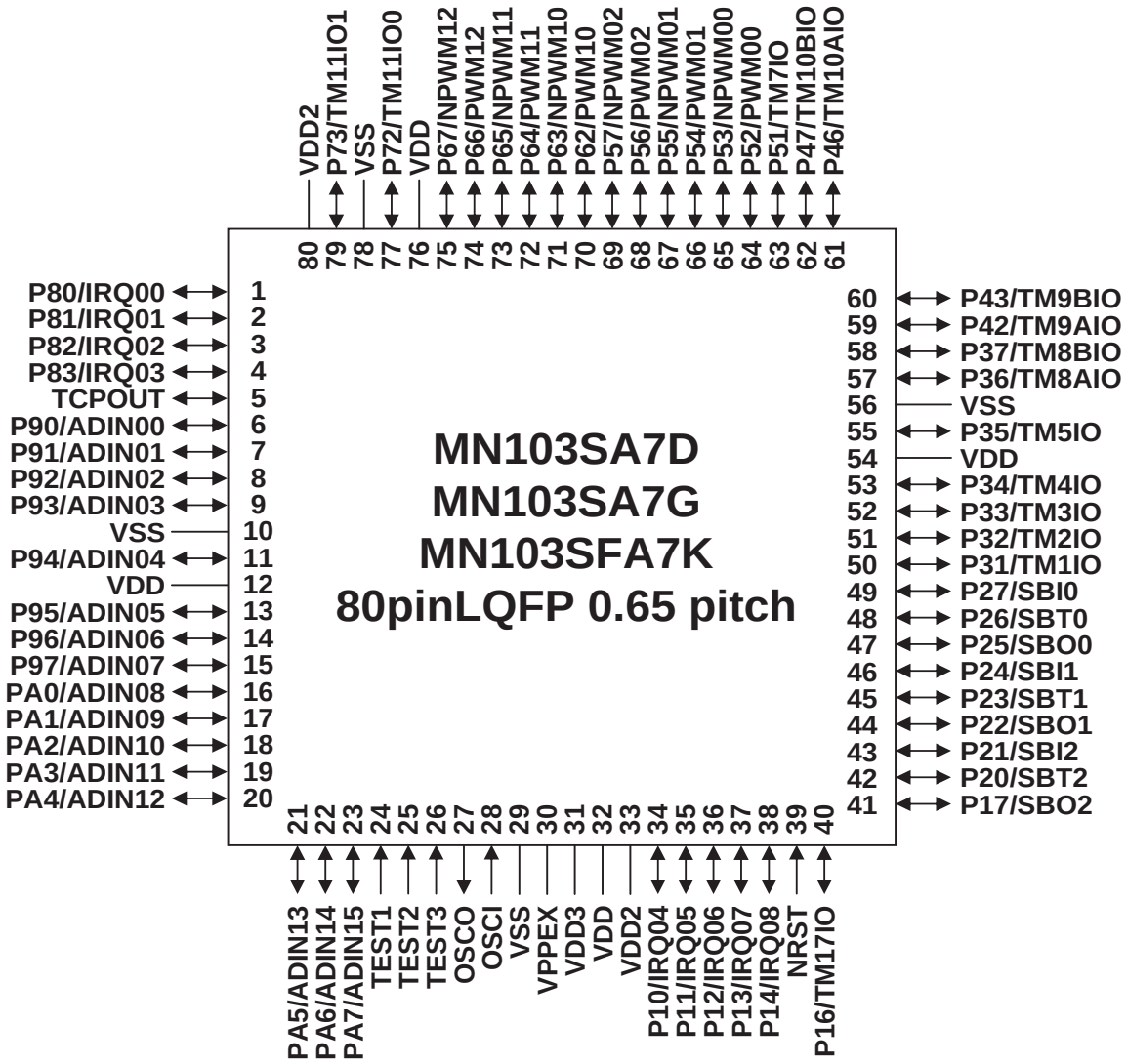


Figure:1.3.1 Pin Configuration

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

Pin	Special functions	I/O	Direction control	Pin control	Function description
NRST	-	in	-	-	Reset input
P10	IRQ04	in/out	P10D	P10R	External interrupt input 4
P11	IRQ05	in/out	P11D	P11R	External interrupt input 5
P12	IRQ06	in/out	P12D	P12R	External interrupt input 6
P13	IRQ07	in/out	P13D	P13R	External interrupt input 7
P14	IRQ08	in/out	P14D	P14R	External interrupt input 8
P16	TM17IO	in/out	P16D	P16R	Timer 17 input / output
P17	SBO2	in/out	P17D	P17R	Serial 2 transmission data output
P20	SBT2	in/out	P20D	P20R	Serial 2 clock I/O
P21	SBI2	in/out	P21D	P21R	Serial 2 reception data input
P22	SBO1	in/out	P22D	P22R	Serial 1 transmission data output
P23	SBT1	in/out	P23D	P23R	Serial 1 clock I/O
P24	SBI1	in/out	P24D	P24R	Serial 1 reception data input
P25	SBO0	in/out	P25D	P25R	Serial 0 transmission data output
P26	SBT0	in/out	P26D	P26R	Serial 0 clock I/O
P27	SBI0	in/out	P27D	P27R	Serial 0 reception data input
P31	TM1IO	in/out	P31D	P31R	Timer 1 I/O
P32	TM2IO	in/out	P32D	P32R	Timer 2 I/O
P33	TM3IO	in/out	P33D	P33R	Timer 3 I/O
P34	TM4IO	in/out	P34D	P34R	Timer 4 I/O
P35	TM5IO	in/out	P35D	P35R	Timer 5 I/O
P36	TM8AIO	in/out	P36D	P36R	Timer 8A I/O
P37	TM8BIO	in/out	P37D	P37R	Timer 8B I/O
P42	TM9AIO	in/out	P42D	P42R	Timer 9A I/O
P43	TM9BIO	in/out	P43D	P43R	Timer 9B I/O
P46	TM10AIO	in/out	P46D	P46R	Timer 10A I/O
P47	TM10BIO	in/out	P47D	P47R	Timer 10B I/O
P51	TM7IO	in/out	P51D	P51R	Timer 7 I/O
P52	PWM00	in/out	P52D	P52R	3-phase PWM0 signal output 0
P53	NPWM00	in/out	P53D	P53R	3-phase PWM0 signal reverse output 0
P54	PWM01	in/out	P54D	P54R	3-phase PWM0 signal output 1
P55	NPWM01	in/out	P55D	P55R	3-phase PWM0 signal reverse output 1
P56	PWM02	in/out	P56D	P56R	3-phase PWM0 signal output 2
P57	NPWM02	in/out	P57D	P57R	3-phase PWM0 signal reverse output 2
P62	PWM10	in/out	P62D	P62R	3-phase PWM1 signal output 0
P63	NPWM10	in/out	P63D	P63R	3-phase PWM1 signal reverse output 0
P64	PWM11	in/out	P64D	P64R	3-phase PWM1 signal output 1
P65	NPWM11	in/out	P65D	P65R	3-phase PWM1 signal reverse output 1
P66	PWM12	in/out	P66D	P66R	3-phase PWM1 signal output 2
P67	NPWM12	in/out	P67D	P67R	3-phase PWM1 signal reverse output 2
P72	TM11IO0	in/out	P72D	P72R	Timer 11 I/O 0
P73	TM11IO1	in/out	P73D	P73R	Timer 11 I/O 1
P80	IRQ00	in/out	P80D	P80R	External interrupt input 0
P81	IRQ01	in/out	P81D	P81R	External interrupt input 1
P82	IRQ02	in/out	P82D	P82R	External interrupt input 2
P83	IRQ03	in/out	P83D	P83R	External interrupt input 3
P90	ADIN00	in/out	P90D	P90R	AD analog signal input 0
P91	ADIN01	in/out	P91D	P91R	AD analog signal input 1
P92	ADIN02	in/out	P92D	P92R	AD analog signal input 2
P93	ADIN03	in/out	P93D	P93R	AD analog signal input 3
P94	ADIN04	in/out	P94D	P94R	AD analog signal input 4
P95	ADIN05	in/out	P95D	P95R	AD analog signal input 5
P96	ADIN06	in/out	P96D	P96R	AD analog signal input 6
P97	ADIN07	in/out	P97D	P97R	AD analog signal input 7

Pin	Special functions	I/O	Direction control	Pin control	Function description
PA0	ADIN08	in/out	PA0D	PA0R	AD analog signal input 8
PA1	ADIN09	in/out	PA1D	PA1R	AD analog signal input 9
PA2	ADIN10	in/out	PA2D	PA2R	AD analog signal input 10
PA3	ADIN11	in/out	PA3D	PA3R	AD analog signal input 11
PA4	ADIN12	in/out	PA4D	PA4R	AD analog signal input 12
PA5	ADIN13	in/out	PA5D	PA5R	AD analog signal input 13
PA6	ADIN14	in/out	PA6D	PA6R	AD analog signal input 14
PA7	ADIN15	in/out	PA7D	PA7R	AD analog signal input 15

1.3.3 Pin Functions

Table:1.3.2 Pin Functions

Name	TQFP 48 Pin No.	I/O	Other Function	Function	Description
VDD VDD VDD VDD	12 32 54 76	-	-	Power supply pin	Power pins for 5 V, digital IO Apply 5 V to all of pins and connect capacitor of over 10 μF between all of the VDD and VSS pins. It is recommended that total capacitance between all of the VDD and VSS is more than 10-times sum of capacitance between all of the VDD2 and VSS plus capacitance etween VDD3 and VSS.
VDD2 VDD2	33 80	-	-	Power supply pin	Power pins for 1.8 V, digital IO Connect capacitor of over 1 mF between all of the VDD2 and VSS pins. .
VSS VSS VSS VSS	10 29 56 78	-	-	Power supply pin	GND for digital
VDD3	31	-	-	Power supply pin	Power pin for 3.3 V, flash Connect capacitor of over 2 μF between VDD3 and VSS pins. N, C for mask ROM version
VPPEX	30	-		Power supply pin	Power for flash EEPROM Connect with VDD3. N, C for mask ROM version
OSC1 OSC0	28 27	input output	-	Clock input pin Clock output pin	Extend ceramic or crystal oscillators or input a clock to OSC1.
NRST	39	input	-	Reset pins (negative logic)	This pin resets the chip when power is turned on and contains an internal pull-up resistor. Setting this pin “L” level initializes the internal state of the device. Thereafter, setting the input to “H” level releases the reset. The hardware waits for the system clock to stabilize, and processes the reset interrupt. Connect capacitor of over 0.1 μF between NRST and VSS pins.
P10 P11 P12 P13 P14 P16 P17	34 35 36 37 38 40 41	I/O	IRQ04 IRQ05 IRQ06 IRQ07 IRQ08 TM7IO SBO2	I/O port 1	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P1DIR register. Pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode (P10 to P14, P16, P17) is selected, and pull-up resistor is disabled.
P20 P21 P22 P23 P24 P25 P26 P27	42 43 44 45 46 47 48 49	I/O	SBT2 SBI2 SBO1 SBT1 SBI1 SBO0 SBT0 SBI0	I/O port 2	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P2DIR register. Pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode (P20 to P27) is selected, and pull-up resistor is disabled.

Name	TQFP 48 Pin No.	I/O	Other Function	Function	Description
P31 P32 P33 P34 P35 P36 P37	50 51 52 53 55 57 58	I/O	TM1IO TM2IO TM3IO TM4IO TM5IO TM8AIO TM8BIO	I/O port 3	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P3DIR register. Pull-up resistor for ech bit can be selected individually by the P3PLU register. At reset, the input mode (P31 to P37) is selected, and pull-up resistor is disabled.
P42 P43 P46 P47	59 60 61 62	I/O	TM9AIO TM9BIO TM10AIO TM10BIO	I/O port 4	8-bit CMOS I/O port. Each bit can be set individually as either input or output by the P4DIR register. Pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode (P42, P43, P46, P47) is selected and pull-up resistor is disabled.
P51 P52 P53 P54 P55 P56 P57	63 64 65 66 67 68 69	I/O	TM7IO PWM00 NPWM00 PWM01 NPWM01 PWM02 NPWM02	I/O port 5	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P5DIR register. Pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode (P51 to P57) is selected, and pull-up resistor is disabled.
P62 P63 P64 P65 P66 P67	70 71 72 73 74 75	I/O	PWM10 NPWM10 PWM11 NPWM11 PWM12 NPWM12	I/O port 6	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P6DIR register. Pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode (P62 to P67) is selected, and pull-up resistor is disabled.
P72 P73	77 79	I/O	TM11IO0 TM11IO1	I/O port 7	8-bit CMOS I/O ports. Each bit can be set individually as either input or output by the P7DIR register. P pull-up resistor for each bit can be selected individually by the P7PLU register. At reset, the input mode (P72, P73) is selected, and pull-up resistor is disabled.
P80 P81 P82 P83	1 2 3 4	I/O	IRQ00 IRQ01 IRQ02 IRQ03	I/O port 8	8-bit CMOS input ports. Each bit can be set individually as either input or output by the P8PLU register. Pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode (P80 to P83) is selected, and pull-up resistor is disabled.
P90 P91 P92 P93 P94 P95 P96 P97	6 7 8 9 11 13 14 15	I/O	ADIN00 ADIN01 ADIN02 ADIN03 ADIN04 ADIN05 ADIN06 ADIN07	I/O port 9	8-bit CMOS input ports. Each bit can be set individually as either input or output by the P9DIR register. Pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode (P90 to P97) is selected, and pull-up resistor is disabled.
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	16 17 18 19 20 21 22 23	I/O	ADIN08 ADIN09 ADIN10 ADIN11 ADIN12 ADIN13 ADIN14 ADIN15	I/O port A	8-bit CMOS input ports. Each bit can be set individually as either input or output by the PADIR register. Pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode (PA0 to PA7) is selected, and pull-up resistor is disabled.

Name	TQFP 48 Pin No.	I/O	Other Function	Function	Description
SB00 SB01 SB02	47 44 41	Output	P25 P22 P17	Serial interface transmission data output pin	Transmission data output pins for serial interface 0, 1, and 2. Select output by the P1DIR and P2DIR registers and serial pin function by the P1MD and P2MD registers. These can be used as normal I/O pins when serial interfaces are not used.
SBI0 SBI1 SBI2	49 46 43	Input	P27 P24 P21	Serial interface reception data input pin	Reception data input pins for serial interface 0, 1, and 2. Pull-up resistor can be selected by the P2PLU register. Select input by the P2DIR register. These can be used as normal I/O pins when serial interfaces are not used.
SBT0 SBT1 SBT2	48 45 42	I/O	P26 P23 P20	Serial interface clock I/O pin	Clock I/O pins for serial interface 0, 1, and 2. Pull-up resistor can be selected by the P2PLU register. Select either input or output by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when serial interfaces are not used.
TM1IO TM2IO TM3IO TM4IO TM5IO TM7IO TM17I	50 51 52 53 55 63 40	I/O	P31 P32 P33 P34 P35 P51 P16	Timer I/O pin	Event counter input and timer pulse output pins for 8-bit timer 1 to 5, 7 and 17. At event count input, input mode dan be selected by the P1, 3 and 5DIR registers. At input mode, pull-up resistor can be selected by the P1, 3 and 5PLU registers. At timer pulse output, selected timer output pins by the P1,3 and 5MD registers and set output mode by the P1,3 and 5DIR registers. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM8AIO TM8BIO TM9AIO TM9BIO TM10AIO TM10BIO TM11IO0 TM11IO1	57 58 59 60 61 62 77 79	I/O	P36 P37 P42 P43 P46 P47 P72 P73	Timer I/O pin	Event counter input, timer output, and PWM output pins for 16-bit timer 8 to 11. At event counte input, input mode can be selected by the P3, 4, and 7DIR registers. At input mode, pull-up resistor can be selected by the P3, 4, and 7PLU register. At timer output and PWM output, select timer output pins by the P3, 4, and 7MD registers, and set output mode by the P3, 4, and 7DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM11IO0 TM11IO1	77 79	Output	P72 P73	PWM output pin	Motor control PWM signal output pins for 16-bit timer 11. These output PWM signals for 16-bit timer 11 to 2 pins simultaneously. At PWM output, select timer output pin by the P7MD register and set to output mode by the P7DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.

Name	TQFP 48 Pin No.	I/O	Other Function	Function	Description
ADIN00 ADIN01 ADIN02 ADIN03 ADIN04 ADIN05 ADIN06 ADIN07 ADIN08 ADIN09 ADIN10 ADIN11 ADIN12 ADIN13 ADIN14 ADIN15	6 7 8 9 11 13 14 15 16 17 18 19 20 21 22 23	Input	P90 P91 P92 P93 P94 P95 P96 P97 PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	Analogue input pin	Analogue input pins for 16-channel, 10-bit 3 A/D converters. These can be used as normal I/O pins when these are not used as analog input.
IRQ00 IRQ01 IRQ02 IRQ03 IRQ04 IRQ05 IRQ06 IRQ07 IRQ08	1 2 3 4 34 35 36 37 38	Input	P80 P81 P82 P83 P10 P11 P12 P13 P14	External interrupt pin	External interrupt input pins. The valid edge can be selected. Set whether both edges are detected or not by the edge detection register (IRQEDGESEL). When it is set not to detect both edges, select rising edge, falling edge, H level, or L level by the external interrupt condition specification register (EXTMD0 and EXTMD1). When it is set to detect both edges, select rising edge by the external interrupt condition setting register.
PWM00 PWM01 PWM02 PWM10 PWM11 PWM12	64 66 68 70 72 74	Output	P52 P54 P56 P62 P64 P66	Motor control PWM signal output pin	Motor control 3-phase PWM signal output pins. Select PWM signal output pins by the P5MD and P6MD registers and set output mode by the P5DIR and P6DIR registers. These can be used as normal I/O pins when these are not used as PWM signal output pins.
NPWM00 NPWM01 NPWM02 NPWM11 NPWM12 NPWM13	65 67 69 71 73 75	Output	P53 P55 P57 P63 P65 P67	Motor control PWM signal reverse output pin	Motor control 3-phase PWM signal revers output pins. Select PWM signal output pins by the P5MD and P6MD registers and set output mode by the P5DIR and P6DIR registers. These can be used as normal I/O pins when these are not used as PWM signal output pins.
TCPOUT	5	Input	-	Test signal input	Test signal input pin. Fix at VSS.
TEST1 TEST2 TEST3	24 25 26	Input	-	Test signal input	Test signal input pins built-in pull-up resistor. Pull-up with resistor of OPEN or 1 kΩ.

VPPEX is power supply for flash EEPROM rewriting. Its potential should be the same as VDD3. In mask ROM version, VPPEX is N.C; however, it is recommended to connect to VDD3 for compatibility with flash EEPROM version.

1.4 Block Diagram

1.4.1 Block Diagram

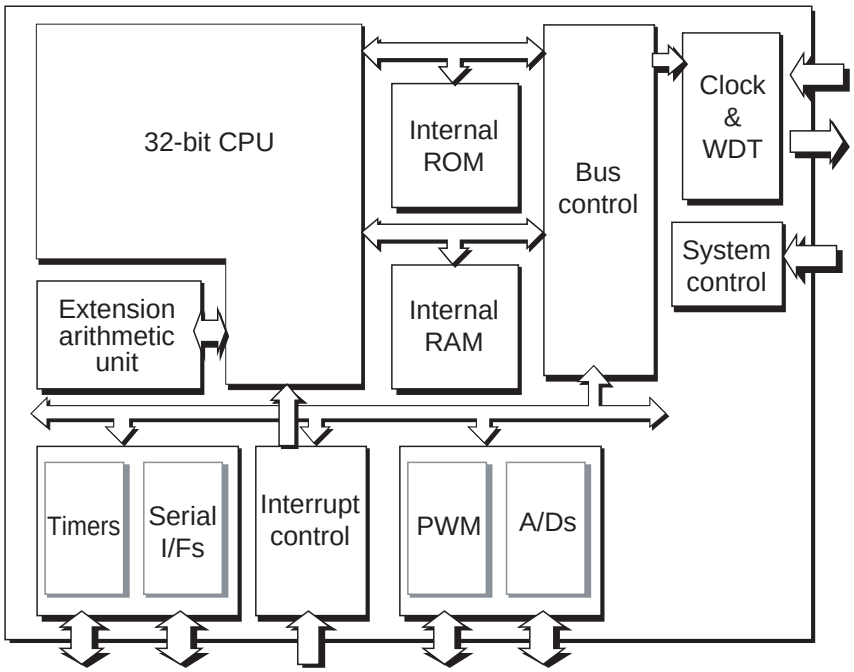


Figure:1.4.1 Block Diagram

1.5 Electrical Characteristics

This LSI manual describes the standard specification.

Electrical characteristics given in this section are preliminary and subject to change without notice. When using LSI, contact our sales office for product specifications.

Model	CMOS LSI
Application	General-purpose
Function	CMOS 32-bit 1 chip microcontroller

1.5.1 Absolute Maximum Ratings

V_{SS}=0.0 V

Parameter		Symbol	Rating	Unit
A1	External supply voltage	V_{DD}	-0.3 to +7.0	V
A2	Internal supply voltage	V_{DD2}	-0.3 to +2.5 V	V
A3	Flash EEPROM supply voltage	V_{DD3}	-0.3 to +4.6 V	V
A4	Input pin voltage	V_I	-0.3 to VDD +0.3 (upper limit: 7.0)	V
A5	I/O pin voltage	V_{IO}	-0.3 to VDD +0.3 (upper limit: 7.0)	V
A6	Peak output current	IOPEAK	±10	mA
A7	Typ. range output current	IOAVG	±5	mA
A8	Operating ambient temperature	TOPR	-40 to +85	°C
A9	Storage temperature	TSTG	-40 to +125	°C
A10	Power dissipation	PD	600	mW

Note: Each of the absolute maximum ratings refers to limits or values that will not damage the chip even if the chip is subject to that rating. The average output current rating is applicable to any given 100-ms period. The total of the average output current of all pins should be less than 50mA. Insert at least one 10 μF or higher bypass capacitor between each power supply pins (VDD pins) and ground. Additionally, insert at least one 1 μF or higher bypass capacitor between internal each power supply pins (V_{DD2} pins) and ground.
Additionally, insert at least one 2μF or higher bypass capacitor between Flash EEPROM power supply pins (V_{DD3} pins) and ground.
It is recommended that total capacitance between all of the VDD and VSS is more than 10-times sum of capacitance between all of the VDD2 and VSS plus capacitance etween VDD3 and VSS.

1.5.2 Operating Conditions

Ta= -40 °C to +85 °C
VSS = 0.0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
B1	External supply voltage 1	V_{DD11}	-	Vrst	5.0	5.5	V

Oscillation

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
B2	Input frequency	FOSC	-	5.0	-	15	MHz

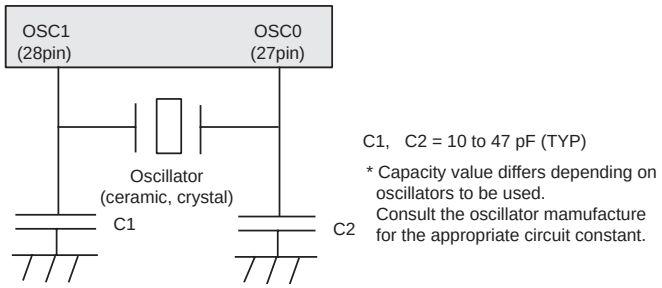


Figure:1.5.1 Oscillation

VDD = 5.0 V
VSS = 0.0 V
Ta= -40 °C to +85 °C

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
External clock input 1 OSCI (OSCO left open)							
B3	Clock frequency	fosc	-	5.0	-	15.0	MHz
B4	High-level pulse width	twh1	Fig. 1.5.2	25.0	-	-	ns
B5	Low-level pulse width	twl1		25.0	-	-	ns
B6	Rise time	twr1	Fig. 1.5.2	-	-	5.0	ns
B7	Fall time	twf1		-	-	5.0	ns

Note: Be sure that the clock duty ratio is 45 % to 55 %.

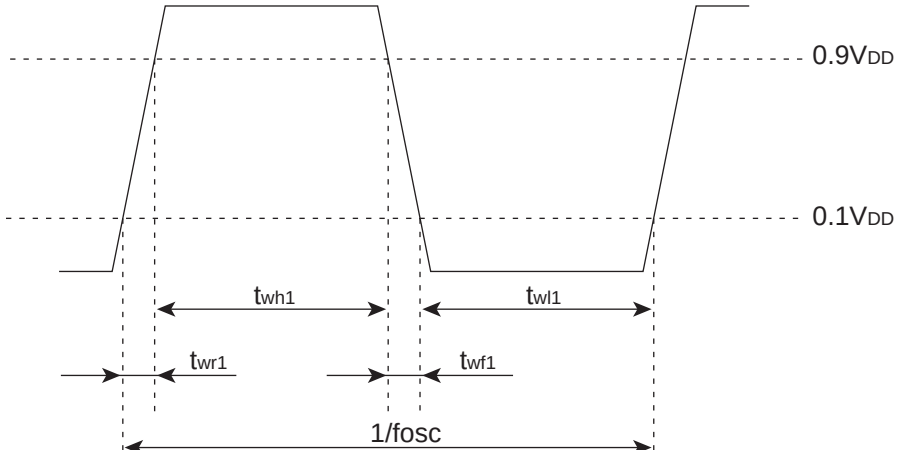


Figure:1.5.2 OSCI Timing Chart

1.5.3 DC Characteristics

V1 = V_{DD} or V_{SS}
Output open
V_{SS}, PV_{SS} = 0.0 V

DC Characteristics (Upper:M-ROM, Lower:Flash)

Parameter		Symbol	Conditions	Limits		Unit
				Typ.	Max.	
C1	Operating supply current (V_{DD} pin)j	IDDm	VDD = 5.0 V Internal regulator used. FOSC = 10 MHz (6 multiplication) Operating circuitry AD0, 1, 2: Continuously convert multiple channels PWM0, 1: Output triangular wave Timer 0 to 17: Free running Serial I/F 0 to 2: Send data through synchronous transmission. Other ports: Product H, L toggle output	60*1	90*1	mA
				80*2	120*2	

* 1 MN103SA7D/A7G

*2 MN103SFA7K

V_{DD} = 5.0 V
V_{SS} = 0.0 V
Ta = - 40 °C to +85 °C

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
I/O pin <output: push/pull / input: CMOS level> P10 to P14, P16, P17, P20 to P27, P31 to P37, P42, P43, P46, P47, P51 to P57, P62 to P67, P72, P73, P80 to P83, P90 to P97, PA0 to PA7							
C2	Input voltage High level	V_{IH1}	-	V_{DD} x 0.8	-	V_{DD}	V
C3	Input voltage Low level	V_{IL1}	-	0.0	-	V_{DD} x 0.2	V
C4	Input current Low level	I_{IH1}	V_{IN}=0 V Pull-up resistor is used	-55	-166	-500	µA
C5	Output voltage High level	V_{OH11}	I_O= -2 mA	V_{DD} - 0.3	-	-	V
		V_{OH12}	I_O= -4 mA	V_{DD} - 0.6	-	-	V
C6	Output voltage Low level	V_{OL11}	I_O= 2 mA	-	-	0.3	V
		V_{OL12}	I_O= 4 mA	-	-	0.4	V
C7	Output leak current	I_{OZ1}	V0=Hi-Z status	-10	-	10	µA

Value of Internal pull-up resistor
The standard value of internal pull-up resistor is 30 kΩ when V_{DD}= 5 V and V_{IN}= 0 V.
However, this value may change greatly depending on temperature. In the range from -40 °C to +85 °C,.the value may be 10 kΩ to 91 kΩ.

V_{DD} = 5.0 V
V_{SS} = 0.0 V
Ta= -40 °C to +85 °C

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
Input pins < input: CMOS level> NRST, TEST1 to TEST3							
C8	Input voltage High level	V_{IH2}	-	V_{DD} x 0.8	-	V_{DD}	V
C9	Input voltage Low level	V_{IL2}	-	0.0	-	V_{DD} x 0.2	V
C10	Input current Low level	I_{IH2}	V_{IN}=0 V Pull-up resistor is always connected	-55	-166	-500	µA

How to use test pins
The following pins are for LSI test. These pins are incorporated pull-up resistor.
TEST1 (P24) ... Pull-up to VDD with OPEN or about 1 kΩ resistor.
TEST2 (P25) ... Pull-up to VDD with OPEN or about 1 kΩ resistor.
TEST3 (P26) ... Pull-up to VDD with OPEN or about 1 kΩ resistor.

V_{DD}=5.0 V
V_{SS} = 0.0 V
Ta= -40 °C to +85 °C

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
OSCI pin							
C11	Input voltage High level	V_{IH4}	When external clock is input	V_{DD} x 0.9	-	V_{DD}	V
C12	Input current Low level	V_{IL4}	When external clock is input	0.0	-	V_{DD} x 0.1	V
C13	Internal feedback resistor	R_{FB}	V_1= V_{DD} or V_{SS}	-	1.0	-	MΩ
Regulator output pin V_{DD2}, V_{DD3}*1							
C14	Output voltage range	V_{DD2}	-	1.65	1.8	1.95	V
C15	Output voltage range	V_{DD3}	-	3.0	3.3	3.6	V

*1.Use the regulator output as power supply only for the microcontroller

1.5.4 A/D Converter Characteristics

V_{DD}=5.0 V
V_{SS} = 0.0 V
V_1 = V_{DD} or V_{SS}
Ta= 25 °C

A/D0, A/D1, A/D2

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	MAx.	
D1	Resolution	-	-	-	-	10	Bits
D2	Non-linearity error	-	Sampling time ≥ 200 ns A/D conversion clock ≥ 80 ns	-	-	±3	LSB
D3	Differential linearity error	-		-	-	±3	LSB
D4	Zero transition voltage	-		-25	-	25	mV
D5	Full-scale transition voltage	-		4975	-	5025	mV
D6	A/D conversion time	-	-	1.3	-	-	µs
D7	Analog input voltage	V_{1A}	-	VSS	-	VDD	V
D8	Analog input leakage current	I_{LA}	Unselected channel V_{LA} = 0 V to V_{DD}	-	-	±10	µA

1.5.5 AC Characteristics

Power-On sequence

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
E1	Reset signal pulse width (NRST)	tRSTW	-	1	-	-	ms
E2	Reset release timing (NRST)	tRSTS	-	1	-	-	ms

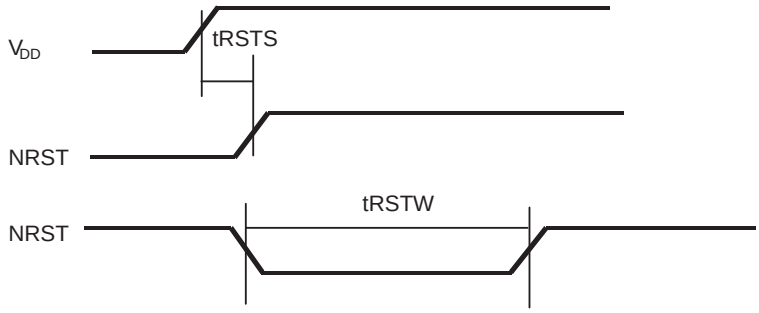


Figure:1.5.3 Power-On Sequence

* Insert capacitor of over 0.1 μF between NRST pin and ground.

V_{DD}=5.0 V
V_{SS} = 0.0 V
Ta= -40 °C to +85 °C
CL= 50 pF
Tmclk = 1/MCLK
Tsmp = n/IOCLK
n = 4,8 ,16,32

Interrupt signal input timing

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
E3	Interrupt signal pulse width(IRQn) In not using noise filter	tIRQW1	-	Tmclk x 3*1	-	-	ns
E4	Interrupt signal pulse width(IRQn) In using noise filter	tIRQW2	-	Tsmp x 3*2	-	-	ns

*1.When no noise filter is used, the minimum pulse width is determined by system clock(MCLK). Maintain the interrupt signal for a minimum of 3 cycles of MCLK.

*2.When noise filter is used, the minimum pulse width is determined by sampling clock. Maintain the interrupt signal for a minimum of 3 cycles of sampling clock. Refer to [5-4-7 Noise Filter Operation] for further details.

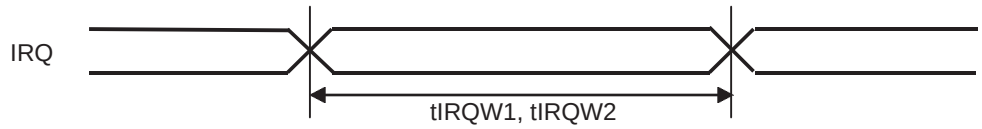


Figure:1.5.4 Interrupt signal timing

Power supply detection circuit characteristics

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
E4	Power supply detection level	V_{Rst}	-	3.6	-	4.5	V
E5	Rate of change for power supply voltage	ΔV_{DD}	-	0.2	-	-	ms/V

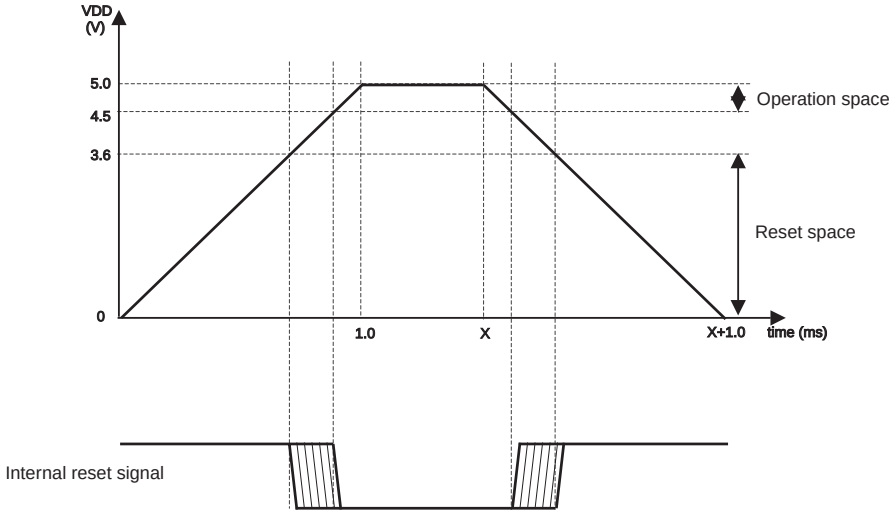


Figure:1.5.5 Power Supply Detection Level

1.6 Package Dimension

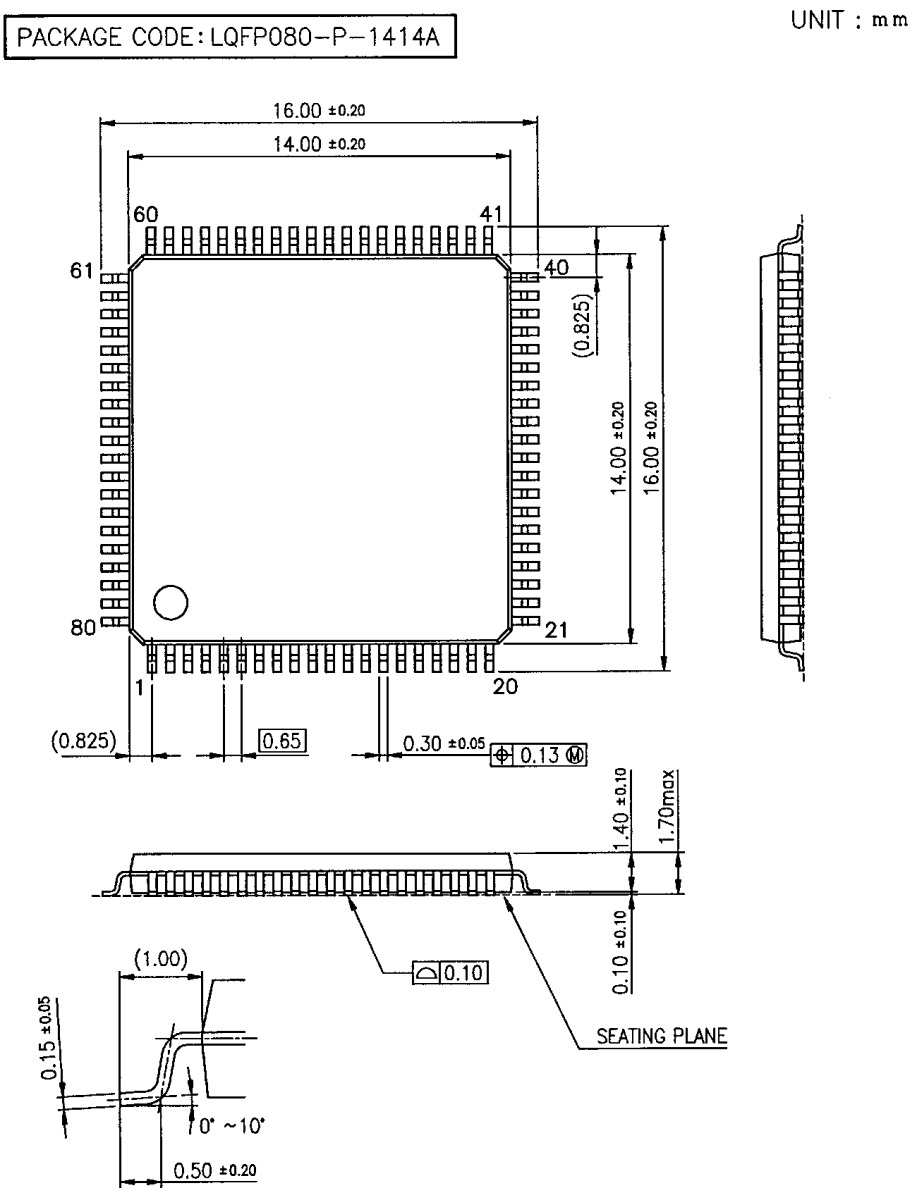


Figure:1.6.1 Package Dimension

Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Chapter 2 CPU Basics

2

2.1 Overview

Table: 2.1.1 shows basic specifications.

Table:2.1.1 Basic Specifications

Structure	Load/store architecture (9 registers)	Data: 32-bit x 4 Address: 32-bit x 4 Stack pointer: 32-bit x 1
	Load/store architecture (Others)	PC: 32-bit × 1 PSW : 16-bit × 1 Multiply/divide register: 32-bit x 1 Branch target register: 32-bit x 2
Instructions	Number of instructions	46
	Addressing modes	6
	Basic instruction length	1 byte
	Code assignment	1 byte to 2 bytes (basic part) + 0 byte to 6 bytes (extension)
Basic performance	Maximum Internal operating frequency	60.0 MHz (External oscillation 10MHz)
	Minimum instruction execution cycle	1 clock (16.7 nsec)
	Inter-register operations	1 clock
	Load/store	1 clock
	Conditional branch	1 clock to 3 clock
Pipeline	5-stage (instruction fetch, decode, execution, memory access, write-back)	
Address space	4 GB	

2.2 Block Diagram

Table: 2.2.1 shows the block diagram focusing on the CPU.

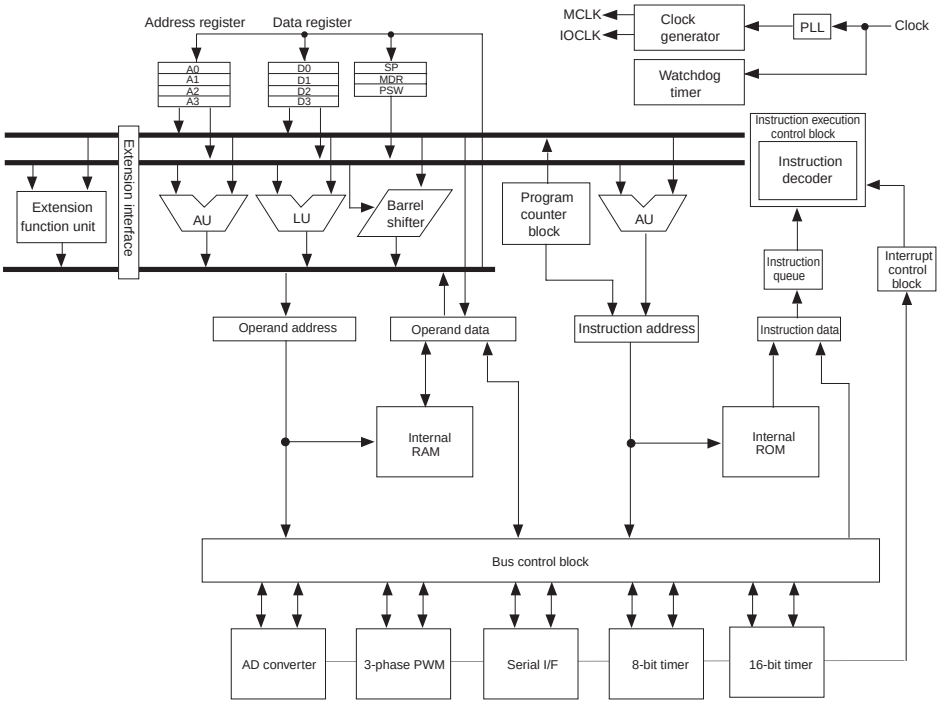


Figure:2.2.1 CPU Block Diagram

Table:2.2.1 Block Diagram and Function

Blocks	Description
Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores the instructions up to execution.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
Extension function	Executes extended instructions such as high-speed multiplication and multiply and accumulate operation instructions.
AU	Executes arithmetic operations.
LU	Executes logic operations.
Barrel shifter	Executes shift operations.
IInternal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Be used as address pointers and supports the operation instructions (addition, subtraction, and comparison) involved in address calculations.
Data register	Can use generally for all operations.
Interrupt control	Detects interrupt requests from peripheral functions, requests CPU shift to interrupt processing.
Bus control	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (A/D converter, 3-phase PWM, serial I/F, 8-bit timer, 16-bit timer). Peripheral functions vary depending on the model.

2.3 Programming Model

2.3.1 CPU Registers

The register set is divided into data registers that are used for arithmetic operations, etc., address registers that are used for pointers, and a stack pointer. This arrangement contributes greatly to the improved performance of the internal architecture, through reduction on instruction code size, improved parallelism in pipeline processing, etc. This register enables programming in C and other high-level languages. The loop instruction register (LIR) and the loop address register (LAR) are used to provide high-speed execution of branch instructions. High-speed loop control is performed by loading the branch target instruction and following fetch address with the SETLB instruction and forming the loop using the Lcc instruction.

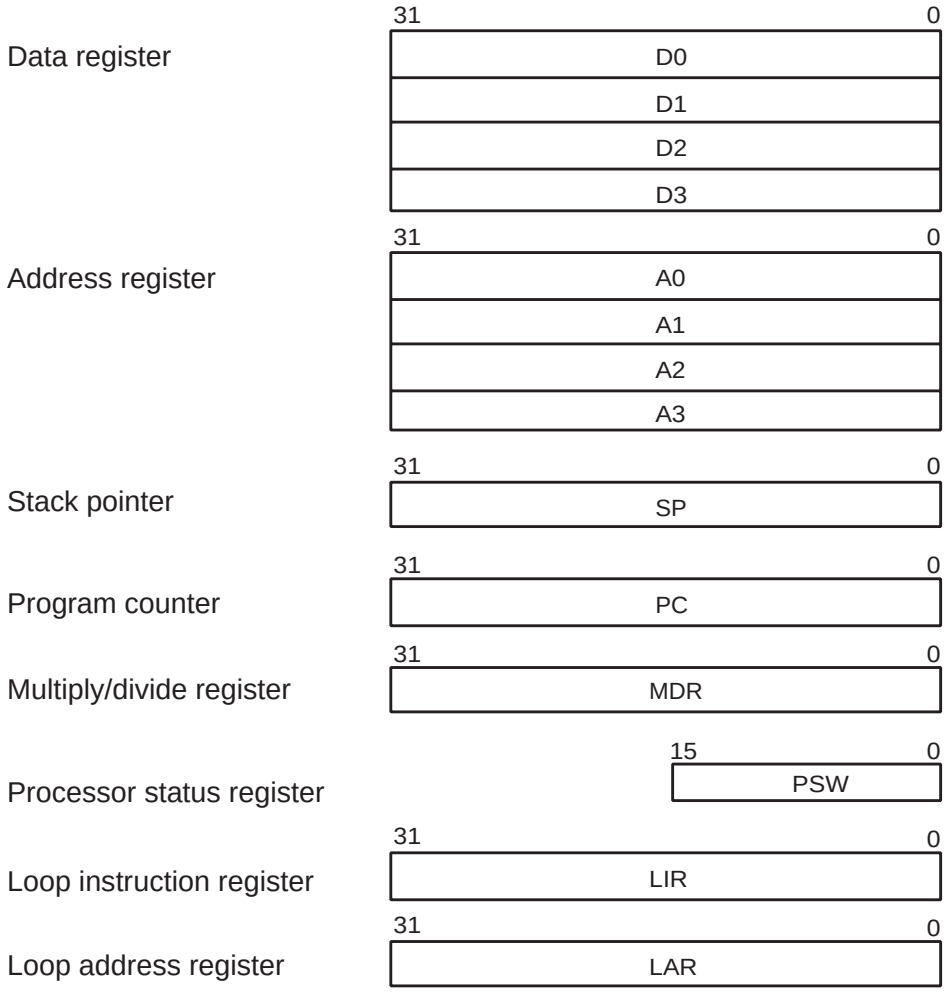


Figure:2.3.1 CPU Block Diagram

■ Data Register (32-bit x 4)

This register can be used generally for all operations. Operations are performed with a 32-bit length and the data size is converted when sending data to and from the memory or by executing of the EXTB or EXTH instructions. When loading data, 8-bit data is zero-extended to 32 bits and send to the register. When storing data, the lower 8 bits of the register are sent to the memory. When handling the loaded 8-bit data as a signed integer, the data is sign-extended from 8 bits to 32 bits with the EXTB instruction. When loading data, 16-bit data is zero-extended to 32 bits and sent to the register. When storing data, the lower 16 bits of the register are sent to the memory. When handling the loaded 16 bits data as a signed integer, the data is sign-extended from 16 bits to 32 bits with the EXYH instruction.

■ Address Register (32-bit x 4)

This register is used as an address pointer, and only instructions (addition, subtraction, and comparison) for address calculation are supported.

■ Stack Pointer (32-bit x 4)

This pointer designates the first address of the stack region.

■ Program Counter (32-bit x 1)

This counter designates the address of the instruction being executed.

■ Multiply/Divide Register (32-bit x 1)

This register is provided for multiply and divide instructions. It holds the upper 32 bits of 64-bit multiplication results for multiply instructions and the remainder (32 bits) for divide instructions. Also, the upper 32 bits of the dividend are loaded to this register before executing divide instructions.

■ Loop Instruction Register (32-bit x 1)

This register is provided for branch instruction (Lcc), and is used for storing the branch target instruction with SETLB instruction.

■ Loop Address Register (32-bit x 1)

This register is provided for branch instruction (Lcc), and is used for storing the fetch address with SETLB instruction.

■ Processor Status Word (16-bit x 1)

This register indicates the CPU status, and stores flags for operation results and interrupt mask level, etc.

Table:2.3.1 Processor Status Word

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	S1	S0	IE	IM2	IM1	IM0	-	-	-	-	V	C	N	Z
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-14	-	-	-
13-12	S1 S0	Software bit	These are the software control bits for the operating system (OS). These bits cannot be used by general user programs.
11	IE	Interrupt enable	0: disabled 1: enabled This flag permits and accepts all interrupts except reset and non-maskable interrupts. When the CPU accepts an interrupt request, the IE will be cleared to 0. Therefore, IE flag must be set to “1”, if nested interrupts need to be accepted in the interrupt processing program.
10-8	IM2 IM1 IM0	Interrupt mask level	The three bits defines the mask level from level 0 (000) to level 7 (111), with level 0 being the highest mask level. The CPU accepts only those interrupt requests of a level higher than the mask level indicated here. When an interrupt is accepted, the IM flag is set to the priority level of that interrupt. Until the processing of the accepted interrupt is completed, the CPU does not accept interrupts with the same interrupt level or lower.
7-4	-	-	-
3	V	Overflow flag	0: When an overflow does not occurs in a signed value in the course of executing an operation. 1: When an overflow occurs in a signed value in the course of executing an operation.
2	C	Carry flag	0: When a carry or a borrow from the most significant bit (MSB) did not occur as a result of computation. 1: When a carry or a borrow from the most significant bit (MSB) occured as a result of computation.
1	N	Negative flag	0: When the most significant bit (MSB) is "0" as a result of computation. 1: When the most significant bit (MSB) is “1” as a result of computation.
0	Z	Zero flag	0: Operation result is not “0”. 1: Operation result is “0”.

2.3.2 Control Registers

The microcontroller core uses the memory-mapped I/O method to allocate a variety of control registers in a control register address space between x'00008000 and x'00009FFF.

The registers listed below are described in this section. For details on other control registers, refer to the respective sections that explain the various built-in peripheral functions.

Table:2.3.2 Control Register

	Registers	Address	R/W	Access size	Function	Pages
CPU mode	CPUM	0x00008040	R/W	8, 16	CPU mode register	II-8

■ CPU Mode Register (CPUM: 0x00008040) [8, 16-bit Access Register]

This register is prohibited to access.

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	OSCID	STSEL	HASEL	SLSEL	OSC1	OSC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-0	-	System reserve	Setting prohibited

Never change the CPU mode register.

2.4 Data Formats

Data types can be processed in the four types of bit, byte, halfword and word data. Byte data, halfword data and word data can be handled as signed and unsigned data. The sign bit is MSB.

The data in the memory must be aligned data. In other words, the two bits on the LSB side of addresses storing word data must be "00" (addresses which are a multiple of 4), and the LSB of addresses storing halfword data must be "0" (addresses which are a multiple of 2).

Byte and bit placement conforms with the Little Endian format. Therefore, the address of the byte data on the MSB side of halfword data is the LSB side byte data address + 1, and the address of the byte data on the MSB side of word data is the LSB side byte data address + 3. The bit number for bit data starts at 0 on the LSB and increases towards the MSB.

Table:2.4.1 Data Types

Data type	Contents
Bit data	Bit data
Byte data	Unsigned 8-bit data Signed 8-bit data (sign bit: MSB)
Halfword data	Unsigned 16-bit data Signed 16-bit data (sign bit: MSB)
Word data	Unsigned 32-bit data Signed 32-bit data (sign bit: MSB)

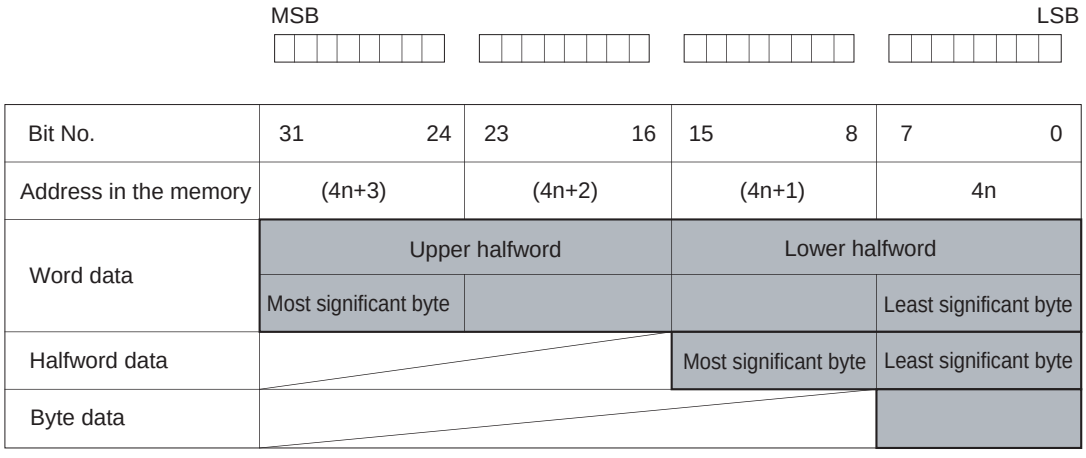


Figure:2.4.1 Little Endian Format

2.5 Instructions

2.5.1 Instruction Format

The following 11 types of instruction formats are available.

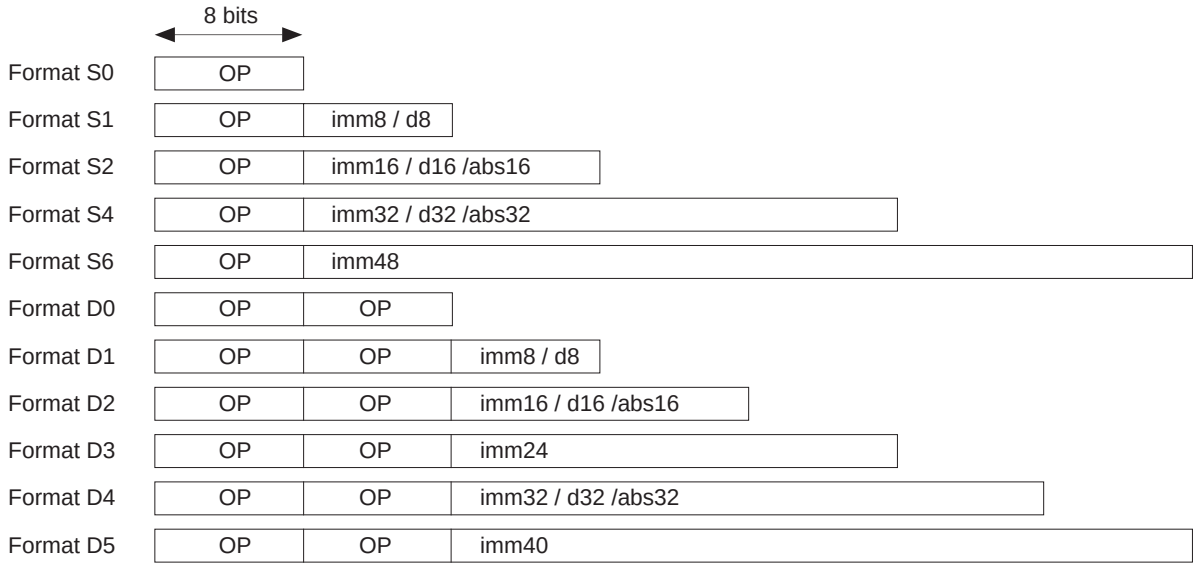


Figure:2.5.1 Types of Instruction Formats

Usually, 8-, 16-, or 32-bit immediate value, displacement, and absolute are connected after the operation code. In the case of the above instruction formats (S2, S4, S6, D2, D3, and D5), two or more of immediate value, displacement, and absolute are connected to the operation code. As a whole, these values express a 16-bit immediate value (imm16), 24-bit immediate value (imm24), 32-bit immediate value (imm32), 40-bit immediate value (imm40), and 48-bit immediate value (imm48). According to this expression method, the following instructions connect 16-, 32-, 40-, and 48-bit immediate values.

imm16:	RET	regs,imm8
	RETF	regs,imm8
	BTST	imm8,(d8,An)
	BSET	imm8,(d8,An)
	BCLR	imm8,(d8,An)
imm24:	BTST	imm8,(abs16)
	BSET	imm8,(abs16)
	BCLR	imm8,(abs16)
imm32:	CALL	(d16,PC),regs,imm8
imm40:	BTST	imm8,(abs32)
	BSET	imm8,(abs32)
	BCLR	imm8,(abs32)
imm48:	CALL	(d32,PC),regs,imm8

2.5.2 Addressing Modes

The 32-bit microcontroller is equipped with the following 6 addressing modes which are frequently used with compilers. All 6 addressing modes of register direct, immediate value, register indirect, register indirect with displacement, absolute and register indirect with index can be used with data transfer group instructions. The 2 addressing modes of register direct and immediate addressing can be used with register operation instructions. Register indirect with index addressing is an addressing mode used to efficiently access arrays and other data.

Table:2.5.1 Addressing Mode Types

Addressing mode		Address calculation	Effective address
Register direct	Dm / Dn Am / An SP /PSW / MDR	—	—
Immediate value	imm8 / regs imm16 imm24 imm32 imm40 imm48	—	—
Register indirect	(Am) / (An)	31 0 Am/An	31 0 (32-bit address)
Register indirect with displacement	(d8,Am) / (d8,An) :d8 is sign-extended (d16,Am) / (d16,An) :d16 is sign-extended (d32,Am) / (d32,An)	31 0 Am/An + 31 15 7 0 d32/d16/d8	31 0 (32-bit address)
	(Branch instructions only) (d8,PC) :d8 is sign-extended (d16,PC) :d16 is sign-extended (d32,PC)	31 0 PC + 31 15 7 0 d32/d16/d8	31 0 (32-bit address)
	(d8,SP) :d8 is zero-extended (d16,SP) :d16 is zero-extended (d32,SP)	31 0 SP + 31 15 7 0 d32/d16/d8	31 0 (32-bit address)
Absolute	(abs16) :abs16 is zero-extended (abs32)	31 15 0 abs32/abs16	31 0 (32-bit address)
Register indirect with index	(Di,Am) / (Di,An)	31 0 Am/An + 31 0 Di	31 0 (32-bit address)

2.5.3 Instruction Set

The instruction set has a simple organization, and features the generation of compact and optimized code through a C compiler. Basic instructions are one byte in length. Although these instructions are simple and provided with limited data transfer functions (load/store functions), the instructions make it possible to reduce an expansion in code size of assembler programs to the minimum.

Table:2.5.2 Instruction Types (All 46 types and extension instructions)

Transfer instructions	Transfer MOV MOVBU MOVHU MOVM	Sign extention EXT EXTB EXTBU EXTH EXTHU	Clear CLR	
Arithmetic instructions	Addition ADD ADDC INC INC4	Substruction SUB SUBC	Multiplication MUL MULU	Division DIV DIVU
Compare instructions	Compare CMP			
Logical instructions	Logical add OR	Logical product AND	Inversion NOT	Exclusive logical add XOR
Bit instructions	Test BTST	Test Test and set BSET	Test and clear BCLR	
Shift instructions	Shift ASR LSR ASL ASL2	Rotate ROR ROL		
Branch instructions	Branch Bcc Lcc JMP	Loop set SETLB	Subroutine call CALL CALLS TRAP	Return RET RETF RETS RTI
NOP instructions	No operation NOP			
Extension instructions	Expansion UDF UDFU			

Note: Interrupts are prohibited and the bus is locked (occupied by the CPU) when executing BSET or BCLR.

■ Transfer Instructions

Transfer instructions are used for register-to-register, memory-to-register, or memory-to registers (or register-to-memory or registers-to-memory) data transfer. Transfer instructions are classified into MOV-, EXT-, and CLR-type instructions. MOV-type instructions provide data transfer functions in a variety of addressing modes. Displacement and immediate values will be sign expanded according to the operation. EXT-type instructions provide a register-to-register transfer function involving sign expansion. CLR-type instructions provide a register clear function (with 0 transferred). No flag change will be involved unless CLR-type instructions are used.

Table:2.5.3 Transfer Instructions

Instruction	Description
MOV	Register-to-register word data transfer Register-to-memory (or memory-to-register) word data transfer Transfer of immediate value to register
MOVBU	Register-to-memory (or memory-to-register) byte data transfer (zero expansion)
MOVHU	Register-to-memory (or memory-to-register) half-word data transfer (zero expansion)
MOVM	Register-to-memory (or memory-to-registers) data transfer
EXT	64-bit sign expansion of word data
EXTB	32-bit sign expansion of byte data
EXTBU	32-bit sign expansion of byte data
EXTH	32-bit zero expansion of byte data
EXTHU	32-bit zero expansion of half-word data
CLR	Data clear

■ Arithmetic Operation Instructions

These instructions are used for the arithmetic operation between source operands, the results of which are stored in a register. All of these instructions involve flag changes. The “+1” and “+4” operations, which are used frequently in address calculations, are adopted as independent instructions.

Table:2.5.4 Arithmetic Operation Instructions

Instruction	Description
ADD	Addition
ADDC	Addition with carry
SUB	Subtraction
SUBC	Subtraction with borrow
MUL	Signed multiplication
MULU	Multiplication with no sign
DIV	Signed division
DIVU	Division with no sign
INC	Added with 1
INC4	Added with 4

■ Comparison Instruction

This instruction is used to compare register data with other register data or an immediate value with register data. The comparison instruction is used prior to the condition branching instruction. The comparison instruction involves flag changes.

Table:2.5.5 Comparison Instruction

Instruction	Description
CMP	Comparison

■ Logic Operation Instructions

These instructions are used for the logic operation between source operands, the results of which are stored in a register. All instructions involve flag changes.

Table:2.5.6 Logic Operation Instructions

Instruction	Description
AND	Logical product
OR	Logical sum
XOR	Exclusive logical sum
NOT	Inversion (1's complement)

■ Bit Control Instructions

These instructions are used to operate the bit control instructions between immediate value and register data, immediate value and memory data, and register data and memory data. All instructions involve flag changes.

Table:2.5.7 Bit Control Instructions

Instruction	Description
BTST	Testing multiple of bits
BSET	Testing and setting multiple of bits (processing unit: bytes)
BCLR	Testing and clearing multiple of bits (processing unit: bytes)

■ Shift Instructions

These instructions are used to shift bits as specified. Each instruction is executed at one cycle regardless of the shift amount. All instructions involve flag changes.

Table:2.5.8 Shift Instructions

Instruction	Description
ASR	Arithmetic right shift of any number of bits
LSR	Logical right shift of any number of bits
ASL	Arithmetic left shift of any number of bits
ASL2	Arithmetic left shift of two bits
ROR	1-bit right rotate
ROL	1-bit left rotate

■ Branching Instructions

These instructions are used to make flow changes in program execution according to the given conditions. Conditional branching instructions are classified into normal conditional branching instructions and loop-dedicated conditional branching instructions. A loop-dedicated conditional branching instructions uses a dedicated register, thus minimizing the branching penalty and ensuring high-speed loop execution. The subroutine call and return are provided with highly functional specifications which manipulate the PC, save and restore multiple registers to and from the stack, and allocate and release stack area.

Table:2.5.9 Branching Instructions

Instruction	Description
Bcc	Conditional branching (PC-relative)
Lcc	Loop-dedicated conditional branching
SETLB	Set start of loop
JMP	Non-conditional branching (PC-relative and register-indirect)
CALL	Subroutine call (high-function type)
CALLS	Subroutine call
RET	Return from subroutine (high-function type)
RETF	Return from subroutine (high-function, high-speed type)
RETS	Return from subroutine
RTI	Return from interrupt program
TRAP	Subroutine call to fixed address

■ NOP Instruction

This instruction does not execute anything, but it is possible to advance one-cycle time without having any influence on any resources by executing the NOP instruction.

Table:2.5.10 NOP Instruction

Instruction	Description
NOP	No operation

■ Extension Instructions

These instructions are defined for extension operation units of add-on type. An extension instruction uses a fixed instruction format. The instruction map is reserved. This microcontroller incorporates 30 extension instructions including high-speed multiplication and sum-of-products operation instructions. For instructions in detail, see Appendix B Expansion Instruction Specifications.

2.6 Memory Space

2.6.1 Overview

This LSI has 4 GB linear address space in which addresses are expressed with 32 bits. The address space consists of the internal ROM space which places built-in memory (ROM/RAM) into the chip and the internal RAM space, the control register space stored various control registers of the microcontroller core, the internal I/O space for the interface of peripheral circuits. Instruction strings can be placed in the internal ROM space which places the internal memory (ROM) mainly stored instructions. Also, it is possible to execute by spacing instruction strings in the internal RAM space temporarily. Data can be stored anywhere in memory, and can be referred via the MOV instruction. Efficient programming is possible because all addressing modes can be used to access data.

2.6.2 Memory Map

Table: 2.6.1 shows memory map in MN103SA7 series. Refer to 1.1.2 Product Summary in Chapter 1 for ROM and RAM capacity of products.

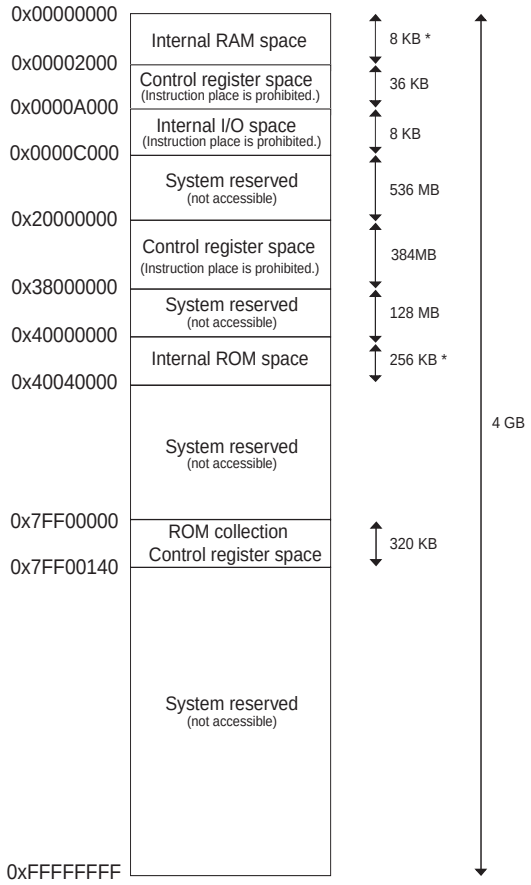


Figure:2.6.1 Memory Map

* Vary by model. Refer to Table 2.6.1. Internal ROM/RAM by model.

Table:2.6.1 Internal ROM/RAM by model

Model	Internal ROM space	ROM size	Internal RAM space	RAM size
MN103SA7D	0x40000000 to 0x4000FFFF	64 KB	0x00000000 to 0x00000FFF	4 KB
MN103SA7G	0x40000000 to 0x4001FFFF	128 KB		
MN103SFA7K	0x40000000 to 0x4003FFFF	256 KB	0x00000000 to 0x00001FFF	8 KB

The operation at the unmounted space access is not assured such as accessing to the internal ROM/ RAM space which has no memory (ROM/RAM) or the internal I/O space without the control register. It is prohibited to execute by placing instructions in 0x00002000 to 0x3FFFFFFF.

2.6.3 Register Map

Table:2.6.2 shows the register map.

Table:2.6.2 Branch Instructions

Address	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
x'0000800X			IVAR3				IVAR2				IVAR1				IVAR0		Interrupt vector
x'0000801X							IVAR6				IVAR5				IVAR4		
x'0000804X															CPUM		CPU control
x'0000807X							ROMCTR										
x'0000820X												RSTCTR		WDCTR		WDBC	Watchdog
x'0000828X															CKCTR		Clock generator
x'0000890X			G3ICR				G2ICR				Reserved				G0ICR		Interrupt control
x'0000891X			G7ICR				G6ICR				G5ICR				G4ICR		
x'0000892X			G11ICR				G10ICR				G9ICR				G8ICR		
x'0000893X			G15ICR				G14ICR				G13ICR				G12ICR		
x'0000894X			G19ICR				G18ICR				G17ICR				G16ICR		
x'0000895X			G23ICR				G22ICR				G21ICR				G20ICR		
x'0000896X			G27ICR				G26ICR				G25ICR				G24ICR		
x'0000897X							G30ICR				G29ICR				G28ICR		
x'00008A0X															IAGR		
x'00008A8X											EXTMD1				EXTMD0		
x'0000A00X					Reserved	PAOUT	P9OUT	P8OUT	P7OUT	P6OUT	P5OUT	P4OUT	P3OUT	P2OUT	P1OUT		General port
x'0000A01X					Reserved	PAIN	P9IN	P8IN	P7IN	P6IN	P5IN	P4IN	P3IN	P2IN	P1IN		
x'0000A02X					Reserved	PADIR	P9DIR	P8DIR	P7DIR	P6DIR	P5DIR	P4DIR	P3DIR	P2DIR	P1DIR		
x'0000A03X					Reserved	PAMD	P9MD	Reserved	P7MD	P6MD	P5MD	P4MD	P3MD	P2MD	P1MD		
x'0000A04X					Reserved	PAPLU	P9PLU	P8PLU	P7PLU	P6PLU	P5PLU	P4PLU	P3PLU	P2PLU	P1PLU		
x'0000A05X									IRQEDGESEL		NFCNT		NFCLK1		NFCLK0		Noise filter
x'0000A10X		SIFCLK		SC0TB			SC0STR					SC0RB			SC0CTR		Serial I/F
x'0000A11X				SC1TB			SC1STR					SC1RB			SC1CTR		
x'0000A12X				SC2RB				SC2STR			SC2 CTR3	SC2 CTR2			SC2 CTR1	SC2 CTR0	
x'0000A13X																SC2TB	
x'0000A18X			TM3BR	TM2BR			TM1BR	TM0BR			TM3MD	TM2MD			TM1MD	TM0MD	8-bit timer
x'0000A19X				TMEX PSC8				TM03 PSC			TM3BC	TM2BC			TM1BC	TM0BC	
x'0000A1AX			TM7BR	TM6BR			TM5BR	TM4BR			TM7MD	TM6MD			TM5MD	TM4MD	
x'0000A1BX								TM47 PSC			TM7BC	TM6BC			TM5BC	TM4BC	
x'0000A1CX			TM17BR	TM16BR			TM15BR	TM14BR			TM17MD	TM16MD			TM15MD	TM14MD	
x'0000A1DX								TM14 17PSC			TM17BC	TM16BC			TM15BC	TM14BC	
x'0000A20X			TM8CB				TM8CA				TM8MDB	TM8MDA			TM8MD		16-bit timer
x'0000A21X								TMEXP SC16				TM8PSC			TM8BC		
x'0000A22X			TM9CB				TM9CA				TM9MDB	TM9MDA			TM9MD		
x'0000A23X												TM9PSC			TM9BC		
x'0000A24X			TM10CB				TM10CA				TM10 MDB	TM10 MDA			TM10MD		
x'0000A25X												TM10 PSC			TM10BC		
x'0000A26X			TM11CB				TM11CA				TM11 MDB	TM11 MDA			TM11MD		
x'0000A27X												TM11 PSC			TM11BC		
x'0000A28X			TM12CB				TM12CA				TM12 MDB	TM12 MDA			TM12MD		
x'0000A29X								TM12 CLKSEL				TM12 PSC			TM12BC		
x'0000A2AX			TM13CB				TM13CA				TM13 MDB	TM13 MDA			TM13MD		
x'0000A2BX								TM13 CLKSEL				TM13 PSC			TM13BC		

Address	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
x'0000A30X			PWMSET0				PWMSEL0				OUTMD0				PWMMD0		PWM
x'0000A31X			DTMSET0				TCMP0C				TCMP0B				TCMP0A		
x'0000A32X							PWMDCNT0				BCSTR0				PWMBC0		
x'0000A33X			PWMSET1				PWMSEL1				OUTMD1				PWMMD1		
x'0000A34X			DTMSET1				TCMP1C				TCMP1B				TCMP1A		
x'0000A35X							PWMDCNT1				BCSTR1				PWMBC1		
x'0000A36X															PWMOFF		
x'0000A40X			AN0CTREGB	AN0CTREGA				ADST0			AN0CTR1				AN0CTR0		A/D
x'0000A41X			AN0BUF03				AN0BUF02				AN0BUF01				AN0BUF00		
x'0000A42X			Reserved				Reserved				AN0BUF05				AN0BUF04		
x'0000A43X											Reserved				AN0BUF0B		
x'0000A44X			AN1CTREGB	AN1CTREGA				ADST1			AN1CTR1				AN1CTR0		
x'0000A45X			AN1BUF05				AN1BUF04				AN1BUF03				AN1BUF02		
x'0000A46X			AN1BUF09				AN1BUF08				AN1BUF07				AN1BUF06		
x'0000A47X											Reserved				AN1BUF0B		
x'0000A48X				AN2CTREGA				ADST2			AN2CTR1				AN2CTR0		
x'0000A49X			AN2BUF09				AN2BUF08				AN2BUF07				AN2BUF06		
x'0000A4AX			AN2BUF13				AN2BUF12				AN2BUF11				AN2BUF10		
x'0000A4BX			Reserved				Reserved				AN2BUF15				AN2BUF14		
x'0000A4CX			Reserved				Reserved				Reserved				Reserved		
x'0000A51X			Reserved				Reserved				Reserved				Reserved		Others
x'0000AFFX			Reserved				Reserved				Reserved		PCNT		Reserved		
x'7FF0000X																RCRCTR	ROM correction
x'7FF0010X	RCR0DR												RCR0AR				
x'7FF0011X	RCR1DR												RCR1AR				
x'7FF0012X	RCR2DR												RCR2AR				
x'7FF0013X	RCR3DR												RCR3AR				

2.7 Operation Mode

2.7.1 Overview

This LSI provides only NORMAL mode as CPU operation mode. Low power consumption mode and other mode are not provided.

2.7.2 Reset Status

■ External Reset Pin Input

If the reset pin (NRST) goes “L” level, the chip resets (initializes) itself internally and if the reset pin goes “H” level, the wait for oscillation to stabilize starts by means of the 18-bit binary counter that is driven by the oscillation clock.

After the wait for oscillation stabilization is completed, the internal rest is released and the microcontroller enters normal operation mode. Refer to [11.3.1 Oscillation Stabilization Wait Operation] for the wait for oscillation stabilization.

■ Self Reset

Self reset is generated by setting the CHIPRST flag of the reset control register (RSTCTR) to from “0” to “1”. When the CHIPRST flag is “1”, self reset is not generated even if “1” is set. The CHIPRST flag retains the value even after self reset. Reset by the self reset is internal reset in the chip, so is not generated by the external reset pin. Also, oscillation stabilization wait operation is not generated. Refer to [11.2.4 Reset Control Register] for reset control register.

Table: 2.7.1 shows the status of the CPU registers right after the reset.

Table:2.7.1 CPU Register Status Right After the Reset

Register		Values
Program counter	PC	0x40000000
Data counter	D0 toD3	Undefined
Address register	A0 to A3	Undefined
Stack pointer	SP	Undefined
Multiply / divide register	MDR	Undefined
Processor status word	PSW	0x0000
Loop instruction register	LIR	Undefined
Loop address register	LAR	Undefined

■ Power Supply Detection Reset

Reset is generated when the power is on for the internal chip. The power supply voltage reaches to the power supply detection level, the oscillation stabilization wait starts. After the oscillation stabilization wait is completed, the internal reset is released and changes to the normal operation status mode (NORMAL mode). Also, when the power supply voltage drops to the power supply detection level, the reset is generated for the internal chip. When the power supply voltage changes more rapidly than the power supply voltage change rate defined in the electric characteristics, the reset may not be generated.

Internal RAM is undefined when the power supply is on. Initialize it before using.

Chapter 3 Clock Generator

3

3.1 Overview

The clock generator has an internal PLL circuit and supplies a frequency that is a multiple of the oscillating frequency of the oscillator to this microcontroller and peripheral circuit.

3.1.1 Functions

Table.3.1.1 shows the functions of the clock generator.

Table:3.1.1 Functions of Clock Generator

Functions	Description
Oscillation support	Self-excited / externally excited oscillation
Oscillating frequency	Maximum: 15.0MHz
System clock (MCLK))	Supplies 1/2, 1, 1.5, 2, 3, 4, 6 and 8 multiplication of the oscillating frequency (Maximum 60.0 MHz)
Peripheral clock (LOCLK)	Supplies 1/4, 1/2, 0.75, 1, 1.5, 2, 3 and 4 multiplication the oscillating frequency (Maximum 30.0 MHz)

3.1.2 Block Diagram

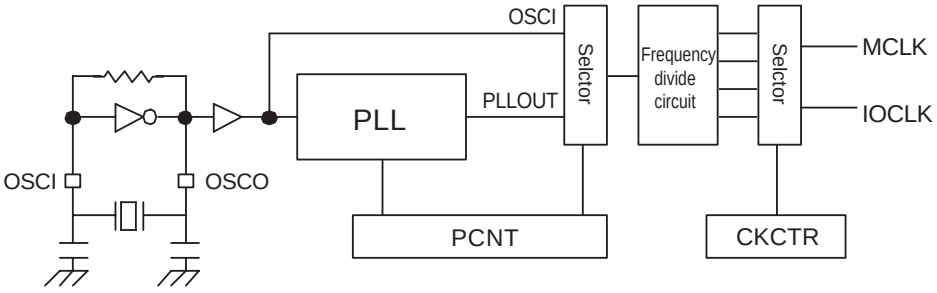


Figure:3.1.1 Block Diagram of Clock Generator

3.2 Control Registers

3.2.1 Clock Generator Control Register

Table:3.2.1 shows the internal clock supply.

Table:3.2.1 Clock Generator Control Register

	Register	Address	R/W	Access size	Description	Page
Clock generator	PCNT	0x0000AFF2	R/W	8, 16	PLL control register	III-3
	CKCTR	0x00008280	R/W	8, 16	Clock control register	III-5

R/W Readable / Writable
R Readable
W Writable

3.2.2 PLL Control Registers

■ PLL Control Register (PCNT: 0x0000AFF2) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	PLL SEL	-	PLL ON	-	CK SEL1	CK SEL0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R/W

bp	Flag	Description	Set condition
15-6	-	-	-
5	PLLSEL	Select the PLL output	0: Oscillation clock (OSCI) 1: PLL output
4	-	-	-
3	PLLON	Set the PLL ON/OFF	0: PLL ON 1: PLL OFF
2	-	-	-
1-0	CKSEL1 CKSEL0	Select the PLL multiplication ratio of oscillation frequency	00: 4 multiplication of oscillation frequency 01: 6 multiplication of oscillation frequency 10: 8 multiplication of oscillation frequency 11: Setting prohibited When changing the PLLON flag and the CKSEL[1:0] flag of the PCNT register, the PLLSEL flag must be set to "0". And then, set the PLLSEL flag to "1" after waiting for more than 200 µs

Set the register to become the oscillation frequency × PLL multiplication ratio of oscillation frequency = 40 MHz to 60 MHz.

When the PLLON and CKSEL [1:0] flags of the PCNT register are changed, reset the PLLSEL flag to “0” before the change and set to “1” after waiting over 200 μs.

3.2.3 Clock Control Registers

■ Clock Control Register (CKCTR: 0x00008280) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	SCK1	SCK0	IOCK1	IOCK0	CGECK1	CGECK0	MCK1	MCK0
At reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-8	-	-	-
7-6	SCK1 SCK0	Reserved	Always set “10”.
5-4	IOCK1 IOCK0	Set the frequency of IOCLK	00: Setting prohibited 01: 1/8 of the clock selected by the PCNT register 10: 1/4 of the clock selected by the PCNT register 11: 1/2 of the clock selected by the PCNT register
3-2	CGECK1 CGECK0	Reserved	Always set “00”.
1-0	MCK1 MCK0	Set the frequency of MCLK	00: Setting prohibited 01: 1/4 of the clock selected by the PCNT register 10: 1/2 of the clock selected by the PCNT register 11: 1/1 of the clock selected by the PCNT register

3.3 Operation

3.3.1 Internal Clock Supply

■ Internal Clock Supply

Table:3.3.1 shows the internal clock supply.

Table:3.3.1 Internal Clock Supply (Multiplying Power to Oscillation Frequency)

Operation clock	Setting condition MCK [1 : 0], IOCK [1 : 0]				Destination
	PLL non-selective	PLL 4 multiplication	PLL 6 multiplication	PLL 8 multiplication	
System clock (MCLK)	00 : - 01 : - 10 : - 11 : 1/2 times	00 : - 01 : 1 times 10 : 2 times 11 : 4 times	00 : - 01 : 1.5 times 10 : 3 times 11 : 6 times	00 : - 01 : 2 times 10 : 4 times 11 : 8 times	CPU core Internal RAM Internal ROM Bus controller
System clock (IOCLK)	00 : - 01 : - 10 : - 11 : 1/4 times	00 : - 01 : 1/2 times 10 : 1 times 11 : 2 times	00 : - 01 : 0.75 times 10 : 1.5 times 11 : 3 times	00 : - 01 : 1 times 10 : 2 times 11 : 4 times	Internal peripheral function

* "_" is "setting prohibited"

* is status at reset release

Be sure to set the frequency of IOCLK to IOCLK ≤ 1/2MCLK.

■ At Reset Release

Supply to MCLK and IOCLK starts after a certain oscillation stabilization wait. When the oscillation frequency is 10 MHz, the oscillation stabilization wait time is 26.21 ms. Refer to [11.3.1 Oscillation Stabilization Wait Operation] for the oscillation stabilization wait.

Table:3.3.2 Frequency at Reset Release

Operation clock	Clock frequency
System clock (MCLK)	1/2 of oscillation frequency
System clock (IOCLK)	1/4 of oscillation frequency

Be sure to set the frequency of IOCLK to IOCLK ≤ 1/2MCLK.

3.3.2 Setup of Input Frequency

Input frequency range of clock generator is 5 MHz (minimum) and 15 MHz (maximum). When the input clock is multiplied, the PLL output frequency (PLLOUT) needs to be set to be 40 MHz to 60 MHz. Table: 3.3.3 shows the input frequency and PLL multiple magnification to be set.

Table:3.3.3 Setting of PLL Multiple Magnification for Input Frequency

Input frequency	PLL multiple magnification		
	4 multiplication	6 multiplication	8 multiplication
5 MHz	Setting prohibited	Setting prohibited	40 MHz
7 MHz	Setting prohibited	42 MHz	56 MHz
8 MHz	Setting prohibited	48 MHz	Setting prohibited
10 MHz	40 MHz	60 MHz	Setting prohibited
15 MHz	60 MHz	Setting prohibited	Setting prohibited

3.3.3 Connection Example of Oscillator

Figure 3.3.1 shows basic configuration connected with a ceramic oscillator, and table 3.3.4 shows recommended oscillators and the circuit constants.

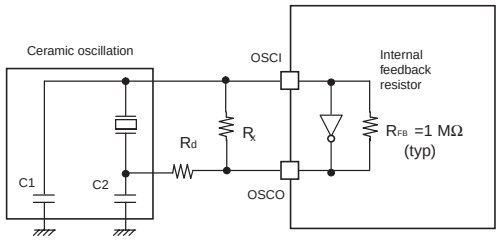


Figure:3.3.1 Connection Example of Ceramic Oscillator

Table:3.3.4 Recommended Ceramic Oscillator and Circuit Constant

Frequency [Hz]	Type	Ceramic oscillator Product Number‘	Recommended circuit constant		
			Load Capacity C1=C2 [pF]	External feedback resistor Rx [Ω]	Dumping resistor Rd [Ω]
5.000M	lead	CSTLS5MOOG56-B0	(47)	Open	0
	SMD	CSTCR5MOOG55-R0	(39)	Open	0
7.000M	lead	CSTLS7MOOG56-B0	(47)	Open	0
	SMD	CSTCR7MOOG55-R0	(39)	Open	0
8.000M	lead	CSTLS8MOOG56-B0	(47)	Open	0
	SMD	CSTCE8MOOG55-R0	(33)	Open	0
10.000M	lead	CSTLS10MOG56-B0	(47)	Open	0
	SMD	CSTCE10MOG55-R0	(33)	Open	0
15.000M	SMD	CSTCE15MOV53-R0	(15)	Open	0

* ( ) shows capacity built into the oscillator.

Above recommended ranges are based on unit oscillating evaluation of this LSI. After evaluating the actual oscillating on the target board, determine the final circuit constant, if necessary.

We do not evaluate oscillating of crystal oscillator on this LSI. Set the circuit constant that the oscillator manufacturer recommends.

Consult the oscillator manufacturer for the appropriate circuit constant because circuit constant of each ceramic or crystal oscillator, which is connected to OSCI/OSCO, depending on stray capacitance of the oscillator or on the mounting circuit.

When switching the masked ROM and flash EEPROM version, matching evaluation of each version and the oscillator is necessary. The masked ROM and flash EEPROM version may have different oscillating characteristics.

3.3.4 Setup Example of Internal Clock

The frequency of the internal clock (MCLK and IOCLK) is determined by setting the PLL control register and the clock control register.

The following table shows the setting sequence when the oscillator of 10 MHz is connected and operated with 6 multiple by PLL.

Operation clock	Internal clock	
	After reset is released	After the setting
System clock (MCLK)	1/2 of oscillation frequency (5 MHz)	6 multiplication of oscillation frequency (60 MHz)
Peripheral clock (IOCLK)	1/4 of oscillation frequency (2.5 MHz)	3 multiplication of oscillation frequency (30 MHz)

Setup Procedure	Description
(1) Set the multiplication ratio PCNT (0x0000AFF2) bp5: PLLSEL=0 bp3: PLLON=0 bp1: CKSEL1=0 bp0: CKSEL0=1	(1) Set the PLL multiplication ratio to 6 by the CKSEL 1 and CKSEL0 of the PLL control register (PCNT). Note: Set the frequency (oscillation frequceny × multiplication ratio) to 40MHz≤PLLOUT≤60MHz
(2) Wait PLL lock time over 200 μs	(2) Wait 200 μs by the execution of the loop program etc.
(3) Select PLL output PCNT (0x0000AFF2) bp5: PLLSEL=1 bp3: PLLON=0 bp1: CKSEL1=0 bp0: CKSEL0=1	(3) Set the PLLSEL of the PLL control register (PCNT) to “1” to select the PLL output to the internal clock. Note: Do not change the values of PLLON, CKSEL1 and CKSEL0.
(4) Set the frequency of MCLK and IOCLK CKCTR (0x00008280) bp5: IOCLK1=1 bp3: IOCLK0=1 bp1: MCK1=1 bp0: MCK0=1	(4) Set the cycle division of MCLK and IOCLK. This setting is not necessary when MCLK=PLLOUT and IOCLK=1/2PLLOUT.

When the CPU clock (MCLK) is 40 MHz or over, change an access to the internal ROM to 3 cycle access (ROMMC[1:0]=10) by the internal ROM access control register (ROMCTR) before the PLLSEL flag of the PLL control register (PCNT) is switched "0" to "1".
The operation that is set to 2 cycle access is not guranteed.

When the PLLON and CKSEL [1:0] flags of the PCNT register are changed, reset the PLLSEL flag to “0” before the change and set to “1” after waiting over 200 μs.

Chapter 4 Bus Controller

4

4.1 Overview

The bus controller controls interfacing between the CPU and internal peripheral circuitry.

4.1.1 Functions

Table:4.1.1 shows the functions of the bus controller.

Table:4.1.1 Functions

Functions	Description
Internal bus	Provides high-speed control by means of the system clock (MCLK)
Store buffer	Avoids time penalty during storage operation by the store buffer of single stage Supports for storage in the internal peripheral circuitry When the store buffer is empty, storage operation is completed with no wait states, and the CPU can execute successive processing

4.1.2 Block Diagram

■ Bus Controller Block Diagram

The bus controller is comprised of a control section, CPU interface section and peripheral circuitry interface section.

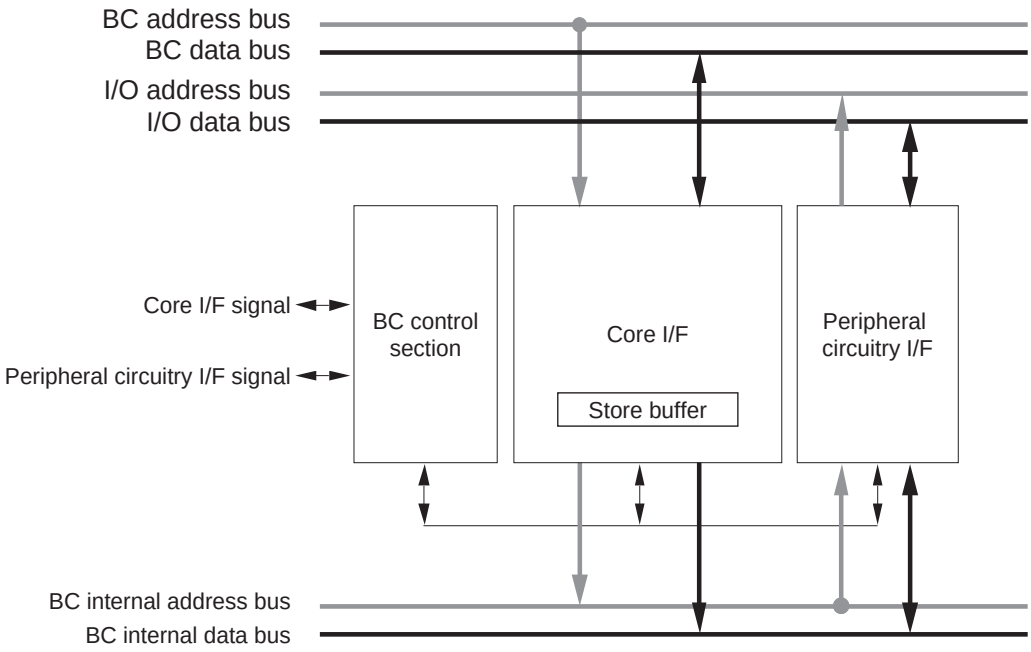


Figure:4.1.1 Bus Controller Block Diagram

4.2 Operation

4.2.1 Operation of Bus Controller

■ Bus Configuration

The ROM bus between the CPU and internal ROM, the RAM bus between the CPU and internal RAM, the BC bus between the CPU and bus controller, and the I/O bus between the bus controller and internal peripheral circuitry are available as the chip's internal buses. The characteristics of each bus and the bus configuration are shown in the following table and figure.

Table:4.2.1 Characteristics of Each Bus

Bus name	Blocks	Bus width	Operating clock
ROM bus	CPU to internal ROM	64	MCLK
RAM bus	CPU to internal RAM	32	MCLK
BC bus	CPU to BC	32	MCLK
I/O bus	BC to internal I/O	32	IOCLK
Refer to chapter 3, " Clock Generator" for MCLK and IOCLK.			

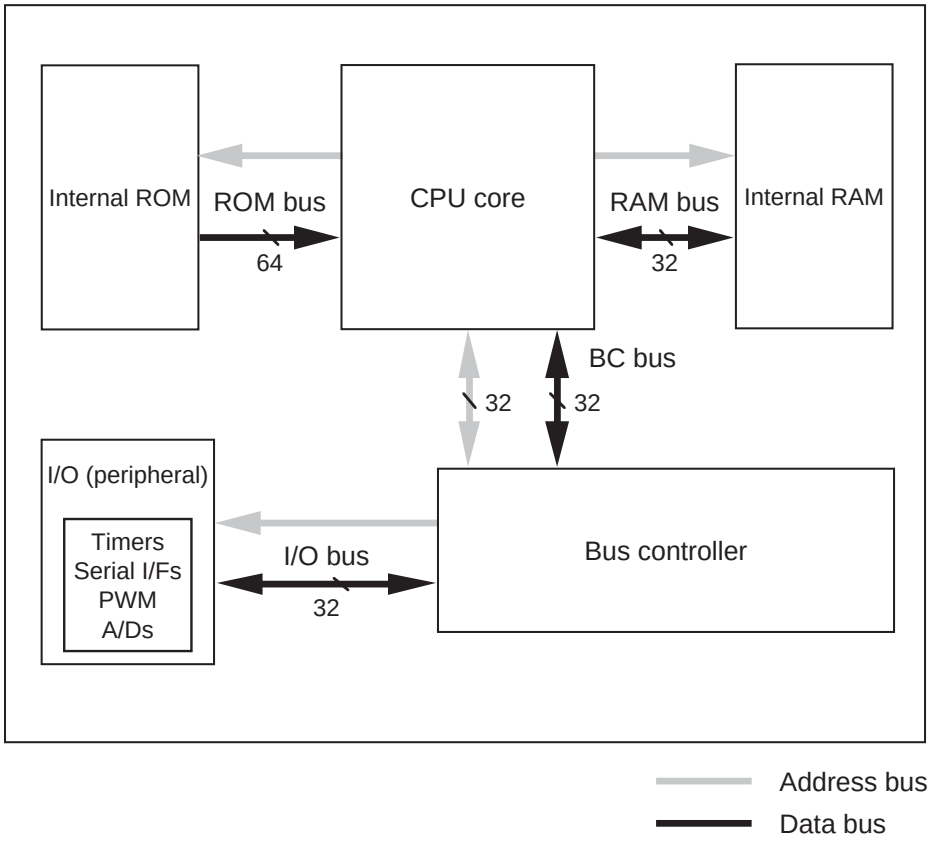


Figure:4.2.1 Bus Configuration

■ Data Access Timing

Data access to peripheral circuitry in the internal I/O space is performed in synchronization with IOCLK. Figure: 4.2.2 shows the data access timing chart of the internal I/O space. The address (ABIOA[30:0]), the chip select signal (NABIOCS[n]) and the read enable signal (NABIORE) are output simultaneously at the falling edge of IOCLK(AKIOCLK), while the peripheral circuitry starts to drive the data onto the read data signal (ABIORD[31:0]). The data on the read data signal is read simultaneously at the falling edge of IOCLK where the access cycle is terminated.

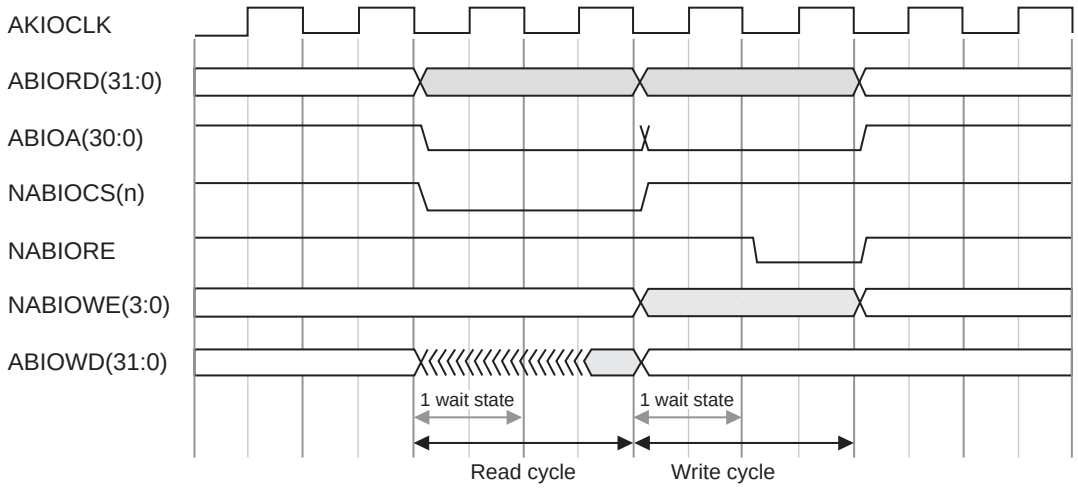


Figure:4.2.2 Data Access Timing in the Internal I/O Space

■ Basic Bus Cycle Count

Refer to chapter 3 “ Clock Generator” for the frequency of MCLK and IOCLK.

Table:4.2.2 Relationship between Clock Frequency and Access Cycle Count (CPU Cycle)

Accessed destination		MCLK (cycle count)	IOCLK (cycle count)
Internal ROM	Instruction read	3 cycles	-
	Data read	3 cycles	-
Internal RAM	Instruction read	4 cycles	-
	Data read/write	1 cycles	-
Control register inside CPU	Read	3 cycles	-
	Write	2 cycles	-
Control register outside CPU (Control register space)	Read	3 cycles	-
	Write	2 cycles	-
Internal I/O (Internal I/O space)	Read (*2)	2 cycles	I/O bus cycle
	Write (*1)(*2)	1 cycles	I/O bus cycle

(*!) : Each of all writes for the internal I/O is performed in 1 cycle by the use of the store buffer.
(*2) : Up to 3 cycles of synchronization wait occur.
The total of MCLK and IOCLK cycle count

■ Store Buffer

The bus controller has one store buffer (with a 32-bit data width) to avoid time penalty when conducting storage operation in internal I/O. The CPU storage operation is completed when the address, data and access size are stored in the store buffer, and is executed with no wait states. Writes from the store buffer to the internal I/O are conducted in parallel with subsequent CPU operations. However, if there is a request from the CPU for loading or storing to the internal I/O before writing from the store buffer is completed, execution of the request is delayed.

4.2.2 Internal ROM access control register

The internal ROM and internal flash memory can access in 2 cycles when the CPU clock (MCLK) is under 40 MHz.

Access cycle is set by the ROM access control register (ROMCTR).

■ Internal ROM Access Control Register (ROMCTR: 0x00008078) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	Reserved	Reserved	ROMWC1	ROMWC0	-	-	-	Reserved	Reserved	Reserved	-	-
At reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
15-12	-	-	-
11-10	Reserved	Reserved	Always set “00”
9-8	ROMWC[1:0]	Set the internal ROM access cycle count	00: Setting prohibited 01: 2 cycle(2 ×MCLK) access If CPU clock (MCLK) becomes 40 MHz or over, it is prohibited. 10: 3 cycle(3 ×MCLK) access When the CPU clock (MCLK) is 40 MHz or over, change an access to the internal ROM to 3 cycle access (ROMMC[1:0]=10) by the internal ROM access control register (ROMCTR) before the PLLSEL flag of the PLL control register (PCNT) is switched from "0" to "1". The operation that is set to 2 cycle access is not guranteed. 11: Setting prohibited
7-5	-	-	-
4-2	Reserved	Reserved	Always set “001”
1-0	-	-	-

When the CPU clock (MCLK) is 40 MHz or over, change an access to the internal ROM to 3 cycle access (ROMMC[1:0]=10) by the internal ROM access control register (ROMCTR) before the PLLSEL flag of the PLL control register (PCNT) is switched "0" to "1".
The operation that is set to 2 cycle access is not guranteed.

4.2.3 Setup Example of Internal Clock

The frequency of the internal clock (MCLK and IOCLK) is determined by setting the PLL control register and the clock control register.

The following table shows the setting sequence when the oscillator of 10 MHz is connected and operated with 6 multiple by PLL.

Operation clock	Internal clock	
	After reset is released	After the setting
System clock (MCLK)	1/2 of oscillation frequency (5 MHz)	6 multiplication of oscillation frequency (60 MHz)
Peripheral clock (IOCLK)	1/4 of oscillation frequency (2.5 MHz)	3 multiplication of oscillation frequency (30 MHz)

Setup Procedure	Description
(1) Set the multiplication ratio PCNT (0x0000AFF2) bp5: PLLSEL=0 bp3: PLLON=0 bp1: CKSEL1=0 bp0: CKSEL0=1	(1) Set the PLL multiplication ratio to 6 by the CKSEL 1 and CKSEL0 of the PLL control register (PCNT). Note: Set the frequency (oscillation frequceny × multiplication ratio) to 40MHz≤PLLOUT≤60MHz
(2) Wait PLL lock time over 200 μs	(2) Wait 200 μs by the execution of the loop program etc.
(3) Select PLL output PCNT (0x0000AFF2) bp5: PLLSEL=1 bp3: PLLON=0 bp1: CKSEL1=0 bp0: CKSEL0=1	(3) Set the PLLSEL of the PLL control register (PCNT) to “1” to select the PLL output to the internal clock. Note: Do not change the values of PLLON, CKSEL1 and CKSEL0.
(4) Set the frequency of MCLK and IOCLK CKCTR (0x00008280) bp5: IOCLK1=1 bp3: IOCLK0=1 bp1: MCK1=1 bp0: MCK0=1	(4) Set the cycle division of MCLK and IOCLK. This setting is not necessary when MCLK=PLLOUT and IOCLK=1/2PLLOUT.

When the CPU clock (MCLK) is 40 MHz or over, change an access to the internal ROM to 3 cycle access (ROMMC[1:0]=10) by the internal ROM access control register (ROMCTR) before the PLLSEL flag of the PLL control register (PCNT) is switched "0" to "1".
The operation that is set to 2 cycle access is not guranteed.

When the PLLON and CKSEL [1:0] flags of the PCNT register are changed, reset the PLLSEL flag to “0” before the change and set to “1” after waiting over 200 μs.

Chapter 5 Interrupt Controller

5

5.1 Overview

The interrupt controllers are comprised of reset interrupts, non-maskable interrupts (NMI), 9 external interrupt pins, and 45 internal interrupts (peripheral function interrupts).

5.1.1 Functions

Table:5.1.1 Interrupt Functions

Interrupt type	Reset interrupt	Non-maskable interrupt	Level interrupt
Starting address	0x40000000	0x40000008	0x40000000+ interrupt Value of vector table
Interrupt level	-	-	Can be set levels from 0 to 6 by program
Interrupt factor count	1	2	9 (external pin input) 31 (internal peripheral function)
Interrupt factor	External RST pin input Software reset Power supply voltage detection reset	Watchdog timer overflow interrupt System error interrupt	External pin input, Interrupts by internal peripheral function
Generated (request) operation	Direct input to CPU core	Input to the CPU core from the NMICR register	Input the interrupt highest priority level to the CPU core by GnICR register.
Accept operation	Always accepts	Always accepts	Acceptance by the processor status register (PSW) and interrupt control register (GnICR).
Machine cycles until accepted	Refer to [11.3.1 Oscillation Stabilization Wait Operation]	Up to 14 cycles	Up to 14 cycles
PWM status after acceptance	All flags are cleared to “0”.	The interrupt mask level of PSW is cleared to “000”.	Values of the interrupt level flag are set to the interrupt mask level in PSW (masking all interrupt requests with the same or the lower priority)

5.1.2 Block Diagram

■ Block Diagram of Interrupt Controller

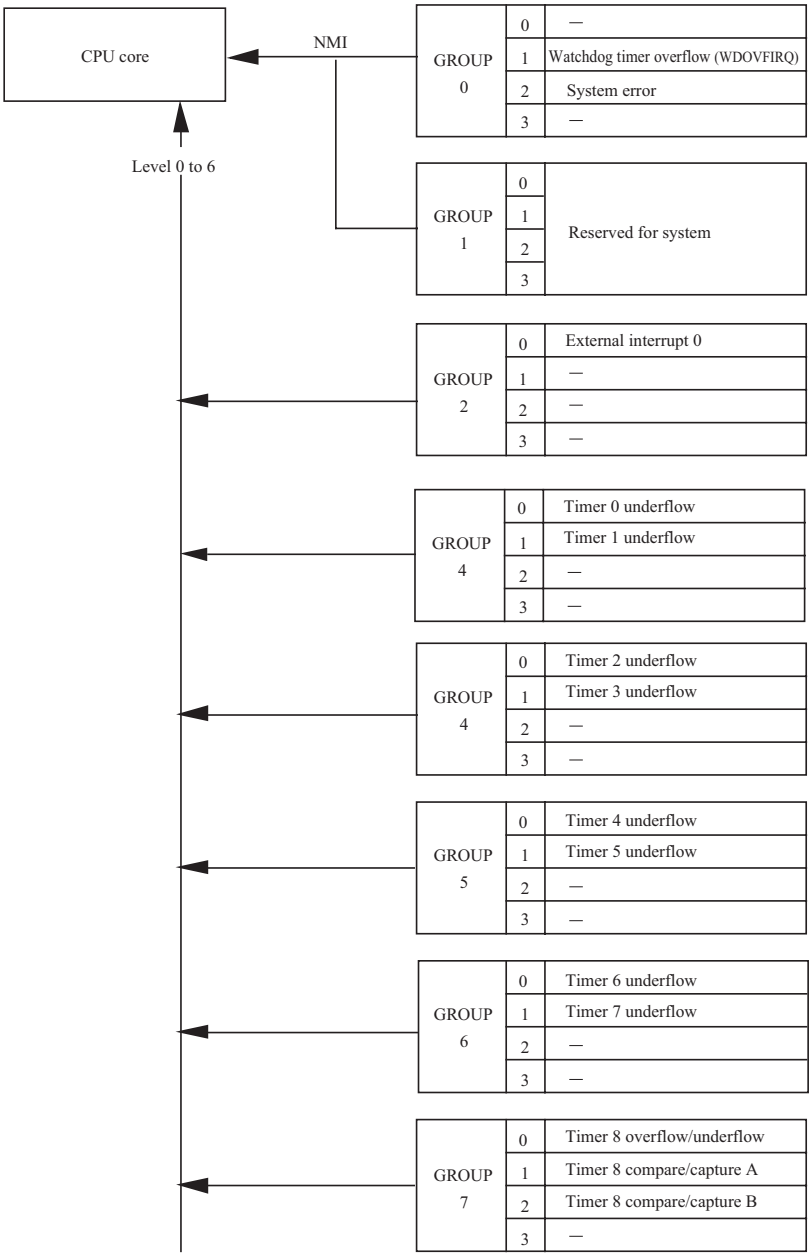


Figure:5.1.1 Block Diagram 1

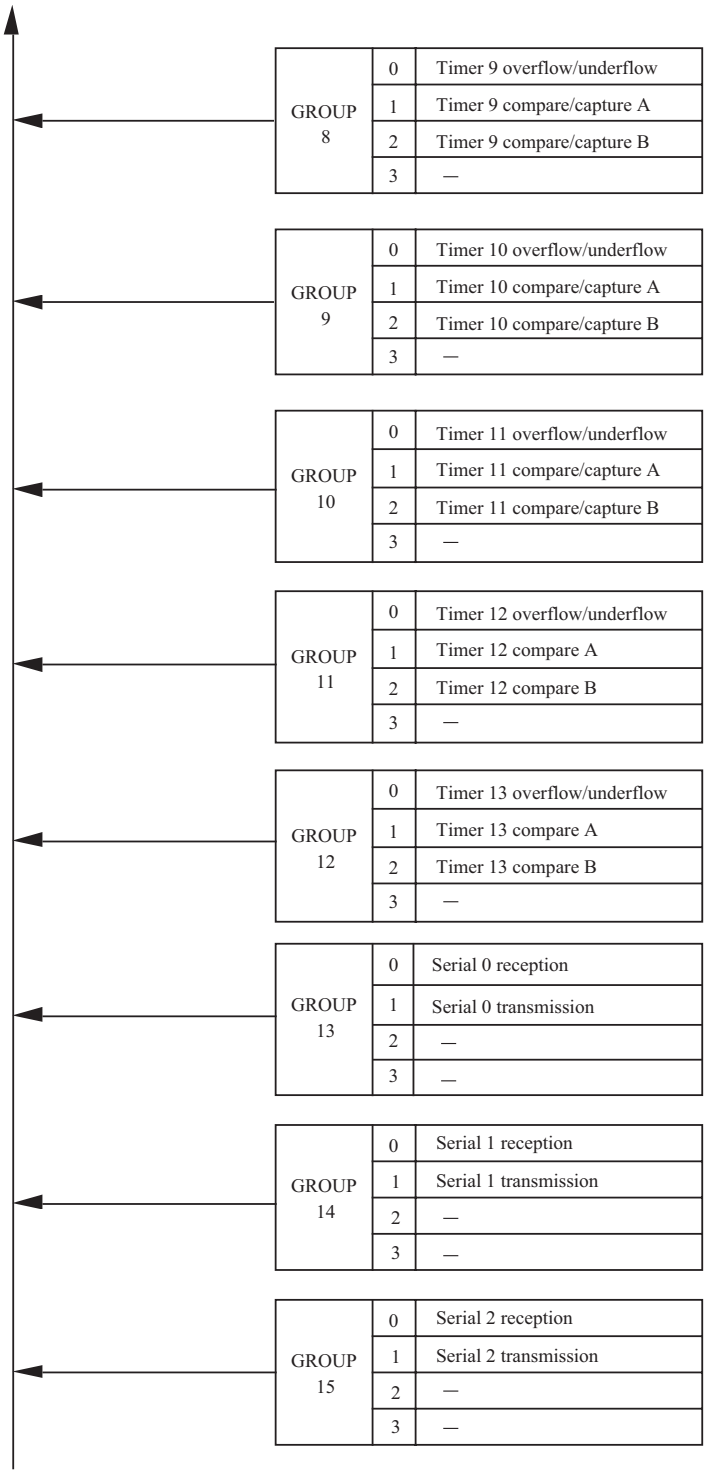


Figure:5.1.2 Block Diagram 2

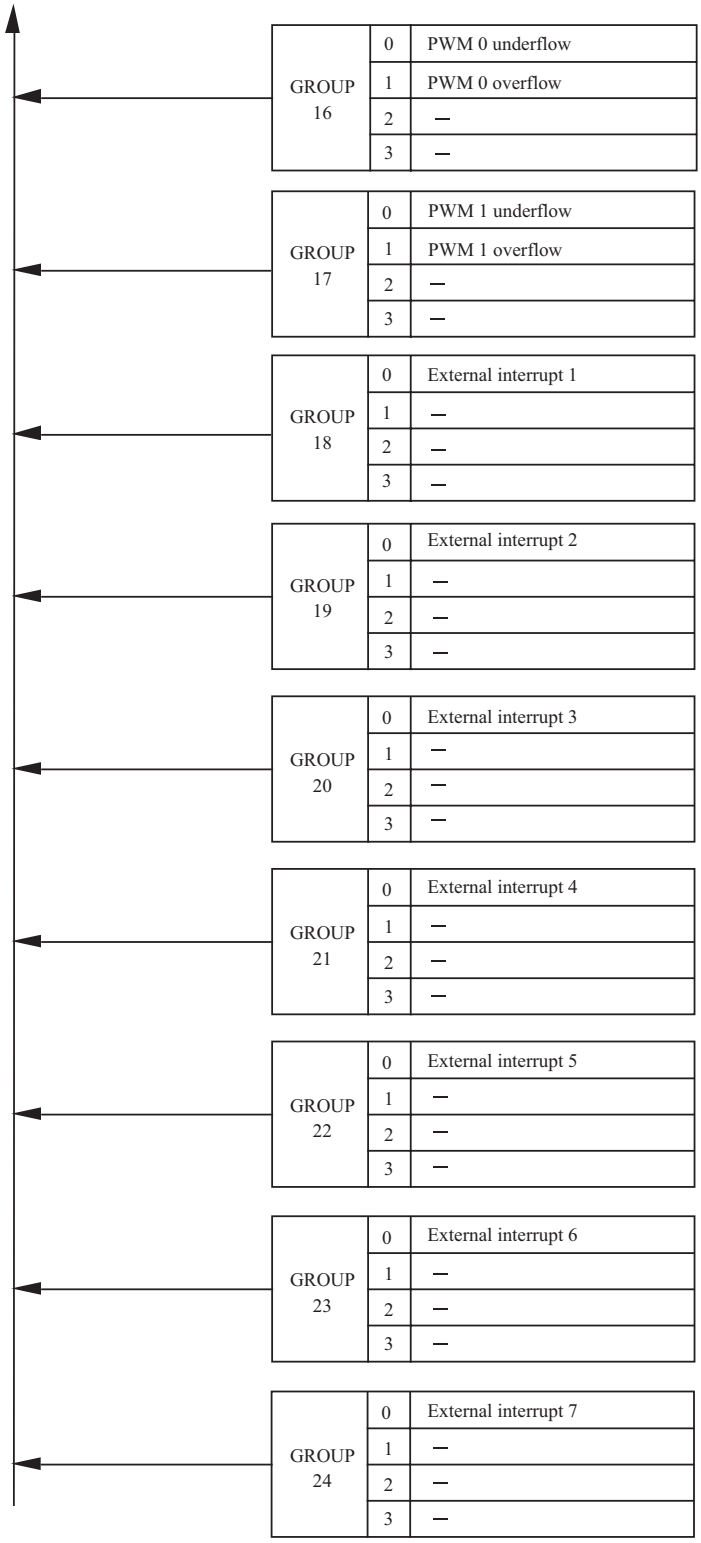


Figure:5.1.3 Block Diagram 3

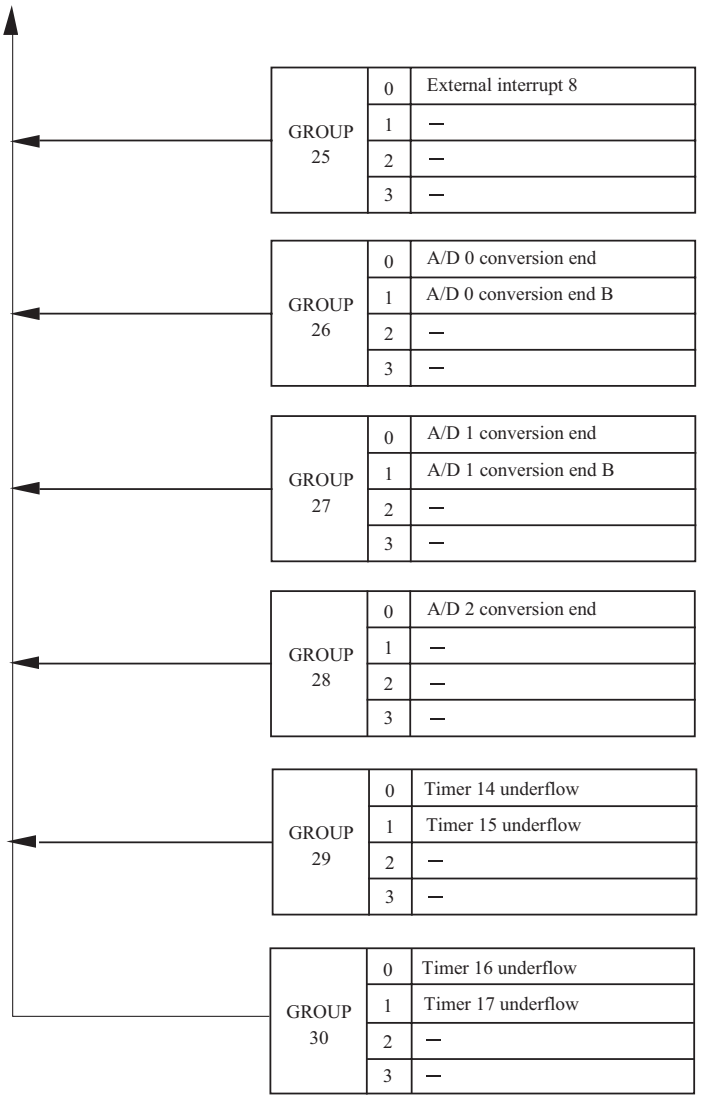


Figure:5.1.4 Block Diagram 4

5.2 Control Registers

The interrupt control registers are comprised of the processor status word (PSW), interrupt vector register, non-maskable control register, group interrupt control register, interrupt accepted group register and external interrupt condition specification register.

5.2.1 Registers List

Table: 5.2.1 shows the interrupt control registers.

Table:5.2.1 Interrupt Control Register List

	Register	Address	R/W	Access size	Functions	Page
CPU register	PSW	-	R/W	16	Processor status word	V-9
Interrupt vector register	IVAR0	0x00008000	R/W	16	Interrupt vector register 0	V-10
	IVAR1	0x00008004	R/W	16	Interrupt vector register 1	V-10
	IVAR2	0x00008008	R/W	16	Interrupt vector register 2	V-11
	IVAR3	0x0000800C	R/W	16	Interrupt vector register 3	V-11
	IVAR4	0x00008010	R/W	16	Interrupt vector register 4	V-11
	IVAR5	0x00008014	R/W	16	Interrupt vector register 5	V-11
	IVAR6	0x00008018	R/W	16	Interrupt vector register 6	V-11
Non-maskable interrupt›	G0ICR (NMICR)	0x00008900	R/W	8,16	Non-maskable interrupt control register	V-12

	Register	Address	R/W	Access size	Functions	Page
Maskable interrupt control	G2ICR	0x00008908	R/W	8,16	Group 2 interrupt control register	V-14
	G3ICR	0x0000890C	R/W	8,16	Group 3 interrupt control register	V-15
	G4ICR	0x00008910	R/W	8,16	Group 4 interrupt control register	V-15
	G5ICR	0x00008914	R/W	8,16	Group 5 interrupt control register	V-16
	G6ICR	0x00008918	R/W	8,16	Group 6 interrupt control register	V-17
	G7ICR	0x0000891C	R/W	8,16	Group 7 interrupt control register	V-18
	G8ICR	0x00008920	R/W	8,16	Group 8 interrupt control register	V-19
	G9ICR	0x00008924	R/W	8,16	Group 9 interrupt control register	V-20
	G10ICR	0x00008928	R/W	8,16	Group 10 interrupt control register	V-21
	G11ICR	0x0000892C	R/W	8,16	Group 11 interrupt control register	V-22
	G12ICR	0x00008930	R/W	8,16	Group 12 interrupt control register	V-22
	G13ICR	0x00008934	R/W	8,16	Group 13 interrupt control register	V-23
	G14ICR	0x00008938	R/W	8,16	Group 14 interrupt control register	V-24
	G15ICR	0x0000893C	R/W	8,16	Group 15 interrupt control register	V-25
	G16ICR	0x00008940	R/W	8,16	Group 16 interrupt control register	V-26
	G17ICR	0x00008944	R/W	8,16	Group 17 interrupt control register	V-27
	G18ICR	0x00008948	R/W	8,16	Group 18 interrupt control register	V-28
	G19ICR	0x0000894C	R/W	8,16	Group 19 interrupt control register	V-29
	G20ICR	0x00008950	R/W	8,16	Group 20 interrupt control register	V-30
	G21ICR	0x00008954	R/W	8,16	Group 21 interrupt control register	V-31
	G22ICR	0x00008958	R/W	8,16	Group 22 interrupt control register	V-32
	G23ICR	0x0000895C	R/W	8,16	Group 23 interrupt control register	V-33
	G24ICR	0x00008960	R/W	8,16	Group 24 interrupt control register	V-34
	G25ICR	0x00008964	R/W	8,16	Group 25 interrupt control register	V-34
	G26ICR	0x00008968	R/W	8,16	Group 26 interrupt control register	V-34
	G27ICR	0x0000896C	R/W	8,16	Group 27 interrupt control register	V-35
	G28ICR	0x00008970	R/W	8,16	Group 28 interrupt control register	V-36
	G29ICR	0x00008974	R/W	8,16	Group 29 interrupt control register	V-37
	G30ICR	0x00008978	R/W	8,16	Group 30 interrupt control register	V-37
Accepted group	IAGR	0x00008A00	R	8,16	Interrupt accepted group register	V-38
External interrupt condition specification	EXTMD0	0x00008A80	R/W	8,16	External interrupt condition specification register 0	V-39
	EXTMD1	0x00008A84	R/W	8,16	External interrupt condition specification register 1	V-40

R/W Readable / Writable
R Readable
W Writable

5.2.2 Processor Status Word

■ Processor Status Word

The interrupt enable flag and interrupt mask level flag are used as interrupt-related flags in the processor status word (PSW). These flags are read- and write-enabled flags. For information about the PSW, refer to [Chapter 2 CPU].

Table:5.2.2 Processor Status Word

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	S1	S0	IE	IM2	IM1	IM0	-	-	-	-	V	C	N	Z
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-12	-	-	Refer to[Chapter 2 CPU]
11	IE	Interrupt enable	0: disabled 1:enabled This flag allows all interrupts to be accepted except for reset interrupts and non-maskable interrupts. When an interrupt is accepted, IE flag is cleared to “0” (interrupt disabled). Set IE flag to “1” when accepting multiple interrupts within the interrupt processing program.
10-8	IM2 IM1 IM0	Interrupt mask level	Specifies the interrupt mask level. When IE flag is “1”, the CPU core accepts the interrupt with level higher than the mask level.
7-0	-	-	Refer to [Chapter 2 CPU]

Table: 5.2.3 shows the relationship between interrupt mask levels and acceptable interrupt levels.

Table:5.2.3 Relationship between Interrupt Mask Levels and Interrupt Levels that Can be Accepted

Interrupt mask level			Acceptable interrupt level
IM2	IM1	IM0	
0	0	0	Interrupt disabled (only non-maskable interrupts accepted.)
0	0	1	0
0	1	0	0 to 1
0	1	1	0 to 2
1	0	0	0 to 3
1	0	1	0 to 4
1	1	0	0 to 5
1	1	1	0 to 6

5.2.3 Interrupt Vector Register

The interrupt vector register is a register that stores the lower 16 bits of the starting address of the processing program for the accepted level interrupts. The starting addressees of level 0 to 6 of the level interrupts correspond to IVAR0 to IVAR 6. When an interrupt occurs, control is transferred from the upper 16 bits to"0x'4000" and from the lower 16 bits to the 32-bit address which is comprised of IVARn corresponding to the interrupt level.

Table:5.2.4 Interrupt Level and Interrupt Vector Register

Interrupt level	Interrupt vector register
0	IVAR0
1	IVAR1
2	IVAR2
3	IVAR3
4	IVAR4
5	IVAR5
6	IVAR6

■ Interrupt Vector Register 0 (IVAR0: 0x00008000) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 015	IVAR 014	IVAR 013	IVAR 012	IVAR 011	IVAR 010	IVAR 09	IVAR 08	IVAR 07	IVAR 06	IVAR 05	IVAR 04	IVAR 03	IVAR 02	IVAR 01	IVAR 00
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 1 (IVAR1: 0x00008004) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 115	IVAR 114	IVAR 113	IVAR 112	IVAR 111	IVAR 110	IVAR 19	IVAR 18	IVAR 17	IVAR 16	IVAR 15	IVAR 14	IVAR 13	IVAR 12	IVAR 11	IVAR 10
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 2 (IVAR2: 0x00008008) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 215	IVAR 214	IVAR 213	IVAR 212	IVAR 211	IVAR 210	IVAR 29	IVAR 28	IVAR 27	IVAR 26	IVAR 25	IVAR 24	IVAR 23	IVAR 22	IVAR 21	IVAR 20
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 3 (IVAR3: 0x0000800C) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 315	IVAR 314	IVAR 313	IVAR 312	IVAR 311	IVAR 310	IVAR 39	IVAR 38	IVAR 37	IVAR 36	IVAR 35	IVAR 34	IVAR 33	IVAR 32	IVAR 31	IVAR 30
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 4 (IVAR4: 0x00008010) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 415	IVAR 414	IVAR 413	IVAR 412	IVAR 411	IVAR 410	IVAR 49	IVAR 48	IVAR 47	IVAR 46	IVAR 45	IVAR 44	IVAR 43	IVAR 42	IVAR 41	IVAR 40
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 5 (IVAR5: 0x00008014) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 515	IVAR 514	IVAR 513	IVAR 512	IVAR 511	IVAR 510	IVAR 59	IVAR 58	IVAR 57	IVAR 56	IVAR 55	IVAR 54	IVAR 53	IVAR 52	IVAR 51	IVAR 50
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Interrupt Vector Register 6 (IVAR6: 0x00008018) [16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IVAR 615	IVAR 614	IVAR 613	IVAR 612	IVAR 611	IVAR 610	IVAR 69	IVAR 68	IVAR 67	IVAR 66	IVAR 65	IVAR 64	IVAR 63	IVAR 62	IVAR 61	IVAR 60
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.2.4 Non-Maskable Interrupt Control Register

If a NMI interrupt request is issued, The flag corresponding to the request is set. After the NMI interrupt request is accepted, the flag is cleared by software in the NMI interrupt processing program. When the flag is set to “1”, the flag can be cleared by writing “1”. Table: 5.2.5 shows the relationship between the flag status, the data written to the flag, and the flag status after the data is written.

Table:5.2.5 Changes of Interrupt Request Flags

Flag status before write	Write data	Flag status after write	Flag change
0	0	0	No change
0	1	0	No change
1	0	1	No change
1	1	0	Flag cleared

■ Non-maskable Interrupt Control Register (NMICR: 0x00008900) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	SYSEF	WDIF	-
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R

bp	Flag	Description	Set condition
15-3	-	-	-
2	SYSEF	System error interrupt request flag	0: No interrupt request 1: Interrupt request
1	WDIF	Watchdog timer overflow interrupt request flag	0: No interrupt request 1: Interrupt request
0	-	-	-

NMI cannot be generated by software.

5.2.5 Group n Interrupt Control Registers

G2ICR to G30ICR registers are designed to control the level interrupts for groups 2 to 30, respectively.

The interrupt priority level is controlled by the GnLV2 to GnLV0 flags. When the interrupt level set in the GnLV2 to GnLV0 flags is smaller than the IM2 to IM0 flags in the PSW, interrupts of the corresponding the interrupt group can be generated. Interrupts in the same interrupt group (max.4 interrupts) are the interrupt level specified by GnLV2 to GnLV0 flags. If interrupt requests are issued by multiple interrupt groups at the same time, the interrupt group with the highest interrupt priority level is accepted. In addition, if the interrupt priority levels of multiple interrupt groups are set to the same level, the interrupt from the interrupt group with the highest interrupt priority level (the interrupt group with the smallest group number) is accepted.

An interrupt is enabled by the GnIE flag. The bits of the GnIE flag correspond to the interrupt factors (max.4 factors) of the interrupt group. When the GnIE flag is “1”, the interrupt corresponding to this flag is enabled. When the GnIR flag is in “1” state and the GnIE flag is set to “1”, an interrupt is generated.

An interrupt request is controlled by the GnIR flag. The bits of the GnIR flag correspond to interrupts respectively. The GnIR flag is cleared by software in the interrupt processing program after the interrupt is accepted. When clearing the GnIR flag to “0”, set the GnIR flag to “0” and the corresponding GnID flag to “1”.

An interrupt detection is controlled by the GnID flag. The logical product of the GnIE and InIR flags is stored. If the interrupt enabled by the GnIE flag is generated, the GnID flag corresponding to the interrupt changes to “1”. It is used for specifying the interrupt factor of the group in the interrupt processing program. The interrupt request is released by writing the specified value on the GnIR and GnID flags and clearing the GnIR flag.

Table:5.2.6 Changes of the GnIR flag and GnID flag

Write data		Result of write	
GnIR	GnID	GnIR	GnID
0	0	No change	No change
0	1	0	0
1	0	No change	No change
1	1	1	IE value

All values except the IR and ID remain unchanged wring.

When using LV2 to 0 bits or IE3 to 0 bits in the group n interrupt control register (GnICR) to set the interrupt priority level or specify whether to enable interrupts, make sure that interrupts are disabled as indicated below.

```
and 0xf7ff,psw ; Clears IE in the PSW
nop        ;  Insert to guarantee that IE has been definitely cleared in the pipeline fashion
nop        ;
mov d0,(GnICR); Changes LV2 to 0 and IE3 to 0
mov (GnICR),d0; Inserted for synchronizing with the store buffer
or 0x0800,psw ; Set IE in the PSW
```

However, during the execution of the interrupt handler, IE in the PSW=0 unless it is set; therefore, it is not necessary to clear IE for disabling interrupts.
The nop instruction shown above can be any instructions provided that they do not change the IE in the PSW or change LV2 to 0 and IE3 to 0 in the GnICR.
In addition, the nop instruction is inserted twice to positively provide the “minimum” number of cycles required to change the IE in the PSW. Therefore, more than two nop instructions may be inserted.

■ Group 2 Interrupt Control Register (G2ICR: 0x00008908) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G2LV2	G2LV1	G2LV0	-	-	-	G2IE0	-	-	-	G2IR0	-	-	-	G2ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G2LV2 G2LV1 G2LV0	Set an interrupt priority level	Set a level from 6 to 0
11-9	-	-	-
8	G2IE0	External interrupt 0 enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G2IR0	External interrupt 0 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G2ID0	External interrupt 0 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 3 Interrupt Control Register (G3ICR: 0x0000890C) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G3LV2	G3LV1	G3LV0	-	-	G3IE1	G3IE0	-	-	G3IR1	G3IR0	-	-	G3ID1	G3ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G3LV2 G3LV1 G3LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G3IE1	Timer 1 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G3IE0	Timer 0 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G3IR1	Timer 1 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G3IR0	Timer 0 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G3ID1	Timer 1 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G3ID0	Timer 0 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 4 Interrupt Control Register (G4ICR: 0x00008910) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G4LV2	G4LV1	G4LV0	-	-	G4IE1	G4IE0	-	-	G4IR1	G4IR0	-	-	G4ID1	G4ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G4LV2 G4LV1 G4LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G4IE1	Timer 3 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G4IE0	Timer 2 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G4IR1	Timer 3 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G4IR0	Timer 2 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G4ID1	Timer 3 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G4ID0	Timer 2 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 5 Interrupt Control Register (G5ICR: 0x00008914) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G5LV2	G5LV1	G5LV0	-	-	G5IE1	G5IE0	-	-	G5IR1	G5IR0	-	-	G5ID1	G5ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G5LV2 G5LV1 G5LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G5IE1	Timer 5 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G5IE0	Timer 4 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G5IR1	Timer 5 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G5IR0	Timer 4 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G5ID1	Timer 5 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G5ID0	Timer 4 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 6 Interrupt Control Register (G6ICR: 0x00008918) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G6LV2	G6LV1	G6LV0	-	-	G6IE1	G6IE0	-	-	G6IR1	G6IR0	-	-	G6ID1	G6ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G6LV2 G6LV1 G6LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G6IE1	Timer 7 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G6IE0	Timer 6 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G6IR1	Timer 7 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G6IR0	Timer 6 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G6ID1	Timer 7 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G6ID0	Timer 6 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 7 Interrupt Control Register (G7ICR: 0x0000891C) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G7LV2	G7LV1	G7LV0	-	G7IE2	G7IE1	G7IE0	-	G7IR2	G7IR1	G7IR0	-	G7ID2	G7ID1	G7ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G7LV2 G7LV1 G7LV0	Set an interrupt priority level	Set a level from 6 to 0
11	-	-	-
10	G7IE2	Timer 8 compare/capture B interrupt enable flag	0: Disabled 1: Enabled
9	G7IE1	Timer 8 compare/capture A interrupt enable flag	0: Disabled 1: Enabled
8	G7IE0	Timer 8 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G7IR2	Timer 8 compare/capture B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G7IR1	Timer 8 compare/capture A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G7IR0	Timer 8 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	-	-
2	G7ID2	Timer 8 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G7ID1	Timer 8 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G7ID0	Timer 8 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 8 Interrupt Control Register (G8ICR: 0x00008920) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G8LV2	G8LV1	G8LV0	-	G8IE2	G8IE1	G8IE0	-	G8IR2	G8IR1	G8IR0	-	G8ID2	G8ID1	G8ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G8LV2 G8LV1 G8LV0	Set an interrupt priority level	Set a level 6 to 0
11	-	-	-
10	G8IE2	Timer 9 compare/capture B interrupt enable flag	0: Disabled 1: Enabled
9	G8IE1	Timer 9 compare/capture A interrupt enable flag	0: Disabled 1: Enabled
8	G8IE0	Timer 9 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G8IR2	Timer 9 compare/capture B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G8IR1	Timer 9 compare/capture A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G8IR0	Timer 9 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	Å-	-
2	G8ID2	Timer 9 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G8ID1	Timer 9 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G8ID0	Timer 9 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 9 Interrupt Control Register (G9ICR: 0x00008924) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G9LV2	G9LV1	G9LV0	-	G9IE2	G9IE1	G9IE0	-	G9IR2	G9IR1	G9IR0	-	G9ID2	G9ID1	G9ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G9LV2 G9LV1 G9LV0	Set an interrupt priority level	Set a level 6 to 0
11	-	-	-
10	G9IE2	Timer 10 compare/capture B interrupt enable flag	0: Disabled 1: Enabled
9	G9IE1	Timer 10 compare/capture A interrupt enable flag	0: Disabled 1: Enabled
8	G9IE0	Timer 10 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G9IR2	Timer 10 compare/capture B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G9IR1	Timer 10 compare/capture A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G9IR0	Timer 10 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	-	-
2	G9ID2	Timer 10 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G9ID1	Timer 10 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G9ID0	Timer 10 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 10 Interrupt Control Register (G10ICR: 0x00008928) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G10 LV2	G10 LV1	G10 LV0	-	G10 IE2	G10 IE1	G10 IE0	-	G10 IR2	G10 IR1	G10 IR0	-	G10 ID2	G10 ID1	G10 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G10LV2 G10LV1 G10LV0	Set an interrupt priority level	Set a level 6 to 0
11	-	-	-
10	G10IE2	Timer 11 compare/capture B interrupt enable flag	0: Disabled 1: Enabled
9	G10IE1	Timer 11 compare/capture A interrupt enable flag	0: Disabled 1: Enabled
8	G10IE0	Timer 11 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G10IR2	Timer 11 compare/capture B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G10IR1	Timer 11 compare/capture A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G10IR0	Timer 11 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	-	-
2	G10ID2	Timer 11 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G10ID1	Timer 11 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G10ID0	Timer 11 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 11 Interrupt Control Register (G11ICR: 0x0000892C) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G11 LV2	G11 LV1	G11 LV0	-	G11 IE2	G11 IE1	G11 IE0	-	G11 IR2	G11 IR1	G11 IR0	-	G11 ID2	G11 ID1	G11 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G11LV2 G11LV1 G11LV0	Set an interrupt priority level	Set a level 6 to 0
11	-	-	-
10	G11IE2	Timer 12 compare B interrupt enable flag	0: Disabled 1: Enabled
9	G11IE1	Timer 12 compare A interrupt enable flag	0: Disabled 1: Enabled
8	G11IE0	Timer 12 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G11IR2	Timer 12 compare B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G11IR1	Timer 12 compare A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G11IR0	Timer 12 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	-	-
2	G11ID2	Timer 12 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G11ID1	Timer 12 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G11ID0	Timer 12 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 12 Interrupt Control Register (G12ICR: 0x00008930) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G12 LV2	G12 LV1	G12 LV0	-	G12 IE2	G12 IE1	G12 IE0	-	G12 IR2	G12 IR1	G12 IR0	-	G12 ID2	G12 ID1	G12 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G12LV2 G12LV1 G12LV0	Set an interrupt priority level	Set a level 6 to 0
11	-	-	-
10	G12IE2	Timer 13 compare B interrupt enable flag	0: Disabled 1: Enabled
9	G12IE1	Timer 13 compare A interrupt enable flag	0: Disabled 1: Enabled
8	G12IE0	Timer 13 overflow/underflow interrupt enable flag	0: Disabled 1: Enabled
7	-	-	-
6	G12IR2	Timer 13 compare B interrupt request flag	0: No interrupt request 1: Interrupt request
5	G12IR1	Timer 13 compare A interrupt request flag	0: No interrupt request 1: Interrupt request
4	G12IR0	Timer 13 overflow/underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3	-	-	-
2	G12ID2	Timer 13 compare/capture B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
1	G12ID1	Timer 13 compare/capture A interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G12ID0	Timer 13 overflow/underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 13 Interrupt Control Register (G13ICR: 0x00008934) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G13 LV2	G13 LV1	G13 LV0	-	-	G13 IE1	G13 IE0	-	-	G13 IR1	G13 IR0	-	-	G13 ID1	G13 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G13LV2 G13LV1 G13LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G13IE1	Serial 0 transmission interrupt enable flag	0: Disabled 1: Enabled
8	G13IE0	Serial 0 reception interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G13IR1	Serial 0 transmission interrupt request flag	0: No interrupt request 1: Interrupt request
4	G13IR0	Serial 0 reception interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G13ID1	Serial 0 transmission interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G13ID0	Serial 0 reception interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 14 Interrupt Control Register (G14ICR: 0x00008938) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G14 LV2	G14 LV1	G14 LV0	-	-	G14 IE1	G14 IE0	-	-	G14 IR1	G14 IR0	-	-	G14 ID1	G14 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G14LV2 G14LV1 G14LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G14IE1	Serial 1 transmission interrupt enable flag	0: Disabled 1: Enabled
8	G14IE0	Serial 1 reception interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G14IR1	Serial 1 transmission interrupt request flag	0: No interrupt request 1: Interrupt request
4	G14IR0	Serial 1 reception interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G14ID1	Serial 1 transmission interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G14ID0	Serial 1 reception interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 15 Interrupt Control Register (G15ICR: 0x0000893C) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G15 LV2	G15 LV1	G15 LV0	-	-	G15 IE1	G15 IE0	-	-	G15 IR1	G15 IR0	-	-	G15 ID1	G15 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G15LV2 G15LV1 G15LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G15IE1	Serial 2 transmission interrupt enable flag	0: Disabled 1: Enabled
8	G15IE0	Serial 2 reception interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G15IR1	Serial 2 transmission interrupt request flag	0: No interrupt request 1: Interrupt request
4	G15IR0	Serial 2 reception interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G15ID1	Serial 2 transmission interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G15ID0	Serial 2 reception interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 16 Interrupt Control Register (G16ICR: 0x00008940) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G16 LV2	G16 LV1	G16 LV0	-	-	G16 IE1	G16 IE0	-	-	G16 IR1	G16 IR0	-	-	G16 ID1	G16 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G16LV2 G16LV1 G16LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G16IE1	PWM0 binary counter overflow interrupt enable flag	0: Disabled 1: Enabled
8	G16IE0	PWM0 binary counter underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G16IR1	PWM0 binary counter overflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G16IR0	PWM0 binary counter underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G16ID1	PWM0 binary counter overflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G16ID0	PWM0 binary counter underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 17 Interrupt Control Register (G17ICR: 0x00008944) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G17 LV2	G17 LV1	G17 LV0	-	-	G17 IE1	G17 IE0	-	-	G17 IR1	G17 IR0	-	-	G17 ID1	G17 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G17LV2 G17LV1 G17LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G17IE1	PWM1 binary counter overflow interrupt enable flag	0: Disabled 1: Enabled
8	G17IE0	PWM1 binary counter underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G17IR1	PWM1 binary counter overflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G17IR0	PWM1 binary counter underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G17ID1	PWM1 binary counter overflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G17ID0	PWM1 binary counter underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 18 Interrupt Control Register (G18ICR: 0x00008948) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G18 LV2	G18 LV1	G18 LV0	-	-	-	G18 IE0	-	-	-	G18 IR0	-	-	-	G18 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G18LV2 G18LV1 G18LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G18IE0	External interrupt 1 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G18IR0	External interrupt 1 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G18ID0	External interrupt 1 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 19 Interrupt Control Register (G19ICR: 0x0000894C) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G19 LV2	G19 LV1	G19 LV0	-	-	-	G19 IE0	-	-	-	G19 IR0	-	-	-	G19 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G19LV2 G19LV1 G19LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G19IE0	External interrupt 2 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G19IR0	External interrupt 2 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G19ID0	External interrupt 2 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 20 Interrupt Control Register (G20ICR: 0x00008950) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G20 LV2	G20 LV1	G20 LV0	-	-	-	G20 IE0	-	-	-	G20 IR0	-	-	-	G20 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G20LV2 G20LV1 G20LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G20IE0	External interrupt 3 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G20IR0	External interrupt 3 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G20ID0	External interrupt 3 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 21 Interrupt Control Register (G21ICR: 0x00008954) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G21 LV2	G21 LV1	G21 LV0	-	-	-	G21 IE0	-	-	-	G21 IR0	-	-	-	G21 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G21LV2 G21LV1 G21LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G21IE0	External interrupt 4 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G21IR0	External interrupt 4 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G21ID0	External interrupt 4 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 22 Interrupt Control Register (G22ICR: 0x00008958) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G22 LV2	G22 LV1	G22 LV0	-	-	-	G22 IE0	-	-	-	G22 IR0	-	-	-	G22 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G22LV2 G22LV1 G22LV0	Set an internal priority level	Set a level 6 to 0
11-9	-	-	-
8	G22IE0	External interrupt 5 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G22IR0	External interrupt 5 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G22ID0	External interrupt 5 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 23 Interrupt Control Register (G23ICR: 0x0000895C) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G23 LV2	G23 LV1	G23 LV0	-	-	-	G23 IE0	-	-	-	G23 IR0	-	-	-	G23 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G23LV2 G23LV1 G23LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G23IE0	External interrupt 6 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G23IR0	External interrupt 6 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G23ID0	External interrupt 6 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 24 Interrupt Control Register (G24ICR: 0x00008960) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G24 LV2	G24 LV1	G24 LV0	-	-	-	G24 IE0	-	-	-	G24 IR0	-	-	-	G24 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G24LV2 G24LV1 G24LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G24IE0	External interrupt 7 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G24IR0	External interrupt 7 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G24ID0	External interrupt 7 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 25 Interrupt Control Register (G25ICR: 0x00008964) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G25 LV2	G25 LV1	G25 LV0	-	-	-	G25 IE0	-	-	-	G25 IR0	-	-	-	G25 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G25LV2 G25LV1 G25LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G25IE0	External interrupt 8 interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G25IR0	External interrupt 8 interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G25ID0	External interrupt 8 interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 26 Interrupt Control Register (G26ICR: 0x00008968) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G26 LV2	G26 LV1	G26 LV0	-	-	G26 IE1	G26 IE0	-	-	G26 IR1	G26 IR0	-	-	G26 ID1	G26 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G26LV2 G26LV1 G26LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G26IE1	A/D0 conversion complete B interrupt enable flag	0: Disabled 1: Enabled
8	G26IE0	A/D0 conversion complete interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G26IR1	A/D0 conversion complete B interrupt request flag	0: No interrupt request 1: Interrupt request
4	G26IR0	A/D0 conversion complete interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G26ID1	A/D0 conversion complete B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G26ID0	A/D0 conversion complete interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 27 Interrupt Control Register (G27ICR: 0x0000896C) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G27 LV2	G27 LV1	G27 LV0	-	-	G27 IE1	G27 IE0	-	-	G27 IR1	G27 IR0	-	-	G27 ID1	G27 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G27LV2 G27LV1 G27LV0	Set an interrupt priority level	Set a level 6 to 0
11-10	-	-	-
9	G27IE1	A/D1 conversion complete B interrupt enable flag	0: Disabled 1: Enabled
8	G27IE0	A/D1 conversion complete interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G27IR1	A/D1 conversion complete B interrupt request flag	0: No interrupt request 1: Interrupt request
4	G27IR0	A/D1 conversion complete interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G27ID1	A/D1 conversion complete B interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G27ID0	A/D1 conversion complete interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 28 Interrupt Control Register (G28ICR: 0x00008970) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G28 LV2	G28 LV1	G28 LV0	-	-	-	G28 IE0	-	-	-	G28 IR0	-	-	-	G28 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G28LV2 G28LV1 G28LV0	Set an interrupt priority level	Set a level 6 to 0
11-9	-	-	-
8	G28IE0	A/D2 conversion complete interrupt enable flag	0: Disabled 1: Enabled
7-5	-	-	-
4	G28IR0	A/D2 conversion complete interrupt request flag	0: No interrupt request 1: Interrupt request
3-1	-	-	-
0	G28ID0	AD2 conversion complete interrupt detection flag	0: No interrupt detected 1: Interrupt request

■ Group 29 Interrupt Control Register (G29ICR: 0x00008974) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G29 LV2	G29 LV1	G29 LV0	-	-	G29 IE1	G29 IE0	-	-	G29 IR1	G29 IR0	-	-	G29 ID1	G29 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G29LV2 G29LV1 G29LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G29IE1	Timer 15 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G29IE0	Timer14 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G29IR1	Timer 15 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G29IR0	Timer 14 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G29ID1	Timer 15 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G29ID0	Timer 14 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

■ Group 30 Interrupt Control Register (G30ICR: 0x00008978) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	G30 LV2	G30 LV1	G30 LV0	-	-	G30 IE1	G30 IE0	-	-	G30 IR1	G30 IR0	-	-	G30 ID1	G30 ID0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Set condition
15	-	-	-
14-12	G30LV2 G30LV1 G30LV0	Set an interrupt priority level	Set a level from 6 to 0
11-10	-	-	-
9	G30IE1	Timer 17 underflow interrupt enable flag	0: Disabled 1: Enabled
8	G30IE0	Timer16 underflow interrupt enable flag	0: Disabled 1: Enabled
7-6	-	-	-
5	G30IR1	Timer 17 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
4	G30IR0	Timer 16 underflow interrupt request flag	0: No interrupt request 1: Interrupt request
3-2	-	-	-
1	G30ID1	Timer 17 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected
0	G30ID0	Timer 16 underflow interrupt detection flag	0: No interrupt detected 1: Interrupt detected

5.2.6 Interrupt Accepted Group Register

During a register read, the interrupt accepted group register (IAGR) returns the smallest group number of the groups generating the interrupt levels accepted by the CPU, specified by IM2 to IM0 of the PSW. The GN4 to GN0 flag corresponds to the interrupt group number. A branch destination of the interrupt program for each group can be found , for example, by referencing the contents of the address obtained by adding the interrupt accept group register value to the leading address of the interrupt vector table. If IM2 to IM0 of the PSW are changed, if the interrupt control register is manipulated or if a new interrupt cause is generated, the value returned by this register may change even during interrupt processing. The IAGR register is a read-only register and can not be written. When there are no interrupt factors of the appropriate interrupt level, IAGR returns “0x0000”. Accessing the IAGR register is meaningless during a NMI interrupt.

■ Interrupt Accepted Group Register (IAGR: 0x00008A00) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	GN4	GN3	GN2	GN1	GN0	-	-
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
15-7	-	-	-
6-2	GN4 GN3 GN2 GN1 GN0	Group number register	The accepted group number is indicated.
1-0	-	-	-

5.2.7 External Interrupt Condition Specification Register

This register specifies the external interrupt generation conditions.

■ External Interrupt Condition Specification Register 0 (EXTMDO: 0x00008A80) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	IR7 TG1	IR7 TG0	IR6 TG1	IR6 TG0	IR5 TG1	IR5 TG0	IR4 TG1	IR4 TG0	IR3 TG1	IR3 TG0	IR2 TG1	IR2 TG0	IR1 TG1	IR1 TG0	IR0 TG1	IR0 TG0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-14	IR7TG1 IR7TG0	IRQ7 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
13-12	IR6TG1 IR6TG0	IRQ6 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
11-10	IR5TG1 IR5TG0	IRQ5 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
9-8	IR4TG1 IR4TG0	IRQ4 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
7-6	IR3TG1 IR3TG0	IRQ3 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
5-4	IR2TG1 IR2TG0	IRQ2 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
3-2	IR1TG1 IR1TG0	IRQ1 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level
1-0	IR0TG1 IR0TG0	IRQ0 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level

■ External Interrupt Condition Specification Register 1 (EXTMD1: 0x00008A84) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	IR8 TG1	IR8 TG0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

bp	Flag	Description	Set condition
15-2	-	-	-
1-0	IR8TG1 IR8TG0	IRQ8 pin trigger condition setting	00: Rising edge 01: Falling edge 10: “H” level 11: “L” level

Refer to [5.4.6 Edge Detection Registers] for setting the external interrupt generation condition to both-edge detection.

5.3 Interrupt Controller Operation

5.3.1 Interrupt Types

■ Reset Interrupts

Reset interrupts are interrupts with the highest priority level, and are generated by setting the NRST pin to “L” or writing the CHIPRST flag of the reset control register from “0” to “1”. Registers are initialized by the reset interrupt, and a program is executed from 0’x40000000 address. Refer to [2.7.2 Reset Mode] for further details.

■ Non-maskable Interrupts

Non-maskable interrupts accept interrupts regardless of the values of the PSW interrupt enable flag (IE) and interrupt mask level IM2 to IM0. When the non-maskable interrupt is accepted, it branches to the interrupt processing program located at the addressees from 0x40000009~0x4003FFFF. After accessing the NMICR register to analyze the interrupt factor, perform the interrupt processing and cancel the interrupt factor, the interrupt processing program returns to the normal program by the RTI instruction.

Non-maskable interrupts have watchdog timer overflow interrupts and system error interrupts.

Watchdog timer overflow interrupt occur when the WDCNE flag in the watchdog timer control register (WDCTR) is “1” and the watchdog timer overflows. When the watchdog timer interrupt generates, the watchdog timer overflow interrupt request flag (WDIF) of the non-maskable interrupt control register (NMICR) is set to “1”.

System error interrupt occur when an unmounted instruction is executed or other fatal error occurs. When the system error interrupt generates, the system error interrupt request flag (SYSEF) of the NMICR register is set to “1”.

Interrupt Condition Register(ISR:0x00008034) is available for development of OS and debugging.

■ Level Interrupts

Level interrupts are interrupts that can control the interrupt level through the interrupt enable flag (IE) of the PSW and interrupt mask level (IM2 to IM0). The Level interrupts are interrupts from the interrupt group controllers external to the CPU core (in other word, peripheral interrupts), and correspond the groups and factors indicated in block diagrams (Figure 5.1.1 to 5.1.4). Each interrupt group controller includes an interrupt control register (GnICR); and, the interrupt priority level can be set per interrupt group. It is also possible to set the same interrupt priority level in the interrupt groups. If interrupts of the same priority level are generated simultaneously, the interrupts are accepted in the order of priority set by hardware (the group with the smallest group number takes the highest priority).

When the level interrupt is accepted, the upper 16 bits branch to “x’4000” and the lower 16 bits branch to the address of the interrupt vector address register (IVARn) corresponding to the interrupt level by hardware. After the interrupt processing program accesses the IAGR register to analyze the interrupt group and the GnICR register to analyze the interrupt factor, perform the interrupt processing and cancel the interrupt factor, it returns to the normal program by the RTI instruction.

5.3.2 Interrupt Controller Operation

When the CPU accepts an interrupt, first the sequence automatically processed by hardware is executed; then, the interrupt handler processing is processed by software, and the interrupt processing program starts up. The interrupt processing sequence is described below.

■ Interrupt Sequence (Interrupt Processing by Hardware)

Step	Process
1	PC (return address) is saved onto the stack. (SP-4)
2	The contents of PSW are saved onto the stack. (SP-8)
3	The contents of PSW are updated. IE is cleared and the accepted interrupt level is set in IM2 to IM0. (IM2 to IM0 are undefined during NMI.)
4	The contents of a stack pointer is updated. (SP-8 →SP)
5	A program branches to the address corresponding to the accepted interrupt factor or the address comprised of the interrupt vector address register (IVARn).

When an interrupt (except a reset interrupt) is accepted, a program branches to the address corresponding to the interrupt factor or the address comprised of the interrupt vector address register. The processing listed below is performed at the branch destination in order to judge the interrupt factor in further details.

■ Interrupt Sequence (Interrupt Processing by Interrupt Handler)

	Step	Process
Pre-processing	1	The contents of registers are saved. The registers are those used by the interrupt handler.
	2	The interrupt group analysis is executed.
	2-1	The interrupt acknowledge sequence is executed. Interrupt acknowledge is to read out the interrupt accept group register (IAGR) in order to obtain the group number of the interrupt group with the highest priority among the specified interrupt levels.
	2-2	The leading address of the interrupt processing program for each level is created.
	2-3	A program branches to the interrupt processing program for each level.
	3	When there are multiple factors within the same group, the interrupt control register (GnICR) is read out to specify the factor. During NMI, the factor is specified by accessing the G0ICR (NMICR) directly without accessing the IAGR.
	4	A program branches to the interrupt processing program for each factor. In addition, the store buffer is used when writing data by the bus controller; therefore, when releasing the interrupt factor, read the corresponding register immediately after the factor of the GnICR is cleared to wait the factor cleared.
Interrupt processing		Interrupt processing program is executed.
Post-processing	5	The contents of the registers are restored. The restored registers are those saved by the pre-processing.
	6	The RTI instruction is executed and a program returns to the program before the interrupt.

Figure: 5.3.1 shows the interrupt sequence flow. (when not accepting multiple interrupts) The numbers in the figure correspond to the steps in the previous list.

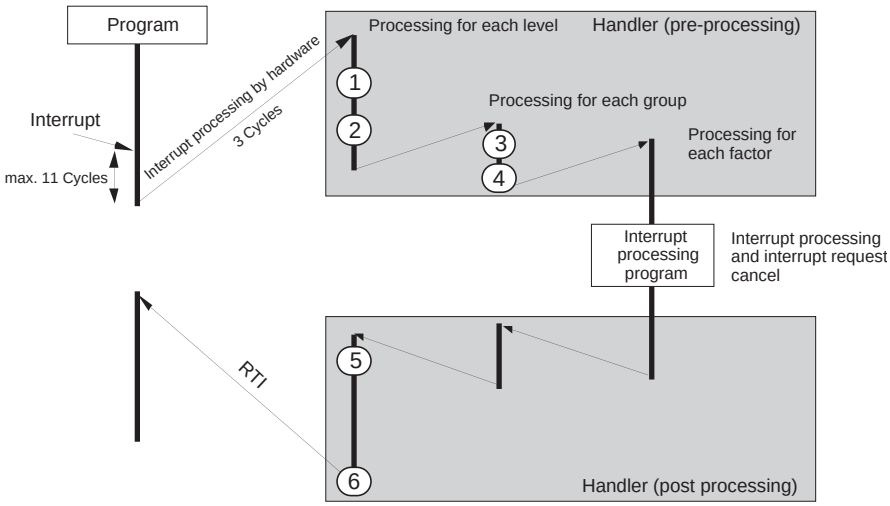


Figure:5.3.1 Interrupt Sequence (Interrupt Sequence by the Interrupt Handler)

■ Speed-up of the Interrupt Handler Processing

An even higher interrupt response speed can be realized by assigning only one factor to a single interrupt level. Figure: 5.3.2 shows the interrupt sequence flow when assigning one factor to a single interrupt level.

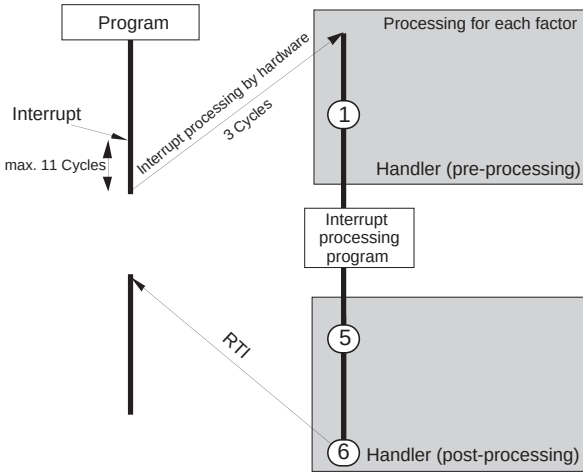


Figure:5.3.2 Speed-up of the Interrupt Handler Processing

■ Multiple Interrupts

When a level interrupt occurs, multiple interrupts are disabled by clearing IE of the PSW. However, multiple interrupts can be achieved even while processing level interrupts by setting IE to “1” during processing. However, in order for multiple interrupts to occur, the interrupts must have a higher priority than interrupt musk level IM2 to IM0 of the PSW at that time. (The GnICR interrupt level LV2 to LV0 is smaller than the PSW interrupt mask level IM2 to IM0.) When non-maskable interrupts occur, multiple interrupts of level interrupts and non-maskable interrupts are disabled until the non-maskable interrupt processing program is finished by the execution of the RTI instruction.

■ Interrupt Acceptance Timing

If an interrupt request occurs part-way through the execution of an instruction, even instructions which require multiple execution cycles such as multiply/divide and other instructions are aborted if possible and the interrupt is accepted. The aborted instruction is executed again after returning from interrupt processing. Aborting these instructions sets the interrupt acceptance prohibited interval to 11 cycles or less.(The maximum interrupt prohibited interval of 11 cycles occurs when saving or restoring all registers with the MOVM, CALL, or RET instructions. This occurs only for special cases such as task context switching.)

■ Stack Frame

When an interrupt is accepted, a stack flame is allocated and the total 6 bytes of information in the PC and PSW are saved in order to return form the interrupt. However, since transferring data across the 32-bit boundary is prohibited, the SP value must constantly be set to a multiple of 4. Accordingly, a stack flame is allocated as shown in Figure: 5.3.3 so that the SP value is constantly set to a multiple of 4. Ultimately, an 8-byte area with a total of 6 bytes of information is saved.

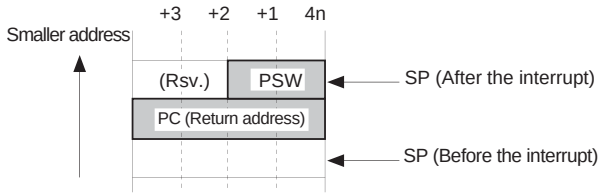


Figure:5.3.3 Stack Flame Configuration

5.3.3 Interrupt Controller Setup

■ Interrupt Flag Setup Procedure

The following shows the setup procedure of the interrupt flag including the software change of the interrupt request flag.

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp11: IE = 0	(1) Clear the IE flag of the PSW to “0” to disable all maskable interrupts.
(2) Select the interrupt factor	(2) Select the interrupt factor such as timer interrupt cycle change.
(3) Clear the interrupt request flag and the interrupt detection flag. GnICR IR of the interrupt factor = 0 ID of the interrupt factor = 1	(3) Change the IR flag corresponding to the interrupt factor of the group n interrupt control register (GnICR) to “0” and the ID flag to “1” simultaneously. By changing these flags simultaneously, the IR flag of the request flag and the ID flag of the detection flag are cleared to “0”.
(4) Set the interrupt level GnICR bp14-12: GnLV2-0	(4) Set the interrupt level by the GnLV2-0 flag of the GnICR register.
(5) Enable the interrupt. GnICR IE of the interrupt factor = 1	(5) Set the IE flag corresponding to the interrupt factor of the GnICR to “1” to enable the interrupt.

Setup Procedure	Description
(6) Enable all maskable interrupts. PSW bp11: IE = 1	(6) Set the IE flag of PSW to “1” to enable maskable interrupts.

5.3.4 Cautions for Programming

■ External Interrupt Request Signal

Maintain the external pin of the interrupt request signal for a minimum of 3 cycles of a system clock (MCLK). The level detection can not be achieved if the signal is not maintained for at least that long.

■ When the GnICR register is changed

Clear the IE flag of the PSW to “0” to change the GnICR.

■ Processing in Interrupt program

When the GnIR and GnID flags of the GnICR register are cleared and restored from the interrupt program, write the instruction for the I/O bus access between the clear processing instruction (movhu etc.,) of the GnICR register and the restore instruction to synchronize with the store buffer of the bus controller.

```
mov     0x0f:b,d0     d0=clear data
movbu   d0,(GnICR)    GnIR and GnID flags of the GnICR register
movhu   (GnICR),d1    I/O bus access
rti                   Restore instruction
```

When there is no instruction for the I/O bus access, the restore operation from the interrupt is not guaranteed. When the restore instruction is written right after the clear processing instruction of the GnICR register, a mal-function that the interrupt program is executed occurs.

```
mov     0x0f:b,d0     d0=clear data
movbu   d0,(GnICR)    Clear the GnIR and GnID flag of the GnICR register
rti                   Restore instruction
```

5.4 Noise Filter Function

This LSI incorporates noise filters for external interrupt pins. The noise filter control register can be used to select whether to enable or disable noise filters and sampling frequency. The sampling frequency can be selected from 1/4, 1/8, 1/16, and 1/32 of IOCLK.

5.4.1 Noise Filter Function List

Table:5.4.1 Noise Filter Function List

Operation condition	Description
Noise filter	enable/disable
Sampling frequency	IOCLK x 1/4 IOCLK x 1/8 IOCLK x 1/16 IOCLK x 1/32

5.4.2 Noise Filter Block Diagram

■ Noise Filter Block Diagram

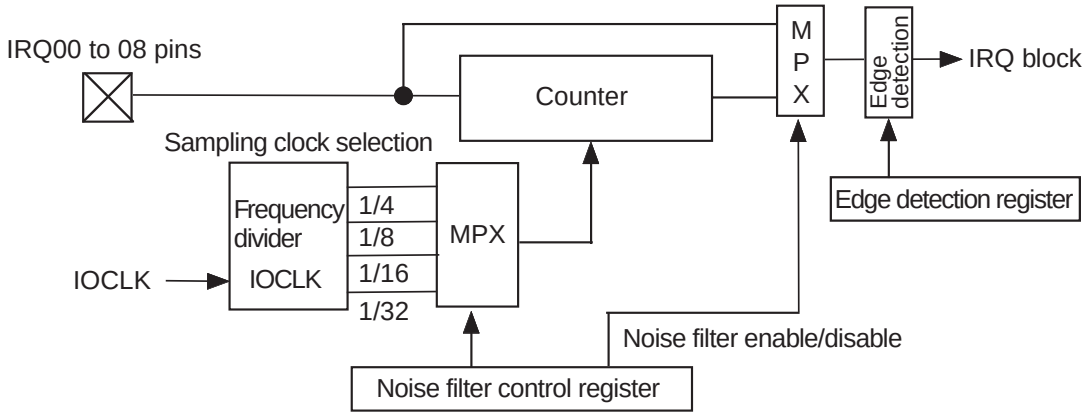


Figure:5.4.1 Noise Filter Block Diagram

5.4.3 Noise Filter Control Registers List

Table; 5.4.2 shows the registers that control the noise filter.

Table:5.4.2 Noise Filter Control Registers List

	Register	Address	R/W	Access size	Name	Page
Noise filter	NFCLK0	0x0000A050	R/W	8,16	Sampling clock setting register 0	V-42
	NFCLK1	0x0000A052	R/W	8,16	Sampling clock setting register 1	V-43
	NFCNT	0x0000A054	R/W	8,16	Noise filter control register	V-44
	IRQEDGESEL	0x0000A056	R/W	8,16	Edge detection register	V-45

5.4.4 Noise Filter Sampling Clock Setting Registers

■ Sampling Clock Setting Register 0 (NFCLK0: 0x0000A050) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	NFCK 71	NFCK 70	NFCK 61	NFCK 60	NFCK 51	NFCK 50	NFCK 41	NFCK 40	NFCK 31	NFCK 30	NFCK 21	NFCK 20	NFCK 11	NFCK 10	NFCK 01	NFCK 00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-14	NFCK71 NFCK70	Select the IRQ7 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
13-12	NFCK61 NFCK60	Select the IRQ6 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
11-10	NFCK51 NFCK50	Select the IRQ5 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
9-8	NFCK41 NFCK40	Select the IRQ4 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
7-6	NFCK31 NFCK30	Select the IRQ3 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
5-4	NFCK21 NFCK20	Select the IRQ2 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
3-2	NFCK11 NFCK10	Select the IRQ1 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency
1-0	NFCK01 NFCK00	Select the IRQ0 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency

■ Sampling Clock Setting Register 1 (NFCLK1: 0x0000A052) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	NFCK 81	NFCK 80
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

bp	Flag	Description	Set condition
15-2	-	-	-
1-0	NFCK81 NFCK80	Select the IRQ8 sampling clock	00: 1/4 of IOCLK frequency 01: 1/8 of IOCLK frequency 10: 1/16 of IOCLK frequency 11: 1/32 of IOCLK frequency

5.4.5 Noise Filter Control Registers

This register is used to specify how to control noise filters, that is , specify whether to enable or disable noise filter for external interrupts as desired.

■ Noise Filter Control Register (NFCNT: 0x0000A054) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	NF CNT8	NF CNT7	NF CNT6	NF CNT5	NF CNT4	NF CNT3	NF CNT2	NF CNT1	NF CNT0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-9	-	-	-
8	NFCNT8	IRQ8 noise filter enable/disable	0: Disabled 1: Enabled
7	NFCNT7	IRQ7 noise filter enable/disable	0: Disabled 1: Enabled
6	NFCNT6	IRQ6 noise filter enable/disable	0: Disabled 1: Enabled
5	NFCNT5	IRQ5 noise filter enable/disable	0: Disabled 1: Enabled
4	NFCNT4	IRQ4 noise filter enable/disable	0: Disabled 1: Enabled
3	NFCNT3	IRQ3 noise filter enable/disable	0: Disabled 1: Enabled
2	NFCNT2	IRQ2 noise filter enable/disable	0: Disabled 1: Enabled
1	NFCNT1	IRQ1 noise filter enable/disable	0: Disabled 1: Enabled
0	NFCNT0	IRQ0 noise filter enable/disable	0: Disabled 1: Enabled

5.4.6 Edge Detection Registers

This register is used to specify how to control edge detection circuity. It specifies whether to enable or disable both-edge interrupt for each external interrupt pin.

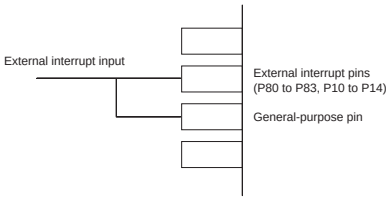
■ Edge Detection Register (IRQEDGESEL: 0x0000A056) [8, 16-bit access register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	IRQ EG8	IRQ EG7	IRQ EG6	IRQ EG5	IRQ EG4	IRQ EG3	IRQ EG2	IRQ EG1	IRQ EG0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
15-9	-	-	-
8	IRQEG8	IRQ8 both-edge detection enable/disable	0: Disabled 1: Enabled
7	IRQEG7	IRQ7 both-edge detection enable/disable	0: Disabled 1: Enabled
6	IRQEG6	IRQ6 both-edge detection enable/disable	0: Disabled 1: Enabled
5	IRQEG5	IRQ5 both-edge detection enable/disable	0: Disabled 1: Enabled
4	IRQEG4	IRQ4 both-edge detection enable/disable	0: Disabled 1: Enabled
3	IRQEG3	IRQ3 both-edge detection enable/disable	0: Disabled 1: Enabled
2	IRQEG2	IRQ2 both-edge detection enable/disable	0: Disabled 1: Enabled
1	IRQEG1	IRQ1 both-edge detection enable/disable	0: Disabled 1: Enabled
0	IRQEG0	IRQ0 both-edge detection enable/disable	0: Disabled 1: Enabled

When setting the generating condition of the external interrupt to the both-edge detection, select the rising edge by [5.2.7 External Interrupt Condition Specification Registers (EXTMD1, EXTMD0)].

If operating the edge detection register (IRQEDGESEL) to select the both-edge detection enable of IRQn, the value of port input register of the selected external interrupt pin is undefined and disagree with the pin input value.
Execute one of the following, to monitor the value of the external interrupt pin.
1. Do not select both-edge interrupt to monitor the value of the external interrupt pin.
2. To select both-edge interrupt and monitor the value of the external interrupt pin, connect the external inerrupt to the other general-purpose pin, and use as a port for monitor.



5.4.7 Noise Filter Operation

■ Noise Filter Operation

Noise filters can be used for external interrupts by setting the NFCNTn flag of the noise filter control register (NFCNT) to “1”. Each of these noise filter uses the sampling clock to count an external interrupt signal. The filter recognizes such a signal as an interrupt and issues a signal to the internal interrupt controller if the same signal level (“H” or “L”) is detected 3 times or more.

Be sure to disable interrupts when specifying whether to enable or disable noise filters.

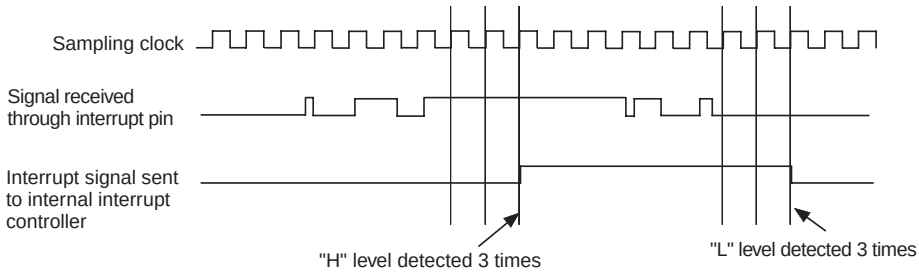


Figure:5.4.2 Noise Filter Operation

■ Noise Filter Sampling Frequency Setup

Sampling clock set registers (NFCLK0, NFCLK1) can be used to select a sampling clock of noise filters. The sampling clock can be selected from 1/4, 1/8, 1/16, and 1/32 of IOCLK.

■ Setup of Interrupt Generation Condition for External Interrupts

Generation condition for an external interrupt can be selected from 5 types: both-edge detection, rising edge, falling edge, H level, and L level. Edge detection registers (IRQEDGESEL) are used to set whether to enable or disable both-edge detection; and, if setting disable both-edge detection, external interrupt condition specification registers (EXTMD0, EXTMD1) are used to select the rising edge, falling edge, H level, and L level from. If setting enable both-edge detection, the EXTMD0 and EXTMD1 registers are used to select the rising edge.

5.4.8 Noise Filter Setup Example

■ Enable Noise Filter and Both-edge Setup Example

Noise remove function (noise filter function) is added to the input signal from P74 pin to generate the external interrupt 0 (IRQ0) at the both-edge. The sampling clock is set to 1/8 of IOCLK.

The following shows the setup procedure and description.

Setup Procedure	Description
(1) Disable the interrupt G2ICR(0x00008908) bp8: G2IE0=0	(1) Set the G2IE0 flag of the G2ICR register to “0” to disable the interrupt.
(2) Set the interrupt generation condition (both-edge detection) IRQEDGESEL(0x0000A056) bp0: IRQEG0=1	(2) Set the IRQEG0 flag of the edge detection register (IRQEDGE) to “1” to set the both-edge detection.
(3) Set the sampling clock NFCLK0(0x0000A050) bp1-0: NFCK01-0=01	(3) Set the NFCK01-0 flag of the sampling clock setup register 0 (NFCLK0) to “01” to set 1/8 sampling clock of IOCLK.
(4) Setup the noise filter operation NFCNT(0x0000A054) bp0: NFCNT0=1	(4) Set the NFCNT0 flag of the noise filter control register (NFCNT) to “1” for the noise filter operation to be valid.
(5) Set the interrupt generation condition (both-edge detection) EXTMD0(0x00008A80) bp1-0: IR0TG1-0=00	(5) Set the IROTG1-0 flag of the external interrupt condition specification register 0 (EXTMD0) to “00” to set the rising edge. This flag should be set to the rising edge.
(6) Set the interrupt level G2ICR(0x00008908) bp14-12: G2LV2-0=100	(6) Set the interrupt level by the G2LV2-0 flag of the G2ICR register. If the interrupt request flag has been already set, clear the interrupt request flag.
(7) Enable the interrupt G2ICR(0x00008908) bp8: G2IE0=1	(7) Set the G2IE0 flag of the G2ICR register to “1” to enable the interrupt.

■ Disable Noise Filter and programmable active edge Setup Example

The external interrupt 0 (IRQ0) is generated at the rising edge of the input signal from P74 pin.

Setup Procedure	Description
(1) Disable the interrupt G2ICR(0x00008908) bp8: G2IE0=0	(1) Set the G2IE0 flag of the G2ICR register to “0” to disable the interrupt.
(2) Set the interrupt generation condition (disable both-edge detection) IRQEDGESEL(0x0000A056) bp0: IRQEG0=0	(2) Set the IRQEG0 flag of the edge detection register (IRQEDGE) to “0” to set the both-edge interrupt detection disabled.
(3) Set the interrupt generation condition (falling edge) EXTMD0(0x00008A80) bp1-0: IR0TG1-0=01	(3) Set the IR0TG1-0 flag of the external interrupt condition specification register 0 (EXTMD0) to “00” to set the rising edge.
(4) Set the interrupt level G2ICR(0x00008908) bp14-12: G2LV2-0=100	(4) Set the interrupt level by the G2LV2-0 flag of the G2ICR register. If the interrupt request flag has been already set, clear the interrupt request flag.
(5) Enable the interrupt G2ICR(0x00008908) bp8: G2IE0=1	(5) Set the G2IE0 flag of the G2ICR register to “1” to enable the interrupt.

Chapter 6 ROM Correction

6

6.1 Overview

ROM correction provides the function to replace incorrect instructions and data stored in the internal ROM with correct ones.

This ROM correction function has 4 channels, each of which can correct 8 bytes of data from a desired address in the internal ROM.

6.1.1 Functions

	ROM correction
Channel	4 channels
Change byte	8 byte / 1 channel

6.1.2 Block Diagram

■ ROM Correction Block Diagram

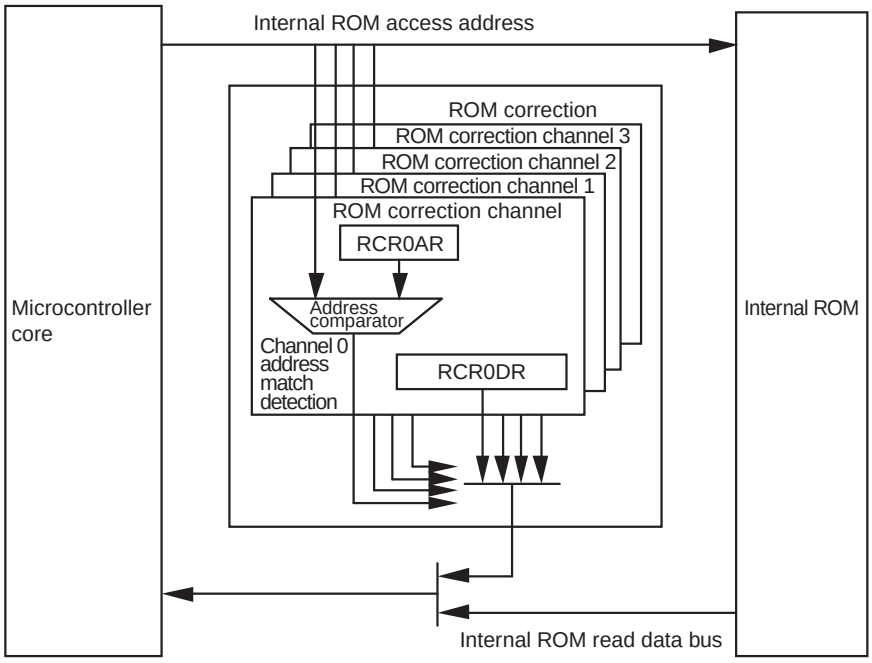


Figure:6.1.1 ROM Correction Block Diagram

6.2 ROM Correction Control Registers

ROM correction is comprised of the ROM correction address register (RCRnAR) and ROM correction data register (RCRnDR), and is controlled by the ROM correction control register (RCRCTR).

6.2.1 ROM Correction Control Registers List

Table: 6.2.1 shows the registers that control ROM correction.

Table:6.2.1 ROM Correction Control Registers List

	Register	Address	R/W	Access size	Name	Page
	RCRCTR	0x7FF00000	R/W	8,16,32	ROM correction control register	VI-4
Channel 0	RCR0AR	0x7FF00100	R/W	32	ROM correction 0 address register	VI-5
	RCR0DR	0x7FF00108	R/W	32	ROM correction 0 data register	VI-7
Channel 1	RCR1AR	0x7FF00110	R/W	32	ROM correction 1 address register	VI-5
	RCR1DR	0x7FF00118	R/W	32	ROM correction 1 data register	VI-8
Channel 2	RCR2AR	0x7FF00120	R/W	32	ROM correction 2 address register^	VI-6
	RCR2DR	0x7FF00128	R/W	32	ROM correction 2 data register	VI-9
Channel 3	RCR3AR	0x7FF00130	R/W	32	ROM correction 3 address register	VI-6
	RCR3DR	0x7FF00138	R/W	32	ROM correction 3 data register	VI-10

R/W Readable / Writable
R Readable
W Writable

6.2.2 ROM Correction Control Registers

This register that is a 8-bit readable / writable register controls ROM correction.

■ ROM Correction Control Registers (RCRCTR: 0x7FF00000) [8, 16, 32-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	RC MEN	RC CEN	-	RC RWE
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R	R/W

bp	Flag	Description	Set condition
7-4	-	-	-
3	RCMEN	ROM correction mode clear enable	0: ROM correction mode (RCCEN) clear disabled 1: ROM correction mode (RCCEN) clear enabled
2	RCCEN	ROM correction mode	0: ROM correction disabled 1: ROM correction enabled
1	-	-	-
0	RCRWE	ROM correction address / data register write enable	0: Write disabled 1: Write enabled

A ROM correction control register can be written under the following cases only.

Follow the arrow steps as described below.

Table:6.2.2 Value of Registers and Condition List

RCMEN	RCCEN	RCRWE	Condition
0	0	0	Disable the interrupt (except the NMI)
	↓		ROM correction reset status
0	0	1	Register change setting (* 1)
	↓		Register changeable status
0	1	0	ROM correction enabled status
	↓		ROM correction enabled status
1	1	0	ROM correction reset setting 1
	↓		ROM correction reset setting status
0	0	0	ROM correction reset setting 2
			ROM correction reset status

* 1: The registers are ROM correction address registers and ROM correction data registers.

6.2.3 ROM Correction Address Registers

Each of these registers specifies the address (channel number) at which ROM correction is to be performed. Data can be written only when the RCRWE flag in the ROM correction control register (RCRCTR) is “1”.

■ ROM Correction 0 Address Register (RCROAR: 0x7FF00100) [32-bit access register]

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC0 CEN	-	-	-	-	-	-	-	-	-	-	-	RC0 AD19	RC0 AD18	RC0 AD17	RC0 AD16
At reset	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
Access	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC0 AD15	RC0 AD14	RC0 AD13	RC0 AD12	RC0 AD11	RC0 AD10	RC0 AD9	RC0 AD8	RC0 AD7	RC0 AD6	RC0 AD5	RC0 AD4	RC0 AD3	RC0 AD2	RC0 AD1	RC0 AD0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
31	RC0CEN	ROM correction channel o enable	0: ROM correction disabled 1: ROM correction enabled
30-20	-	-	-
19-0	RC0AD19 to RC0AD0	ROM correction channel 0 address	These bits specify the lower 20 bits of the ROM address subject to ROM correction. 8 bytes of data from the above ROM address to (ROM address + 7) are subject to ROM correction.

■ ROM Correction 1 Address Register (RCR1AR: 0x7FF00110) [32-bit access register]

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC1 CEN	-	-	-	-	-	-	-	-	-	-	-	RC1 AD19	RC1 AD18	RC1 AD17	RC1 AD16
At rest	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
Access	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC1 AD15	RC1 AD14	RC1 AD13	RC1 AD12	RC1 AD11	RC1 AD10	RC1 AD9	RC1 AD8	RC1 AD7	RC1 AD6	RC1 AD5	RC1 AD4	RC1 AD3	RC1 AD2	RC1 AD1	RC1 AD0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
31	RC1CEN	ROM correction channel 1 enable	0: ROM correction disabled 1: ROM correction enabled
30-20	-	-	-
19-0	RC1AD19 to RC1AD0	ROM correction channel 1 address	These bits specify the lower 20 bits of the ROM address subject to ROM correction. 8 bytes of data from the above ROM address to (ROM address + 7) are subject to ROM correction.

■ ROM Correction 2 Address Register (RCR2AR: 0x7FF00120) [32-bit access register]

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC2 CEN	-	-	-	-	-	-	-	-	-	-	-	RC2 AD19	RC2 AD18	RC2 AD17	RC2 AD16
At reset	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
Access	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC2 AD15	RC2 AD14	RC2 AD13	RC2 AD12	RC2 AD11	RC2 AD10	RC2 AD9	RC2 AD8	RC2 AD7	RC2 AD6	RC2 AD5	RC2 AD4	RC2 AD3	RC2 AD2	RC2 AD1	RC2 AD0
At rest	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
31	RC2CEN	ROM correction channel 2 enabled	0: ROM correction disabled 1: ROM correction enabled
30-20	-	-	-
19-0	RC2AD19 to RC2AD0	ROM correction channel 2 address	These bits specify the lower 20 bits of the ROM address subject to ROM correction. 8 bytes of data from the above ROM address to (ROM address + 7) are subject to ROM correction.

■ ROM Correction 3 Address Register (RCR3AR: 0x7FF00130) [32-bit access register]

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC3 CEN	-	-	-	-	-	-	-	-	-	-	-	RC3 AD19	RC3 AD18	RC3 AD17	RC3 AD16
At reset	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
Access	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC3 AD15	RC3 AD14	RC3 AD13	RC3 AD12	RC3 AD11	RC3 AD10	RC3 AD9	RC3 AD8	RC3 AD7	RC3 AD6	RC3 AD5	RC3 AD4	RC3 AD3	RC3 AD2	RC3 AD1	RC3 AD0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
31	RC3CEN	ROM correction channel 3 enable	0: ROM correction disabled 1: ROM correction enabled
30-20	-	-	-
19-0	RC3AD19 to RC3AD0	ROM correction channel 3 address	These bits specify the lower 20 bits of the ROM address subject to ROM correction. 8 bytes of data from the above ROM address to (ROM address + 7) are subject to ROM correction.

6.2.4 ROM Correction Data Registers

Each of these registers specifies the correction data (channel number) used for ROM correction. Data can be written only when the RCRWE flag in the ROM correction control register (RCRCTR) is “1”.

■ ROM Correction 0 Data Register (RCR0DR: 0x7FF00108) [32-bit access register]

bp	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Flag	RC0 DT63	RC0 DT62	RC0 DT61	RC0 DT60	RC0 DT59	RC0 DT58	RC0 DT57	RC0 DT56	RC0 DT55	RC0 DT54	RC0 DT53	RC0 DT52	RC0 DT51	RC0 DT50	RC0 DT49	RC0 DT48
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Flag	RC0 DT47	RC0 DT46	RC0 DT45	RC0 DT44	RC0 DT43	RC0 DT42	RC0 DT41	RC0 DT40	RC0 DT39	RC0 DT38	RC0 DT37	RC0 DT36	RC0 DT35	RC0 DT34	RC0 DT33	RC0 DT32
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC0 DT31	RC0 DT30	RC0 DT29	RC0 DT28	RC0 DT27	RC0 DT26	RC0 DT25	RC0 DT24	RC0 DT23	RC0 DT22	RC0 DT21	RC0 DT20	RC0 DT19	RC0 DT18	RC0 DT17	RC0 DT16
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC0 DT15	RC0 DT14	RC0 DT13	RC0 DT12	RC0 DT11	RC0 DT10	RC0 DT9	RC0 DT8	RC0 DT7	RC0 DT6	RC0 DT5	RC0 DT4	RC0 DT3	RC0 DT2	RC0 DT1	RC0 DT0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
63-56	RC0DT63 to RC0DT56	ROM correction 0 correction data	Data of the address (lower 3bits set to 7) to be corrected
55-48	RC0DT55 to RC0DT48	ROM correction 0 correction data	Data of the address (lower 3bits set to 6) to be corrected
47-40	RC0DT47 to RC0DT40	ROM correction 0 correction data	Data of the address (lower 3bits set to 5) to be corrected
39-32	RC0DT39 to RC0DT32	ROM correction 0 correction data	Data of the address (lower 3bits set to 4) to be corrected
31-24	RC0DT31 to RC0DT24	ROM correction 0 correction data	Data of the address (lower 3bits set to 3) to be corrected
23-16	RC0DT23 to RC0DT16	ROM correction 0 correction data	Data of the address (lower 3bits set to 2) to be corrected
15-8	RC0DT15 to RC0DT8	ROM correction 0 correction data	Data of the address (lower 3bits set to 1) to be corrected
7-0	RC0DT7 to RC0DT0	ROM correction 0 correction data	Data of the address (lower 3bits set to 0) to be corrected

■ ROM Correction 1 Data Register (RCR1DR: 0x7FF00118) [32-bit access register]

bp	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Flag	RC1 DT63	RC1 DT62	RC1 DT61	RC1 DT60	RC1 DT59	RC1 DT58	RC1 DT57	RC1 DT56	RC1 DT55	RC1 DT54	RC1 DT53	RC1 DT52	RC1 DT51	RC1 DT50	RC1 DT49	RC1 DT48
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Flag	RC1 DT47	RC1 DT46	RC1 DT45	RC1 DT44	RC1 DT43	RC1 DT42	RC1 DT41	RC1 DT40	RC1 DT39	RC1 DT38	RC1 DT37	RC1 DT36	RC1 DT35	RC1 DT34	RC1 DT33	RC1 DT32
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC1 DT31	RC1 DT30	RC1 DT29	RC1 DT28	RC1 DT27	RC1 DT26	RC1 DT25	RC1 DT24	RC1 DT23	RC1 DT22	RC1 DT21	RC1 DT20	RC1 DT19	RC1 DT18	RC1 DT17	RC1 DT16
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC1 DT15	RC1 DT14	RC1 DT13	RC1 DT12	RC1 DT11	RC1 DT10	RC1 DT9	RC1 DT8	RC1 DT7	RC1 DT6	RC1 DT5	RC1 DT4	RC1 DT3	RC1 DT2	RC1 DT1	RC1 DT0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
63-56	RC1DT63 to RC1DT56	ROM correction 1 correction data	Data of the address (lower 3bits set to 7) to be corrected
55-48	RC1DT55 to RC1DT48	ROM correction 1 correction data	Data of the address (lower 3bits set to 6) to be corrected
47-40	RC1DT47 to RC1DT40	ROM correction 1 correction data	Data of the address (lower 3bits set to 5) to be corrected
39-32	RC1DT39 to RC1DT32	ROM correction 1 correction data	Data of the address (lower 3bits set to 4) to be corrected
31-24	RC1DT31 to RC1DT24	ROM correction 1 correction data	Data of the address (lower 3bits set to 3) to be corrected
23-16	RC1DT23 to RC1DT16	ROM correction 1 correction data	Data of the address (lower 3bits set to 2) to be corrected
15-8	RC1DT15 to RC1DT8	ROM correction 1 correction data	Data of the address (lower 3bits set to 1) to be corrected
7-0	RC1DT7 to RC1DT0	ROM correction 1 correction data	Data of the address (lower 3bits set to 0) to be corrected

■ ROM Correction 2 Data Register (RCR2DR: 0x7FF00128) [32-bit access register]

bp	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Flag	RC2 DT63	RC2 DT62	RC2 DT61	RC2 DT60	RC2 DT59	RC2 DT58	RC2 DT57	RC2 DT56	RC2 DT55	RC2 DT54	RC2 DT53	RC2 DT52	RC2 DT51	RC2 DT50	RC2 DT49	RC2 DT48
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Flag	RC2 DT47	RC2 DT46	RC2 DT45	RC2 DT44	RC2 DT43	RC2 DT42	RC2 DT41	RC2 DT40	RC2 DT39	RC2 DT38	RC2 DT37	RC2 DT36	RC2 DT35	RC2 DT34	RC2 DT33	RC2 DT32
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC2 DT31	RC2 DT30	RC2 DT29	RC2 DT28	RC2 DT27	RC2 DT26	RC2 DT25	RC2 DT24	RC2 DT23	RC2 DT22	RC2 DT21	RC2 DT20	RC2 DT19	RC2 DT18	RC2 DT17	RC2 DT16
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC2 DT15	RC2 DT14	RC2 DT13	RC2 DT12	RC2 DT11	RC2 DT10	RC2 DT9	RC2 DT8	RC2 DT7	RC2 DT6	RC2 DT5	RC2 DT4	RC2 DT3	RC2 DT2	RC2 DT1	RC2 DT0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
63-56	RC2DT63 to RC2DT56	ROM correction 2 correction data	Data of the address (lower 3bits set to 7) to be corrected
55-48	RC2DT55 to RC2DT48	ROM correction 2 correction data	Data of the address (lower 3bits set to 6) to be corrected
47-40	RC2DT47 to RC2DT40	ROM correction 2 correction data	Data of the address (lower 3bits set to 5) to be corrected
39-32	RC2DT39 to RC2DT32	ROM correction 2 correction data	Data of the address (lower 3bits set to 4) to be corrected
31-24	RC2DT31 to RC2DT24	ROM correction 2 correction data	Data of the address (lower 3bits set to 3) to be corrected
23-16	RC2DT23 to RC2DT16	ROM correction 2 correction data	Data of the address (lower 3bits set to 2) to be corrected
15-8	RC2DT15 to RC2DT8	ROM correction 2 correction data	Data of the address (lower 3bits set to 1) to be corrected
7-0	RC2DT7 to RC2DT0	ROM correction 2 correction data	Data of the address (lower 3bits set to 0) to be corrected

■ ROM Correction 3 Data Register (RCR3DR: 0x7FF00138) [32-bit access register]

bp	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Flag	RC3 DT63	RC3 DT62	RC3 DT61	RC3 DT60	RC3 DT59	RC3 DT58	RC3 DT57	RC3 DT56	RC3 DT55	RC3 DT54	RC3 DT53	RC3 DT52	RC3 DT51	RC3 DT50	RC3 DT49	RC3 DT48
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Flag	RC3 DT47	RC3 DT46	RC3 DT45	RC3 DT44	RC3 DT43	RC3 DT42	RC3 DT41	RC3 DT40	RC3 DT39	RC3 DT38	RC3 DT37	RC3 DT36	RC3 DT35	RC3 DT34	RC3 DT33	RC3 DT32
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Flag	RC3 DT31	RC3 DT30	RC3 DT29	RC3 DT28	RC3 DT27	RC3 DT26	RC3 DT25	RC3 DT24	RC3 DT23	RC3 DT22	RC3 DT21	RC3 DT20	RC3 DT19	RC3 DT18	RC3 DT17	RC3 DT16
At reset	x	x	x	x	x	Åx	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	RC3 DT15	RC3 DT14	RC3 DT13	RC3 DT12	RC3 DT11	RC3 DT10	RC3 DT9	RC3 DT8	RC3 DT7	RC3 DT6	RC3 DT5	RC3 DT4	RC3 DT3	RC3 DT2	RC3 DT1	RC3 DT0
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
63-56	RC3DT63 to RC3DT56	ROM correction 3 correction data	Data of the address (lower 3bits set to 7) to be corrected
55-48	RC3DT55 to RC3DT48	ROM correction 3 correction data	Data of the address (lower 3bits set to 6) to be corrected
47-40	RC3DT47 to RC3DT40	ROM correction 3 correction data	Data of the address (lower 3bits set to 5) to be corrected
39-32	RC3DT39 to RC3DT32	ROM correction 3 correction data	Data of the address (lower 3bits set to 4) to be corrected
31-24	RC3DT31 to RC3DT24	ROM correction 3 correction data	Data of the address (lower 3bits set to 3) to be corrected
23-16	RC3DT23 to RC3DT16	ROM correction 3 correction data	Data of the address (lower 3bits set to 2) to be corrected
15-8	RC3DT15 to RC3DT8	ROM correction 3 correction data	Data of the address (lower 3bits set to 1) to be corrected
7-0	RC3DT7 to RC3DT0	ROM correction 3 correction data	Data of the address (lower 3bits set to 0) to be corrected

6.3 ROM Correction Operation

ROM correction is designed to supply the microcontroller core (CPU, DMAC) with corrected data by replacing part of data - data read from internal ROM as a result of access by the microcontroller core (CPU, DMAC) - with the correction data stored in a ROM correction data register, thus allowing temporary correction of programs and data stored in internal ROM.

6.3.1 ROM Correction Operation

■ ROM Correction Operation

Whether internal ROM access is made within the address range subject to correction (8 bytes or less from the ROM correction address RCnAD) is detected by comparison between the address at which the microcontroller core accesses internal ROM and the ROM correction address specified in the ROM correction address register (RCRnAR). In the event of detection of access to an address subject to ROM correction, the data read from the ROM is replaced with the correction data set in a ROM correction data register (RCRnDR). This ROM correction function comes equipped with 4 channels, each of which can correct 8 bytes of data from a desired address in the internal ROM. Each channel has a ROM correction address register (RCRnAR) and ROM correction data register (RCRnDR) respectively to store correction address and correction data.

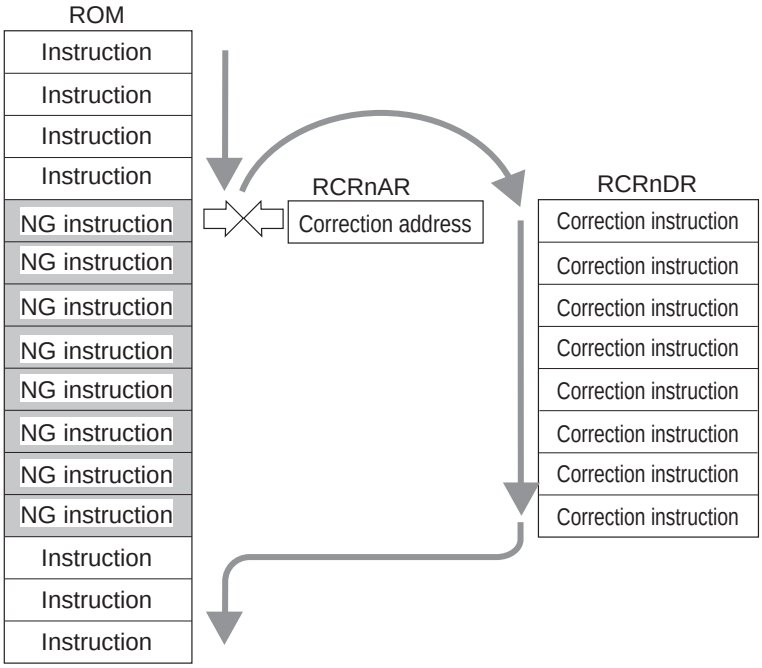


Figure:6.3.1 ROM Correction Operation

■ Setting ROM Correction

Table: 6.3.1 shows setting ROM correction.

Table:6.3.1 Setting ROM Correction

	Description	RCRCTR value
1	Checking the ROM correction control register (RCRCTR)	0x00
	Check that the RCRCTR register is set to “0x00”. When the RCRCTR register is set to “0x04” (during ROM correction enabled status), reset ROM correction.	
2	Set the ROM correction address register (RCRnAR) and the ROM correction data register (RCRnDR) write enabled	0x01
	Set the RCRnAR and the RCRnDR registers write enabled by writing “0x01” to the RCRCTR register	
3	Setting the RCRnAR register	0x01
	Set the lower 20 bits of the first address subject to ROM correction and the value of the RCnCEN flag. Setting the RCnCEN flag of the RCRnAR register to “1” allows ROM correction for the target channel to be enabled. To disable an unused channel, set the RCnCEN flag to “0”.	
4	Setting the RCRnDR register	0x01
	Set 8- byte data used for ROM correction. Each byte of correction data must be set at bit positions of the RCRnDR register determined by the lower 3 bits of the address.	
5	Setting ROM correction enabled	0x04
	Set ROM correction enabled by writing “0x04” to the RCRCTR register .	

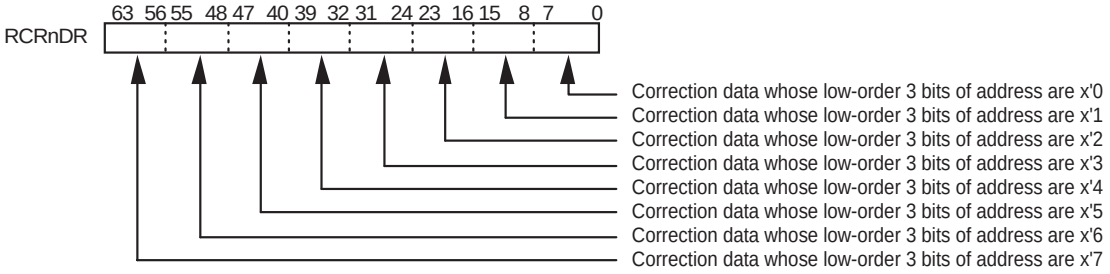


Figure:6.3.2 RCRnDR Register and Correction Data

■ Resetting ROM Correction

Table: 6.3.2 shows resetting ROM correction.

Table:6.3.2 Resetting ROM Correction

	Description	RCRCTR value
1	Resetting ROM correction 1	0x0C
	Write “0x0C” to the ROM correction control register (RCRCTR) to enable ROM correction mode clear (reset)	
2	Resetting ROM correction 2	0x00
	Write a “0x00” to the RCRCTR register to disable ROM correction	

If it is necessary to make changes to settings when ROM correction is enabled (when the RCRCTR register is “0x04”), reset ROM correction once. Then, set ROM correction again.

6.3.2 ROM Correction Setting Example

■ ROM Correction Setting Example (1)

8 bytes of data stored in the internal ROM addressees “0x40002000 ~ 0x40002007” are corrected by ROM correction channel 0 as indicated in the following.

	Lower 3 bits	Before change	→	After change
0x40002000	0	0x00	→	0x00
+1	1	0x00		0x11
+2	2	0x00		0x22
+3	3	0x00		0x33
+4	4	0x00		0x44
+5	5	0x00		0x55
+6	6	0x00		0x66
+7	7	0x00		0x77

Setup Procedure	Description
(1) Confirm ROM correction status RCRCTR (0x7FF00000) bp3: RCMEN=0 bp2: RCCEN=0 bp0: RCRWE=0	(1) Confirm that the ROM correction control register (RCRCTR) is set to “0x00” (ROM correction enable). When it is set to “0x04” (ROM correction enable), reset ROM correction.
(2) Set a register write enabled RCRCTR (0x7FF00000) bp3: RCMEN=0 bp2: RCCEN=0 bp0: RCRWE=1	(2) Write “0x01” to the RCRCTR register to set the ROM correction address register (RCR0AR) and the ROM correction data register (RCR0DR) write enabled.
(3) Set the RCR0AR register RCR0AR (0x7FF00100) bp19-0: RC0AD19-0=0x02000 bp31: RC0CEN=1	(3) Set the lower 20 bits of the first address subject to ROM correction in bp19~bp0 of the RCR0AR register and theRC0CEN flag to “1” in bp31.
(4) Set the RC0DR register RCR0DR (0x7FF00138) = 0x7766554433221100 bp63-0: RC0DT63-0 =0x7766554433221100	(4) Set 8 bytes of data (0x7766554433221100) used for ROM correction to the RCR0DR register.
(5) Set ROM correction enabled	(5) Write “0x04” to the RCRCTR register to enable ROM correction.

■ ROM Correction Setting Example (2)

8 bytes of data stored in the internal ROM addressees “0x40006543 ~ 0x4000654A” are corrected by ROM correction channel 0 as indicated in the following.

	Lower 3 bits	Before change	→	After change
0x40006543	3	0x00	→	0x01
+1	4	0x00		0x23
+2	5	0x00		0x45
+3	6	0x00		0x67
+4	7	0x00		0x89
+5	0	0x00		0xAB
+6	1	0x00		0xCD
+7	2	0x00		0xEF

Setup Procedure	Description
(1) Confirm ROM correction RCRCTR (0x7FF00000) bp3: RCMEN=0 bp2: RCCEN=0 bp0: RCRWE=0	(1) Confirm that the ROM correction control register (RCRCTR) is set to “0x00” (ROM correction enable). When it is set to “0x04” (ROM correction enabled), reset ROM correction.
(2) Set a register write enabled RCRCTR (0x7FF00000) bp3: RCMEN=0 bp2: RCCEN=0 bp0: RCRWE=1	(2) Write “0x01” to the RCRCTR register to set the ROM correction address register (RCR3AR) and the ROM correction data register (RCR3DR) write enabled.
(3) Set the RCR3AR register RCR3AR (0x7FF00130) bp19-0: RC3AD19-0=0x06543 bp31: RC3CEN=1	(3) Set the lower 20 bits of the first address subject to ROM correction in bp19~bp0 of the RCR3AR register and theRC3CEN flag to “1” in bp31.
(4) Set the RC3DR register RCR3DR (0x7FF00108) =0x8967452301EFCDAB bp63-0: RC3DT63-0 =0x8967452301EFCDAB	(4) Set 8 bytes of data (0x8967452301EFCDAB) used for ROM correction to the RCR3DR register.
(5) Set ROM correction enabled	(5) Write “0x04” to the RCRCTR register to enable ROM correction.

6.3.3 Cautions for Programming

ROM correction can be programmed such that 8 bytes of data starting with an address that is a multiple of 8 are changed through 1 channel. For instance, when 8-byte data change from x’40006543 is selected, 8-byte data change from x’40006540 to x’40006547 and from x’40006548 to x’4000654F cannot be selected. When more than 8 bytes of data must be continuously changed, be sure to program ROM correction such that 8-byte data change through each of the channels starts with an address that is a multiple of 8.

Chapter 7 I/O Port

7

7.1 Overview

A total of 61 pins on this LSI, including those shared with special function pins, are allocated for the I/O ports of port 0 to port A. Each I/O port is allocated in the internal I/O space, and can access by bytes or bits the same as RAM.

Table:7.1.1 I/O Ports and Special Function Pins

	I/O port/special function pins		I/O		I/O port/special function pins		I/O
Port1	P10	IRQ04	I/O	Port6	P62	PWM10	I/O
	P11	IRQ05	I/O		P63	NPWM10	I/O
	P12	IRQ06	I/O		P64	PWM11	I/O
	P13	IRQ07	I/O		P65	NPWM11	I/O
	P14	IRQ08	I/O		P66	PWM12	I/O
	P16	TM17IO	I/O		P67	NPWM12	I/O
	P17	SBO2	I/O	Port7	P72	TM11IO0	I/O
Port2	P20	SBT2	I/O		P73	TM11IO1	I/O
	P21	SBI2	I/O	Port8	P80	IRQ00	I/O
	P22	SBO1	I/O		P81	IRQ01	I/O
	P23	SBT1	I/O		P82	IRQ02	I/O
	P24	SBI1	I/O		P83	IRQ03	I/O
	P25	SBO0	I/O	Port9	P90	ADIN00	I/O
	P26	SBT0	I/O		P91	ADIN01	I/O
	P27	SBI0	I/O		P92	ADIN02	I/O
Port3	P31	TM1IO	I/O		P93	ADIN03	I/O
	P32	TM2IO	I/O		P94	ADIN04	I/O
	P33	TM3IO	I/O		P95	ADIN05	I/O
	P34	TM4IO	I/O		P96	ADIN06	I/O
	P35	TM5IO	I/O		P97	ADIN07	I/O
	P36	TM8AIO	I/O	PortA	PA0	ADIN08	I/O
	P37	TM8BIO	I/O		PA1	ADIN09	I/O
Port4	P42	TM9AIO	I/O		PA2	ADIN10	I/O
	P43	TM9BIO	I/O		PA3	ADIN11	I/O
	P46	TM10AIO	I/O		PA4	ADIN12	I/O
	P47	TM10BIO	I/O		PA5	ADIN13	I/O
Port5	P51	TM7IO	I/O		PA6	ADIN14	I/O
	P52	PWM00	I/O		PA7	ADIN15	I/O
	P53	NPWM00	I/O				
	P54	PWM01	I/O				
	P55	NPWM01	I/O				
	P56	PWM02	I/O				
	P57	NPWM02	I/O				

7.1.1 Status at Reset

Table: 7.1.2 shows the I/O port status at reset.

Table:7.1.2 I/O Port Status at Reset

Port	I/O mode	Pull-up resistor	I/O port, special functions
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	No pull-up resistor	I/O port
Port 3	Input mode	No pull-up resistor	I/O port
Port 4	Input mode	No pull-up resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port 9	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up resistor	I/O port

7.1.2 Block Diagram

■ Block Diagram (P10, P11, P12, P13, P14, P80, P81, P82, P83)

P10 to P14, P80 to P83 are dual-purpose ports that also serve as external interrupt pins; IRQ00 to 08.

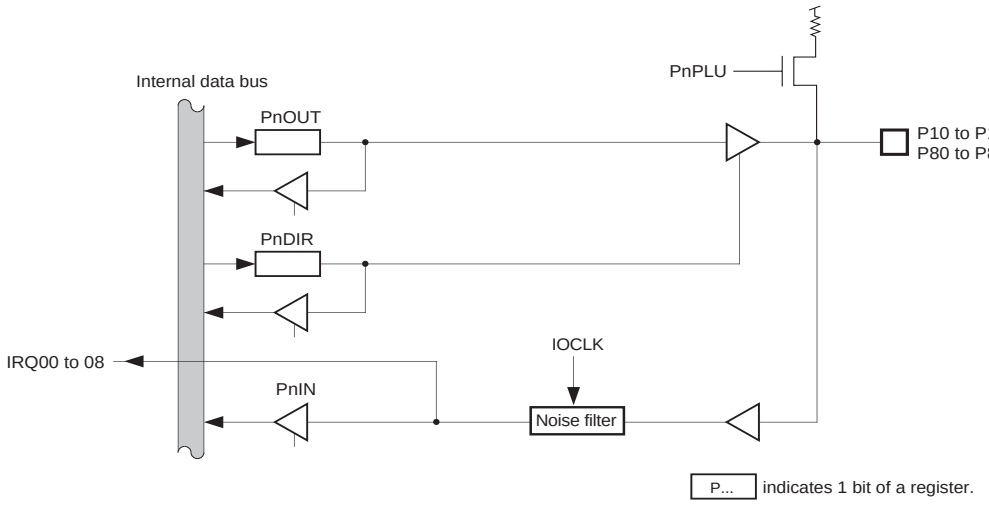


Figure:7.1.1 Block Diagram (P10 to P14, P80 to P83)

■ Block Diagram (P17, P20, P21, P22, P23, P24, P25, P26, P27)

P17, P20 to P27 are dual-purpose ports that serve as serial interface pins.

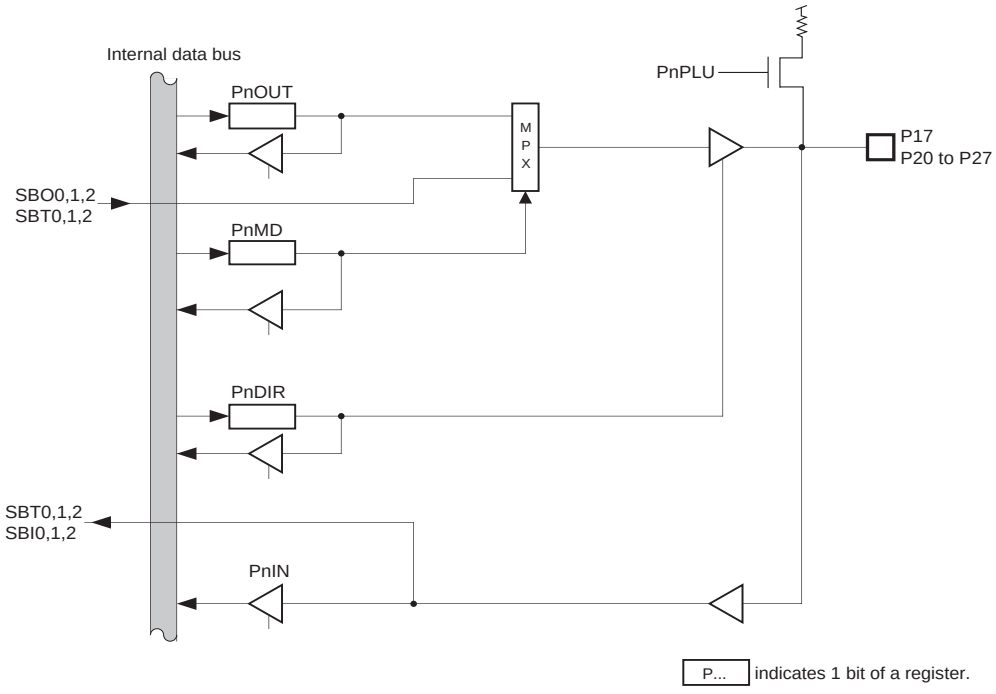


Figure:7.1.2 Block Diagram (P17, P20 to P27)

■ Block Diagram (P16, P31, P32, P33, P34, P35, P51)

P16, P31 to P35, P51 are dual-purpose ports that serve as 8-bit timer pins.

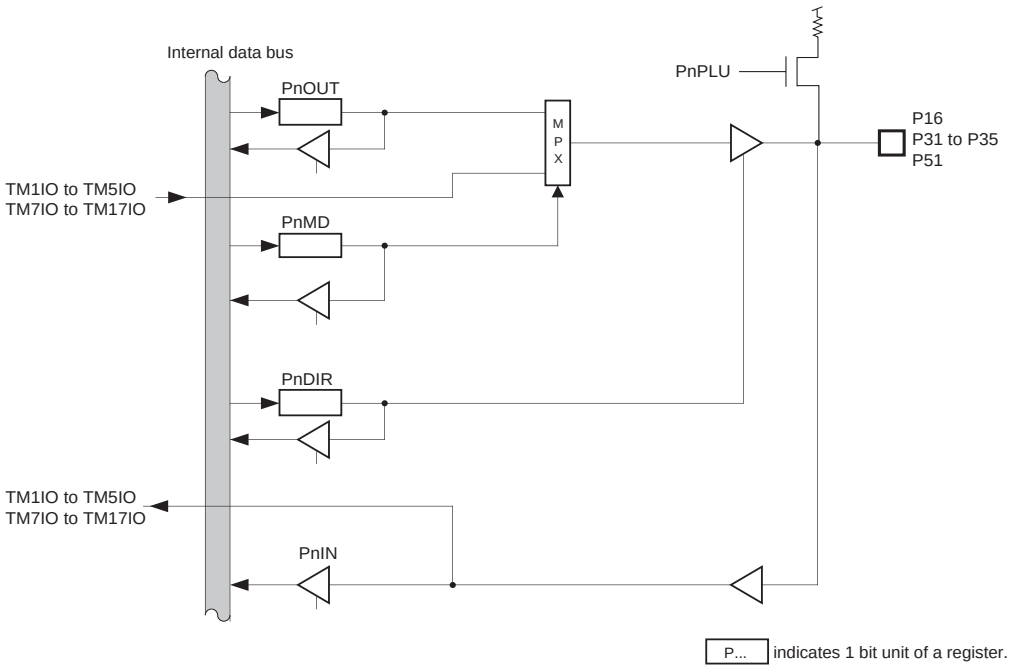


Figure:7.1.3 Block Diagram (P16, P31 to P35, P51)

■ Block Diagram (P36, P37, P42, P43, P46, ,P47)

P36, P37, P42, P43, P46, ,P47 are dual-purpose that serve as 16-bit timer pins.

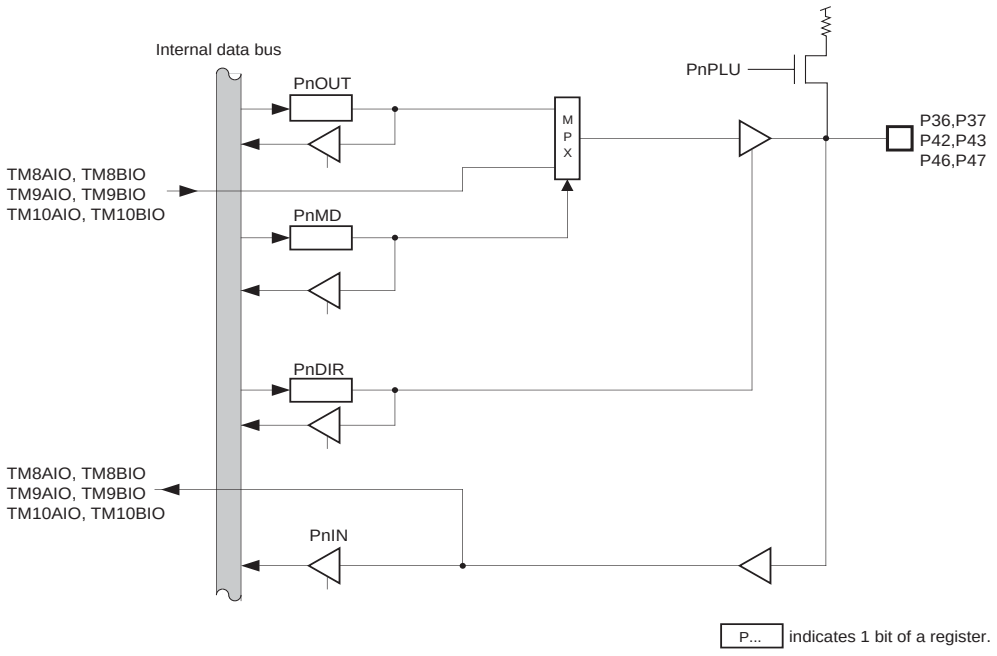


Figure:7.1.4 Block Diagram (P36, P37, P42, P43, P46, ,P47)

■ Block Diagram (P72, P73)

P72, P73 are dual-purpose that serve as 16-bit timer pins.

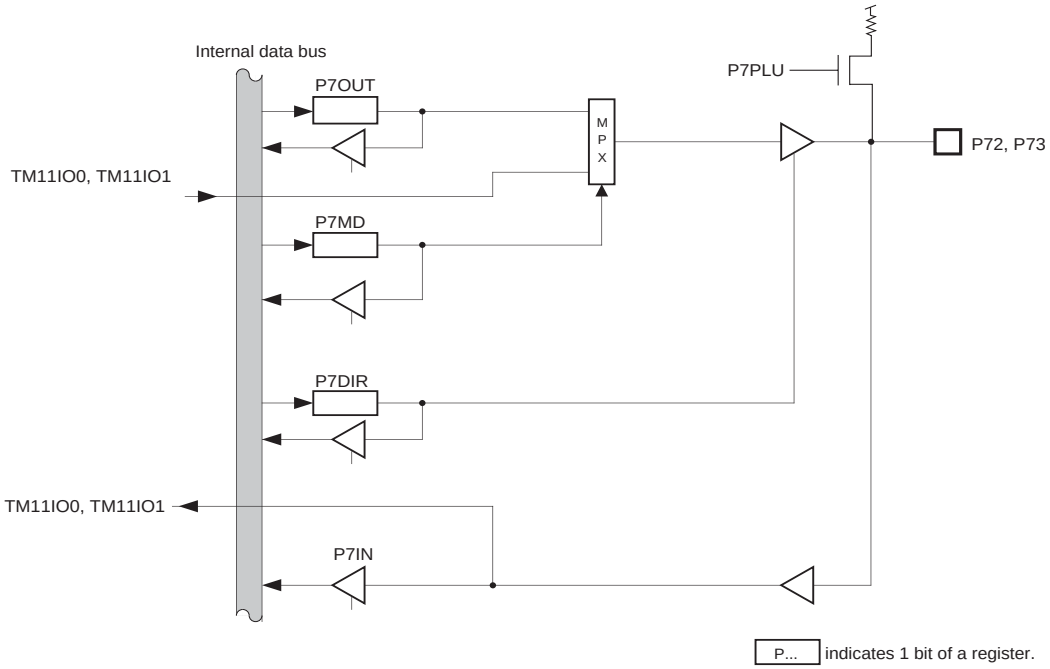


Figure:7.1.5 Block Diagram (P72 to P73)

■ Block Diagram (P52, P53, P54, P55, P56, P57)

P52 to P57 are dual-purpose ports that serve as PWM0 output pins.

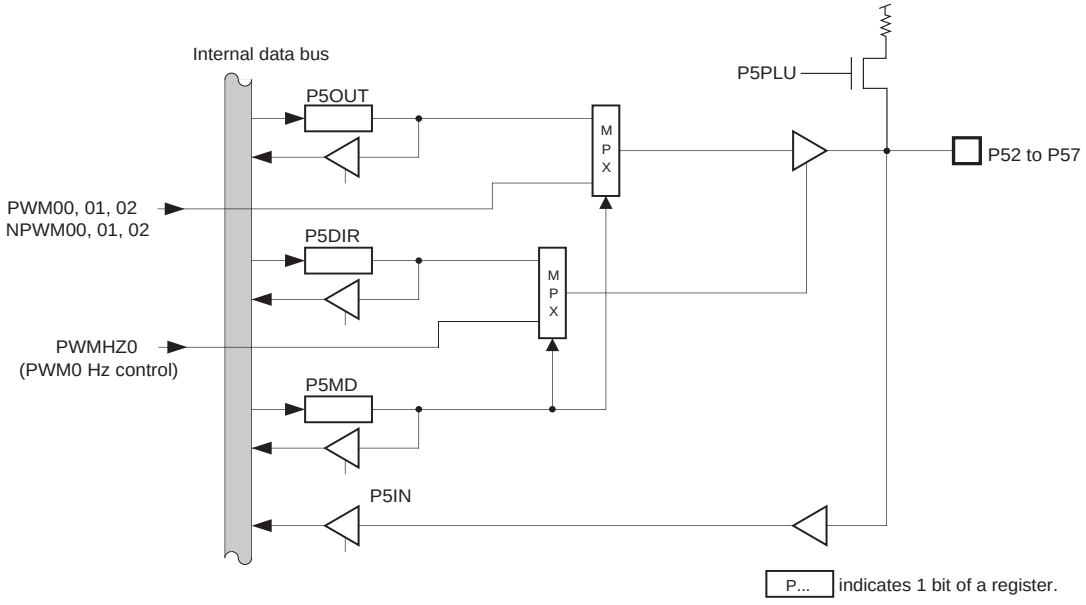


Figure:7.1.6 Block Diagram (P52 to P57)

■ Block Diagram (P62, P63, P64, P65, P66, P67)

P62 to P67 are dual-purpose ports that serve as PWM1 output pins.

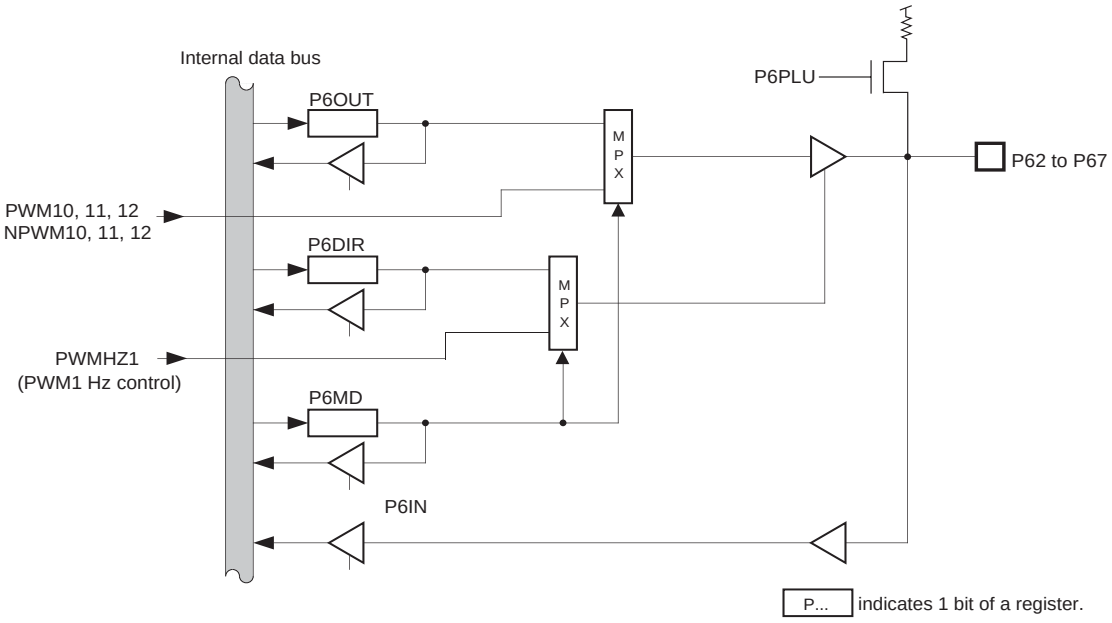


Figure:7.1.7 Block Diagram (P62 to P67)

■ Block Diagram (P90, P91, P92, P93, P94, P95, P96, P97,
PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7,

P90 to P97, PA0 to PA7 are dual-purpose ports that serve as AD input pins.

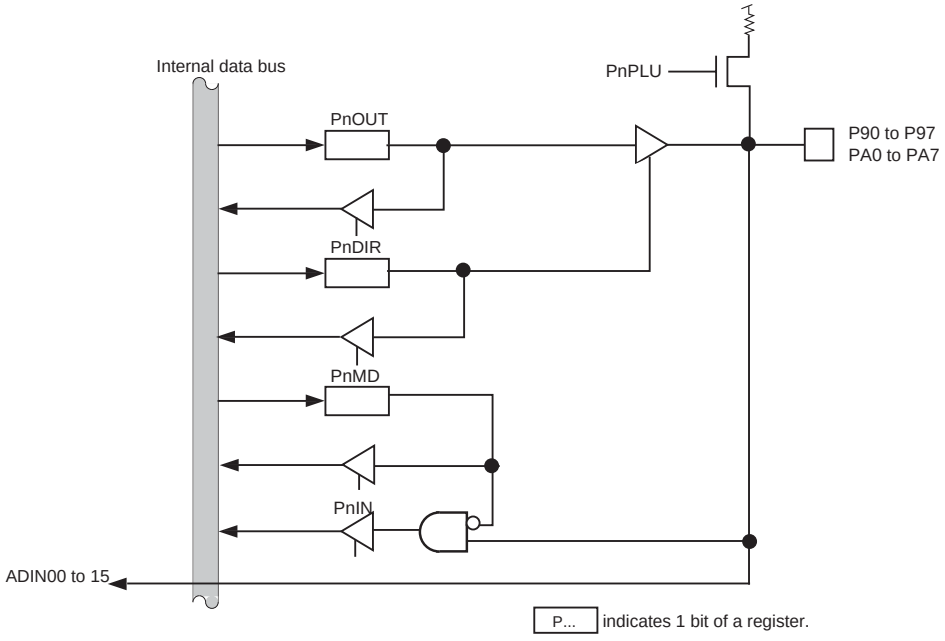


Figure:7.1.8 Block Diagram (P90 to P97, PA0 to PA7)

7.2 Control Registers

Port 1 to port A are controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU), and registers that control special function pins (PnMD).

7.2.1 Control Register List

Table: 7.2.1 shows the I/O port control registers.

Table:7.2.1 I/O Port Control Register List

	Register	Address	R/W	Access size	Function	Page
Port 1	P1OUT	0x0000A001	R/W	8	Port 1 output register	VII-10
	P1IN	0x0000A011	R	8	Port 1 input register	VII-10
	P1DIR	0x0000A021	R/W	8	Port 1 I/O control register	VII-11
	P1MD	0x0000A031	R/W	8	Port 1 output mode register	VII-11
	P1PLU	0x0000A041	R/W	8	Port 1 pull-up resistor control register	VII-12
Port 2	P2OUT	0x0000A002	R/W	8	Port 2 output register	VII-13
	P2IN	0x0000A012	R	8	Port 2 input register	VII-13
	P2DIR	0x0000A022	R/W	8	Port 2 I/O control register	VII-13
	P2MD	0x0000A032	R/W	8	Port 2 output mode register	VII-14
	P2PLU	0x0000A042	R/W	8	Port 2 pull-up resistor control register	VII-14
Port 3	P3OUT	0x0000A003	R/W	8	Port 3 output register	VII-15
	P3IN	0x0000A013	R	8	Port 3 input register	VII-15
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3PLU	0x0000A043	R/W	8	Port 3 pull-up resistor control register	VII-16
Port 4	P4OUT	0x0000A004	R/W	8	Port 4 output register	VII-17
	P4IN	0x0000A014	R	8	Port 4 input register	VII-17
	P4DIR	0x0000A024	R/W	8	Port 4 I/O control register	VII-18
	P4MD	0x0000A034	R/W	8	Port 4 output mode register	VII-18
	P4PLU	0x0000A044	R/W	8	Port 4 pull-up resistor control register	VII-19
Port 5	P5OUT	0x0000A005	R/W	8	Port 5 output register	VII-20
	P5IN	0x0000A015	R	8	Port 5 input register	VII-20
	P5DIR	0x0000A025	R/W	8	Port 5 I/O control register	VII-20
	P5MD	0x0000A035	R/W	8	Port 5 output mode register	VII-21
	P5PLU	0x0000A045	R/W	8	Port 5 pull-up resistor control register	VII-21

	Register	Address	R/W	Access size	Function	Page
Port 6	P6OUT	0x0000A006	R/W	8	Port 6 output register	VII-22
	P6IN	0x0000A016	R	8	Port 6 input register	VII-22
	P6DIR	0x0000A026	R/W	8	Port 6 I/O control register	VII-22
	P6MD	0x0000A036	R/W	8	Port 6 output mode register	VII-23
	P6PLU	0x0000A046	R/W	8	Port 6 pull-up resistor control register	VII-23
Port 7	P7OUT	0x0000A007	R/W	8	Port 7 output register	VII-24
	P7IN	0x0000A017	R	8	Port 7 input register	VII-24
	P7DIR	0x0000A027	R/W	8	Port 7 I/O control register	VII-24
	P7MD	0x0000A037	R/W	8	Port 7 output mode register	VII-25
	P7PLU	0x0000A047	R/W	8	Port 7 pull-up resistor control register	VII-25
Port 8	P8OUT	0x0000A008	R/W	8	Port 8 output register	VII-26
	P8IN	0x0000A018	R	8	Port 8 input register	VII-26
	P8DIR	0x0000A028	R/W	8	Port 8 I/O control register	VII-26
	P8PLU	0x0000A048	R/W	8	Port 8 pull-up resistor control register	VII-27
Port 9	P9OUT	0x0000A009	R/W	8	Port 9 output register	VII-28
	P9IN	0x0000A019	R	8	Port 9 input register	VII-28
	P9DIR	0x0000A029	R/W	8	Port 9 I/O control register	VII-28
	P9MD	0x0000A039	R/W	8	Port 9 output mode register	VII-29
	P9PLU	0x0000A049	R/W	8	Port 9 pull-up resistor control register	VII-29
Port A	PAOUT	0x0000A00A	R/W	8	Port A output register	VII-30
	PAIN	0x0000A01A	R	8	Port A input register	VII-30
	PADIR	0x0000A02A	R/W	8	Port A I/O control register	VII-30
	PAMD	0x0000A03A	R/W	8	Port A output mode register	VII-31
	PAPLU	0x0000A04A	R/W	8	Port A pull-up resistor control register	VII-31

R/W Readable / Writable
R Readable
W Writable

7.2.2 Control Registers

■ Port 1 Output Register (P1OUT: 0x0000A001) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flagº	P17O	P16O	Reserved	P14O	P13O	P12O	P11O	P10O
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P17O to P16O	Output data	Output data
5	Reserved	-	Write "0"
4-0	P14O to P10O	Output data	Output data

■ Port 1 Input Register (P1IN: 0x0000A011) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P17I	P16I	Reserved	P14I	P13I	P12I	P11I	P10I
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-6	P17I to P16I	Input data	Input data
5	Reserved	-	"0" is read out
4-0	P14I to P10I	Input data	Input data

■ Port 1 I/O Control Register (P1DIR: 0x0000A021) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P17D	P16D	Reserved	P14D	P13D	P12D	P11D	P10D
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P17D to P16D	I/O mode selection	0: Input mode 1: Output mode
5	Reserved	-	Write "0"
4-0	P14D to P10D	I/O mode selection	0: Input mode 1: Output mode

■ Port 1 Output Mode Register (P1MD: 0x0000A031) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P17M	P16M	Reserved	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R	R	R	R	R

bp	Flag	Description	Set condition
7	P17M	Output pin setting	0: P17 pin 1: SB02 pin
6	P16M	Output pin setting	0: P16 pin 1: TM17IO pin
5	Reserved	-	Write "0"
4-0	-	-	-

■ Port 1 Pull-up Resistor Control Mode Register (P1PLU: 0x0000A041) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P17R	P16R	Reserved	P14R	P13R	P12R	P11R	P10R
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P17R to P16R	Pull-up resistor selection	0: Not added 1:Added
5	Reserved	-	Write "0"
4-0	P14R to P10R	Pull-up resistor selection	0: Not added 1:Added

■ Port 2 Output Register (P2OUT: 0x0000A002) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P27O	P26O	P25O	P24O	P23O	P22O	P21O	P20O
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P27O to P20O	Output data	Output data

■ Port 2 Input Register (P2IN: 0x0000A012) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P27I	P26I	P25I	P24I	P23I	P22I	P21I	P20I
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-0	P27I to P20I	Input data	ìInput data

■ Port 2 I/O Control Register (P2DIR: 0x0000A022) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P27D	P26D	P25D	P24D	P23D	P22D	P21D	P20D
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P27D to P20D	I/O mode selection	0: Input mode 1: Output mode

■ Port 2 Output Mode Register (P2MD: 0x0000A032) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	-	P26M	P25M	-	P23M	P22M	-	P20M
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R	R/W	R/W	R	R/W

bp	Flag	Description	Set condition
7	-	-	-
6	P26M	Output pin setting	0: P26 pin 1: SBT0 pin
5	P25M	Output pin setting	0: P25 pin 1: SBO0 pin
4	-	-	-
3	P23M	Output pin setting	0: P23 pin 1: SBT1 pin
2	P22M	Output pin setting	0: P22 pin 1: SBO1 pin
1	-	-	-
0	P20M	Output pin setting	0: P20 pin 1: SBT2 pin

■ Port 2 Pull-up Resistor Control Register (P2PLU: 0x0000A042) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P27R	P26R	P25R	P24R	P23R	P22R	P21R	P20R
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P27R to P20R	Pull-up resistor selection	0: Not added 1:Added

■ Port 3 Output Register (P3OUT: 0x0000A003) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P37O	P36O	P35O	P34O	P33O	P32O	P31O	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P37O to P31O	Output data	Output data
0	Reserved	-	Write "0"

■ Port 3 Input Register (P3IN: 0x0000A013) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P37I	P36I	P35I	P34I	P33I	P32I	P31I	Reserved
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-1	P37I to P31I	Input data	Input data
0	Reserved	-	-

■ Port 3 I/O Control Register (P3DIR: 0x0000A023) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P37D	P36D	P35D	P34D	P33D	P32D	P31D	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P37D to P31D	I/O mode selection	0: Input mode 1: Output mode
0	Reserved	-	Write "0"

■ Port 3 Output Mode Register (P3MD: 0x0000A033) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P37M	P36M	P35M	P34M	P33M	P32M	P31M	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	P37M	Output pin setting	0: P37 pin 1: TM8BI0 pin
6	P36M	Output pin setting	0: P36 pin 1: TM8AI0 pin
5	P35M	Output pin setting	0: P35 pin 1: TM5I0 pin
4	P34M	Output pin setting	0: P34 pin 1: TM4I0 pin
3	P33M	Output pin setting	0: P33 pin 1: TM3I0 pin
2	P32M	Output pin setting	0: P32 pin 1: TM2I0 pin
1	P31M	Output pin setting	0: P31 pin 1: TM1I0 pin
0	Reserved	-	Write "0"

■ Port 3 Pull-up Resistor Control Register (P3PLU: 0x0000A043) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P37R	P36R	P35R	P34R	P33R	P32R	P31R	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P37R to P31R	Pull-up resistor selection	0: Not added 1:Added
0	Reserved	-	Write "0"

■ Port 4 Output Register (P4OUT: 0x0000A004) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P47O	P46O	Reserved	Reserved	P43O	P42O	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P47O to P46O	Output data	Output data
5-4	Reserved	-	Write "0"
3-2	P43O to P42O	Output data	Output data
1-0	Reserved	-	Write "0"

■ Port 4 Input Register (P4IN: 0x0000A014) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P47I	P46I	Reserved	Reserved	P43I	P42I	Reserved	Reserved
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-6	P47I to P46I	Input data	Input data
5-4	Reserved	-	-
3-2	P43I to P42I	Input data	Input data
1-0	Reserved	-	-

■ Port 4 I/O Control Register (P4DIR: 0x0000A024) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P47D	P46D	Reserved	Reserved	P43D	P42D	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P47D to P46D	I/O mode selection	0: Input mode 1: Output mode
5-4	Reserved	-	Write "0"
3-2	P43D to P42D	I/O mode selection	0: Input mode 1: Output mode
1-0	Reserved	-	Write "0"

■ Port 4 Output Mode Register (P4MD: 0x0000A034) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P47M	P46M	Reserved	Reserved	P43M	P42M	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	P47M	Output pin setting	0: P47 pin 1: TM10BI0 pin
6	P46M	Output pin setting	0: P46 pin 1: TM10AI0 pin
5-4	Reserved	-	Write "0"
3	P43M	Output pin setting	0: P43 pin 1: TM9BI0 pin
2	P42M	Output pin setting	0: P42 pin 1: TM9AI0 pin
1-0	Reserved	-	Write "0"

■ Port 4 Pull-up Resistor Control Register (P4PLU: 0x0000A044) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P47R	P46R	Reserved	Reserved	P43R	P42R	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-6	P47D to P46D	Pull-up resistor selection	0: No added 1: Added
5-4	Reserved	-	Write "0"
3-2	P43D to P42D	Pull-up resistor selection	0: No added 1: Added
1-0	Reserved	-	Write "0"

■ Port 5 Output Register (P5OUT: 0x0000A005) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P57O	P56O	P55O	P54O	P53O	P52O	P51O	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P57O to P51O	Output data	Output data
0	Reserved	-	Write "0"

■ Port 5 Input Register (P5IN: 0x0000A015) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P57I	P56I	P55I	P54I	P53I	P52I	P51I	Reserved
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-1	P57I to P51I	Input data	Input data
0	Reserved	-	-

■ Port 5 I/O Control Register (P5DIR: 0x0000A025) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flagº	P57D	P56D	P55D	P54D	P53D	P52D	P51D	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P57D to P51D	I/O mode selection	0: Input mode 1: Output mode
0	Reserved	-	Write "0"

■ Port 5 Output Mode Register (P5MD: 0x0000A035) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P57M	P56M	P55M	P54M	P53M	P52M	P51M	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	P57M	Output pin setting	0: P57 pin 1: NPWM02 pin
6	P56M	Output pin setting	0: P56 pin 1: PWM02 pin
5	P55M	Output pin setting	0: P55 pin 1: NPWM01 pin
4	P54M	Output pin setting	0: P54 pin 1: PWM01 pin
3	P53M	Output pin setting	0: P53 pin 1: NPWM00 pin
2	P52M	Output pin setting	0: P52 pin 1: PWM00 pin
1	P51M	Output pin setting	0: P51 pin 1: TM7I0 pin
0	Reserved	-	Write "0"

■ Port 5 Pull-up Resistor Control Register (P5PLU: 0x0000A045) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P57R	P56R	P55R	P54R	P53R	P52R	P51R	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-1	P57R to P51R	Pull-up resistor selection	0: Not added 1:Added
0	Reserved	-	Write "0"

■ Port 6 Output Register (P6OUT: 0x0000A006) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P67O	P66O	P65O	P64O	P63O	P62O	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-2	P67O to P62O	Output data	Output data
1-0	Reserved	-	Write "0"

■ Port 6 Input Register (P6IN: 0x0000A016) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P67I	P66I	P65I	P64I	P63I	P62I	Reserved	Reserved
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-2	P67I to P62I	Input data	Input data
1-0	Reserved	-	-

■ Port 6 I/O Control Register (P6DIR: 0x0000A026) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P67D	P66D	P65D	P64D	P63D	P62D	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-2	P67D to P62D	I/O mode selection	0: Input mode 1: Output mode
1-0	Reserved	-	Write "0"

■ Port 6 Output Mode Register (P6MD: 0x0000A036) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P67M	P66M	P65M	P64M	P63M	P62M	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bp	Flag	Description	Set condition
7	P67M	Output pin setting	0: P67 pin 1: NPWM12 pin
6	P66M	Output pin setting	0: P66 pin 1: PWM12 pin
5	P65M	Output pin setting	0: P65 pin 1: NPWM11 pin
4	P64M	Output pin setting	0: P64 pin 1: PWM11 pin
3	P63M	Output pin setting	0: P63 pin 1: NPWM10 pin
2	P62M	Output pin setting	0: P62 pin 1: PWM10 pin
1-0	-	-	-

■ Port 6 Pull-up Resistor Control Register (P6PLU: 0x0000A046) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P67R	P66R	P65R	P64R	P63R	P62R	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
72	P67R to P62R	Pull-up resistor selection	0: No added 1: Added
1-0	Reserved	-	Write "0"

■ Port 7 Output Register (P7OUT: 0x0000A007) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P73O	P72O	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-2	P73O to P72O	Output data	Output data
1-0	-	-	-

■ Port 7 Input Register (P7IN: 0x0000A017) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P73I	P72I	-	-
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	-
3-2	P73I to P72I	Input data	Input data
1-0	-	-	-

■ Port 7 I/O Control Register (P7DIR: 0x0000A027) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P73D	P72D	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-2	P73D to P72D	I/O mode selection	0: Input mode 1: Output mode
1-0	-	-	-

■ Port 7 Output Mode Register (P7MD: 0x0000A037) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P73M	P72M	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3	P73M	Output pin setting	0: P73 pin 1: TM11IO1 pin
2	P72M	Output pin setting	0: P72 pin 1: TM11IO0 pin
1-0	-	-	-

■ Port 7 Pull-up Resistor Control Register (P7PLU: 0x0000A047) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P73R	P72R	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-2	P73R to P72R	Pull-up resistor selection	0: Not added 1: Added
1-0	-	-	-

■ Port 8 Output Register (P8OUT: 0x0000A008) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P83O	P82O	P81O	P80O
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-0	P83O to P80O	Output data	Output data

■ Port 8 Input Register (P8IN: 0x0000A018) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P83I	P82I	P81I	P80I
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-4	Reserved	-	-
3-0	P83I to P80I	Input data	Input data

■ Port 8 I/O Control Register (P8DIR: 0x0000A028) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P83D	P82D	P81D	P80D
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-0	P83D to P80D	I/O mode selection	0: Input mode 1: Output mode

■ Port 8 Pull-up Resistor Control Register (P8PLU: 0x0000A048) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	P83R	P82R	P81R	P80R
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-4	Reserved	-	Write "0"
3-0	P83R to P80R	Pull-up resistor selection	0: Not added 1: Added

■ Port 9 Output Register (P9OUT: 0x0000A009) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P97O	P96O	P95O	P94O	P93O	P92O	P91O	P90O
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P97O to P90O	Output data	Output data

■ Port 9 Input Register (P9IN: 0x0000A019) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P97I	P96I	P95I	P94I	P93I	P92I	P91I	P90I
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-0	P97I to P90I	Input data	Input data

■ Port 9 I/O Control Register (P9DIR: 0x0000A029) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P97D	P96D	P95D	P94D	P93D	P92D	P91D	P90D
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P97D to P90D	I/O mode selection	0: Input mode 1: Output mode

■ Port 9 Output Mode Register (P9MD: 0x0000A039) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P97M	P96M	P95M	P94M	P93M	P92M	P91M	P90M
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	P97M	Output pin setting	0: P97 pin 1: ADIN07 pin
6	P96M	Output pin setting	0: P96 pin 1: ADIN06 pin
5	P95M	Output pin setting	0: P95 pin 1: ADIN05 pin
4	P94M	Output pin setting	0: P94 pin 1: ADIN04 pin
3	P93M	Output pin setting	0: P93 pin 1: ADIN03 pin
2	P92M	Output pin setting	0: P92 pin 1: ADIN02 pin
1	P91M	Output pin setting	0: P91 pin 1: ADIN01 pin
0	P90M	Output pin setting	0: P90 pin 1: ADIN00 pin

■ Port 9 Pull-up Resistor Control Register (P9PLU: 0x0000A049) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	P97R	P96R	P95R	P94R	P93R	P92R	P91R	P90R
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	P97R to P90R	Pull-up resistor selection	0: Not added 1: Added

■ Port A Output Register (PAOUT: 0x0000A00A) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	PA7O	PA6O	PA5O	PA4O	PA3O	PA2O	PA1O	PA0O
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	PA7O to PA0O	Output data	Output data

■ Port A Input Register (PAIN: 0x0000A01A) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	PA7I	PA6I	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7-0	PA7I to PA0I	Input data	Input data

■ Port A I/O Control Register (PADIR: 0x0000A02A) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	PA7D	PA6D	PA5D	PA4D	PA3D	PA2D	PA1D	PA0D
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	PA7D to PA0D	I/O mode selection	0: Input mode 1: Output mode

■ Port A Output Mode Register (PAMD: 0x0000A03A) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	PA7M	PA6M	PA5M	PA4M	PA3M	PA2M	PA1M	PA0M
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	PA7M	Output pin setting	0: PA7 pin 1: ADIN15 pin
6	PA6M	Output pin setting	0: PA6 pin 1: ADIN14 pin
5	PA5M	Output pin setting	0: PA5 pin 1: ADIN13 pin
4	PA4M	Output pin setting	0: PA4 pin 1: ADIN12 pin
3	PA3M	Output pin setting	0: PA3 pin 1: ADIN11 pin
2	PA2M	Output pin setting	0: PA2 pin 1: ADIN10 pin
1	PA1M	Output pin setting	0: PA1 pin 1: ADIN09 pin
0	PA0M	Output pin setting	0: PA0 pin 1: ADIN08 pin

■ Port A Pull-up Resistor Control Register (PAPLU: 0x0000A04A) [8-bit access register]

bp	7	6	5	4	3	2	1	0
Flag	PA7R	PA6R	PA5R	PA4R	PA3R	PA2R	PA1R	PA0R
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7-0	PA7R to PA0R	Pull-up resistor selection	0: Not added 1: Added

7.3 Ports

7.3.1 Description (Port 1)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 1 I/O control register (P1DIR). The control flag of the P1DIR register is set to “1” for output mode and to “0” for input mode.

To read input data of a pin, set the control flag of the P1DIR to “0” and read the value of the port 1 input register (P1IN).

To output data to a pin, set the control flag of the P1DIR register to “1” and write data to the port 1 output register (P1OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 1 pull-up control register (P1PLU). Set the control flag of the P1PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P10 to P14 are used as external interrupt pins as well.

P16 is used as an I/O pin of timer 17 as well. Each bit can be selected individually as output mode by the port 1 output mode register (P1MD). P16 outputs special function data when the control flag of the P1MD is “1”and is used as a general port when it is “0”.

P17 is used as a serial 2 output pin as well. It is an output pin for the serial 2 and UART2 transmission data. When the SC2SBOS flag of the serial interface 2 mode register 1 (SC2CTR1) and the P17M flag of the port 1 output mode register (P1MD) are set to “1”, P17 becomes an output pin for the serial data.

7.3.2 Description (Port 2)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 2 I/O control register (P2DIR). The control flag of the P2DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P2DIR register to “0” and read the value of the port 2 input register (P2IN).

To output data to a pin, set the control flag of the P2DIR register to “1” and write data to the port 2 output register (P2OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 2 pull-up control register (P2PLU). Set the control flag of the P2PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P20 to P21 are used as serial 2 I/O pins as well. P20 is an I/O pin for the serial 2 clock. When the SC2SBTS flag of the serial interface 2 mode register 1 (SC2CTR1) and the P20M flag of the port 2 output mode register (P2MD) are set to “1”, P20 becomes an I/O pin for serial clock. P21 is an input pin for the serial 2 and UART 2 reception data. When the SC2SBIS flag of the SC2CTR1 register is set to “1” , P21 becomes an input pin for the serial data.

P22 to P24 are used as serial 1 I/O pins as well. P22 is an output pin for the serial 1 and UART 1 transmission data. When the P22M flag of the P2MD register is set to “1”, P22 becomes an output pin for the serial data. When the P22M flag of the P2MD register is set to “1”, P23 becomes an I/O pin for serial clock. P24 is an input pin for the serial 1 and UART 1 reception data.

P25 to P27 are used as serial 0 I/O pins as well. P25 is an output pin for the serial 0 and UART 0 transmission data. When the 25M flag of the P2MD register is set to “1”, P25 becomes an output pin for the serial data. When the P26 flag of the P2MD register is set to “1”, P26 becomes an I/O pin for serial clock. P27 is an input pin for the serial 0 and UART 0 reception data.

7.3.3 Description (Port 3)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 3 I/O control register (P3DIR). The control flag of the P3DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P3DIR register to “0” and read the value of the port 3 input register (P3IN).

To output data to a pin, set the control flag of the P3DIR register to “1” and write data to the port 3 output register (P3OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 3 pull-up control register (P3PLU). Set the control flag of the P3PLU to “1” to add pull-up resistor.

■ Special Function Pin Setup

P30 to P35 are used as I/O pins of timer 0 to 5 as well. Each bit can be selected individually as output mode by port 3 output mode register (P3MD). P30 to P35 output special function data when the control flag of the P3MD is “1”and are used as general ports when it is “0”.

P36 to P37 are used as I/O pins of timer 8 as well. Each bit can be selected individually as output mode by port 3 output mode register (P3MD). P36 to P37 output special function data when the control flag of the P3MD is “1”and are used as general ports when it is “0”.

7.3.4 Description (Port 4)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 4 I/O control register (P4DIR). The control flag of the P4DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P4DIR register to”1” and read the value of the port 4 input register (P4IN).

To output data to a pin, set the control flag of the P4DIR register to “1” and write data to the port 4 output register (P4OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 4 pull-up control register (P4PLU). Set the control flag of the P4PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P42 to P43, P46 to P47 are used as I/O pins of timer 9 and 10 as well. Each bit can be selected individually as output mode by the port 4 output mode register (P4MD). P42 to P43, P46 to P47 output special function data when the control flag of the P4MD is “1”and are used as general ports when it is “0”

7.3.5 Description (Port 5)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 5 I/O control register (P5DIR). The control flag of the P5DIR is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P5DIR register to “0” and read the value of the port 5 input register (P5IN).

To output data to a pin, set the control flag of the P5DIR register to “1”, and write data to the port 2 output register (P5OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 5 pull-up control register (P5PLU). Set the control flag of the P5PLU register to “1” to add the pull-up resistor.

■ Special Function Pin Setup

P51 is used as an I/O pin of timer 7 as well. Each bit can be selected individually as output mode by the port 5 output mode register (P5MD). P51 outputs special function data when the control flag of the P5MD is“1”and is used as an general port when it is “0”.

P52 to P57 are used as PWM0 output pins as well. Each bit can be selected individually as output mode by the port 5 output mode register (P5MD). P52 to P57 output special function data when the control flag of the P5MD is“1”and are used as general ports when it is “0”.

7.3.6 Description (Port 6)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 6 I/O control register (P6DIR). The control flag of the P6DIR is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P6DIR register to “0” and read the value of the port 6 input register (P6IN).

To output data to a pin, set the control flag of the P6DIR register to “1” and write data to the port 6 output register (P6OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 6 pull-up control register (P6PLU). Set the control flag of the P6PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P62 to P67 are used as PWM1 output pins as well. Each bit can be selected individually as output mode by the port 6 output mode register (P6MD). P62 to P67 output special function data when the control flag of the P6MD is“1”and are used as general ports when it is “0”.

7.3.7 Description (Port 7)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 7 I/O control register (P7DIR). The control flag of the P7DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P7DIR register to “0” and read the value of the port 7 input register (P7IN).

To output data to a pin, set the control flag of the P7DIR register to “1” and write data to the port 7 output register (P7OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 7 pull-up control register (P7PLU). Set the control flag of the P7PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P72 to P73 are used as I/O pins of timer 11 as well. Each bit can be selected individually as output mode by the port 7 output mode register (P7MD). P72 to P73 output special function data when the control flag of the P7MD is“1”and are used as general ports when it is “0”.

7.3.8 Description (Port 8)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 8 I/O control register (P8DIR). The control flag of the P8DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P8DIR register to “0” and read the value of the port 8 input register (P8IN).

To output data to a pin, set the control flag of the P8DIR register to “1” and write data to the port 8 output register (P8OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 8 pull-up control register (P8PLU). Set the control flag of the P8PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P80 to P83 are used as external interrupt pins as well.

7.3.9 Description (Port 9)

■ General Port Setup

Each bit can be set individually as either an input or output by the port 9 I/O control register (P9DIR). The control flag of the P9DIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the P9DIR register to “0” and read the value of the port 9 input register (P9IN).

To output data to a pin, set the control flag of the P9DIR register to “1” and write data to the port 9 output register (P9OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 9 pull-up control register (P9PLU). Set the control flag of the P9PLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

P90 to P97 are used as analog input pins as well. Each bit can be selected individually as input mode by the port 9 output mode register (P9MD). P90 to P97 are analogue pins when the control flag of the P9MD is“1” and are used as general ports when it is “0”.

7.3.10 Description (Port A)

■ General Port Setup

Each bit can be set individually as either an input or output by the port A I/O control register (PADIR). The control flag of the PADIR register is set to “1” for output mode, and to “0” for input mode.

To read input data of a pin, set the control flag of the PADIR register to “0” and read the value of the port A input register (PAIN).

To output data to a pin, set the control flag of the PADIR register to “1” and write data to the port A output register (PAOUT).

Each bit can be set individually if pull-up resistor is added or not, by the port A pull-up control register (PAPLU). Set the control flag of the PAPLU register to “1” to add pull-up resistor.

■ Special Function Pin Setup

PA0 to PA7 are used as analogue input pins as well. Each bit can be selected individually as input mode by the port A output mode register (PAMD). PA0 to PA7 are analogue pins when the control flag of the PAMD is“1” and are used as general ports when it is “0”.

Chapter 8 8-bit Timer

8

8.1 Overview

This LSI contains 12 general purpose 8-bit timers (timer 0 to timer 7, timer14 to timer17).

Timer 14 to timer16 can be used as baud rate timers of serial interface.

8.1.1 Functions

Table:8.1.1 shows functions that can be used with each timer.

Table:8.1.1 Timer Functions

	Timer 0	Timer 1	Timer 2	Timer 3	Pages
Interrupt cause	NTMIRQ0	NTMIRQ1	NTMIRQ2	NTMIRQ3	-
Interval timer	○	○	○	○	VIII-32
Timer output	-	○	○	○	VIII-36
Event count	-	○	○	○	VIII-38
Baud rate timer	-	-	-	-	VIII-32
Cascade connection	-	Connect with timer 0	Connect with timer 1	Connect with timer 2	VIII-40
Counter source	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 1 underflow Timer 2 underflow	IOCLK IOCLK/8 IOCLK/32 Timer 0 underflow Timer 2 underflow TM1IO pin input Cascading with timer 0	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 0 underflow Timer 1 underflow TM2IO pin input Cascading with timer 1	IOCLK IOCLK/8 IOCLK/32 Timer 0 underflow Timer 1 underflow Timer 2 underflow TM3IO pin input Cascading with timer 2	VIII-32

	Timer 4	Timer 5	Timer 6	Timer 7	Page
Interrupt cause	NTMIRQ4	NTMIRQ5	NTMIRQ6	NTMIRQ7	-
Interval timer	○	○	○	○	VIII-32
Timer output	○	○	-	○	VIII-36
Event count	○	○	-	○	VIII-38
Baud rate timer	-	-	-	-	VIII-32
Cascade connection	-	Connect with timer 4	Connect with timer 5	Connect with timer 6	VIII-40
Counter source	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 5 underflow Timer 6 underflow TM4IO pin input	IOCLK IOCLK/8 IOCLK/32 Timer 4 underflow Timer 6 underflow TM5IO pin input Cascading with timer 4	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 4 underflow Timer 5 underflow Cascading with timer 5	IOCLK IOCLK/8 IOCLK/32 Timer 4 underflow Timer 5 underflow Timer 6 underflow TM7IO pin input Cascading with timer 6	VIII-32

	Timer 14	Timer 15	Timer 16	Timer 17	Page
Interrupt cause	NTMIRQ14	NTMIRQ15	NTMIRQ16	NTMIRQ17	-
Interval timer	○	○	○	○	VIII-32
Timer output	-	-	-	○	VIII-36
Event count	-	-	-	○	VIII-38
Baud rate timer	○	○	○	-	VIII-32
Cascade connection	-	Connect with timer 14	Connect with timer 15	Connect with timer 16	VIII-40
Counter source	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 15 underflow Timer 16 underflow	IOCLK IOCLK/8 IOCLK/32 Timer 14 underflow Timer 16 underflow Cascading with timer 14	IOCLK IOCLK/8 IOCLK/32 IOCLK/128 Timer 14 underflow Timer 15 underflow Cascading with timer 15	IOCLK IOCLK/8 IOCLK/32 Timer 14 underflow Timer 15 underflow Timer 16 underflow TM17IO pin input Cascading with timer 16	VIII-32

8.1.2 Connection Diagram

■ 8-bit Timer Connection Diagram (Timer 0 to 3)

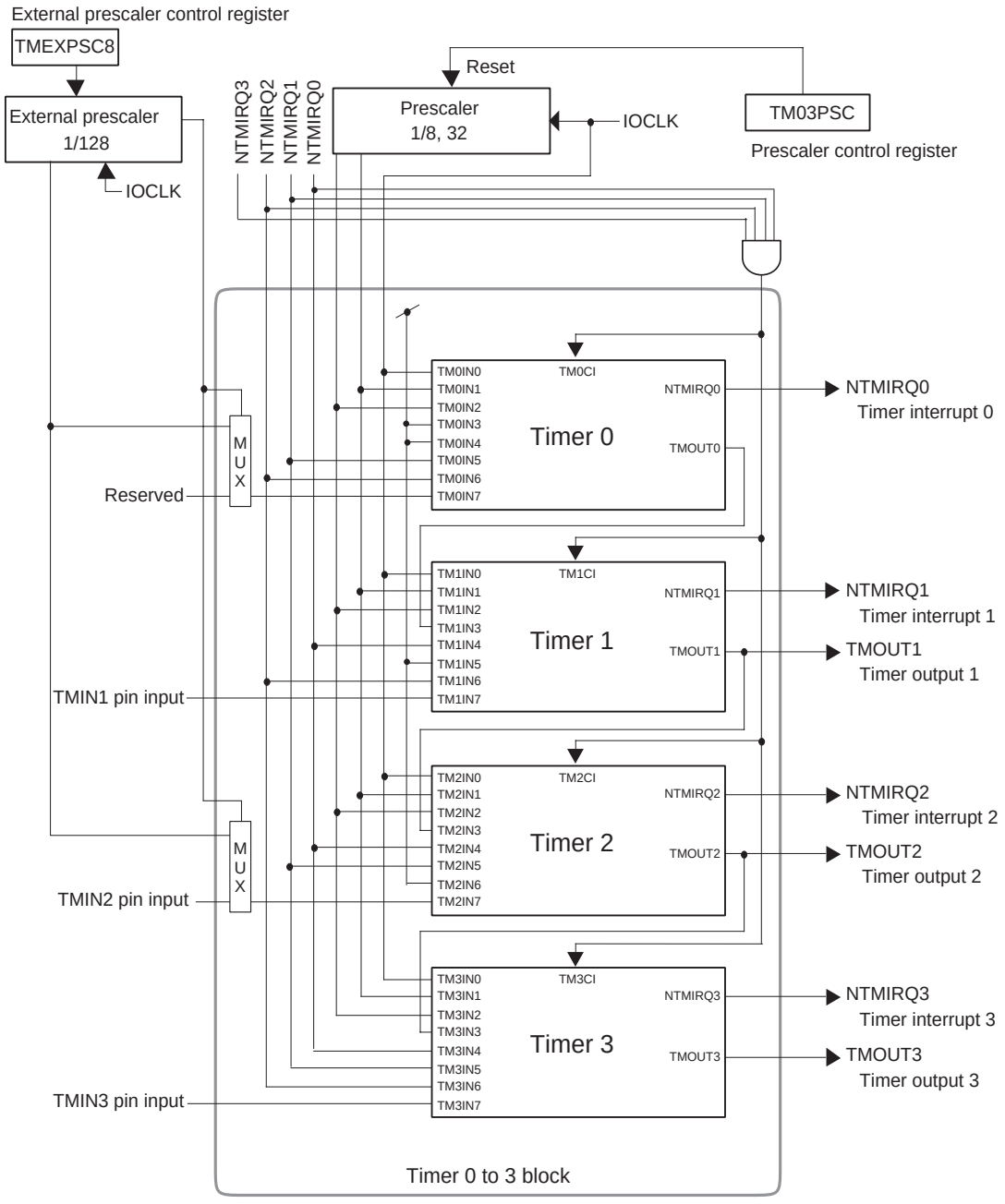


Figure:8.1.1 8-bit Timer Connection Diagram (Timer 0 to 3)

■ 8-bit Timer Connection Diagram (Timer 4 to 7)

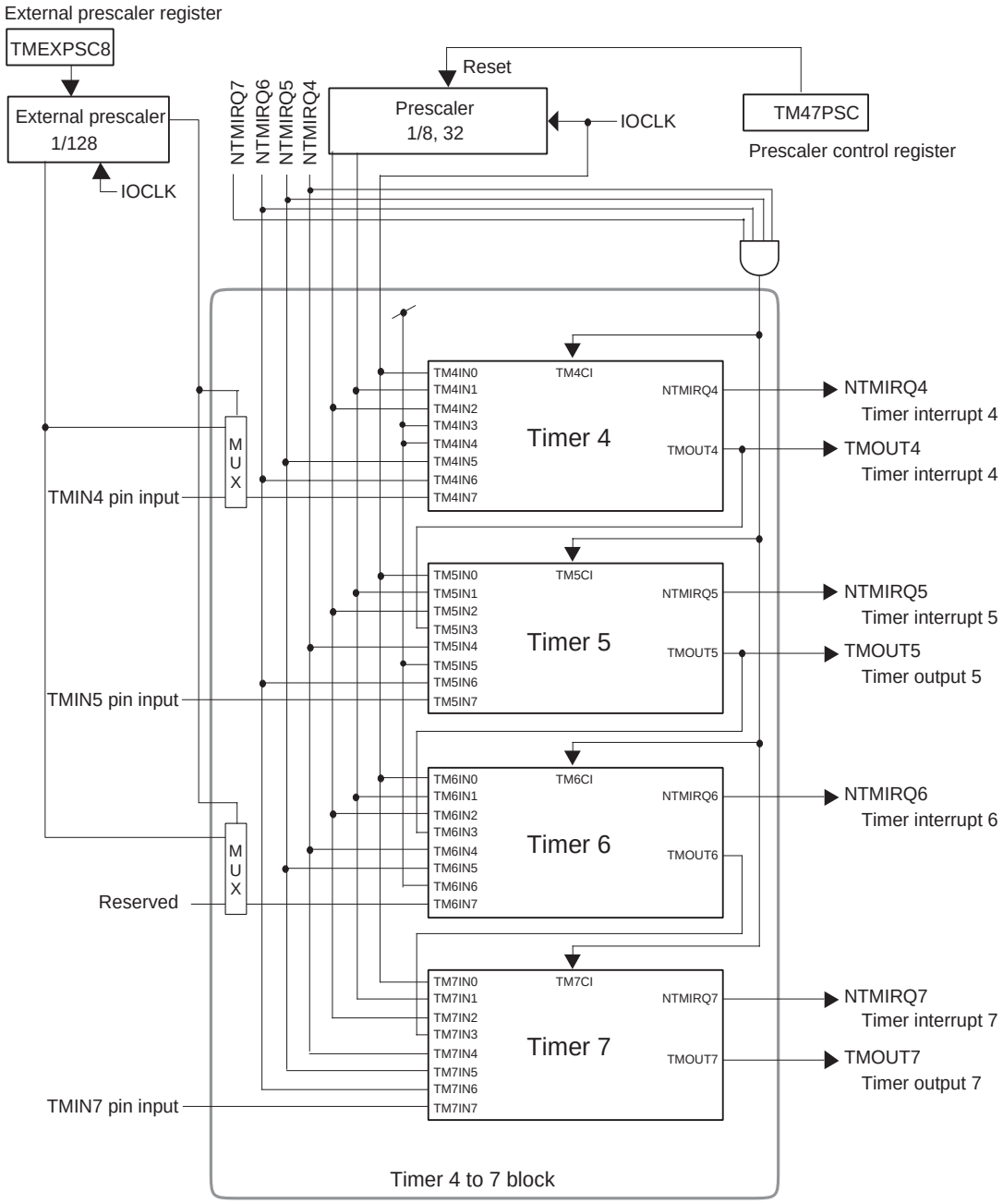


Figure:8.1.2 8-bit Timer Connection Diagram (Timer 4 to 7)

■ 8-bit Timer Connection Diagram (Timer 14 to 17)

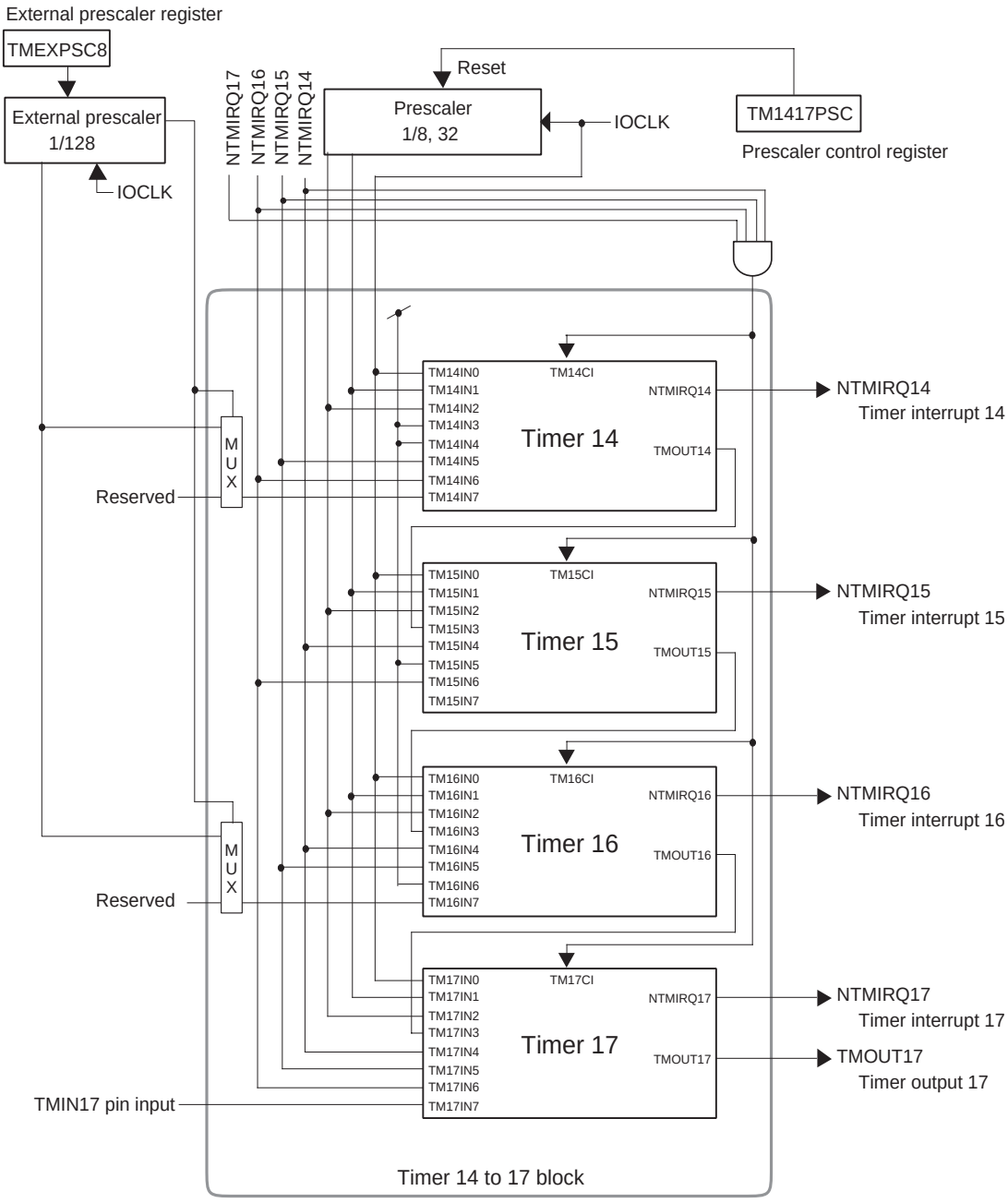


Figure:8.1.3 8-bit Timer Connection Diagram (Timer 14 to 17)

8.1.3 Block Diagram

■ 8-bit Timer Block Diagram

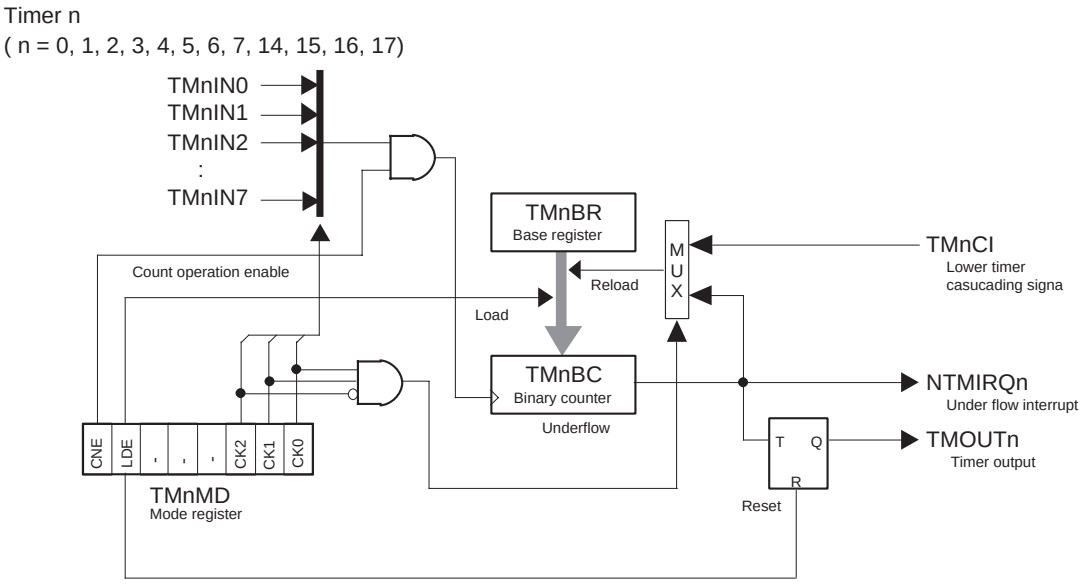


Figure:8.1.4 8-bit Timer Block Diagram

8.2 Control Registers

Timer 0 to timer 7 and timer 14 to timer 17 consist of the binary counter (TMnBC) and the base register (TMnBR), and are controlled by the mode register (TMnMD). When the prescaler output is selected as the count clock source of timer 0 to 7, they should be controlled by the prescaler control register.

8.2.1 Registers

Table: 8.2.1 shows registers that control 8-bit timers.

Table:8.2.1 8-bit Timer Control Registers

	Register	Address	R/W	Access size	Function	Page
Prescaler	TM03PSC	0x0000A198	R/W	8,16	Prescaler control register 1	VIII-11
	TM47PSC	0x0000A1B8	R/W	8,16	Prescaler control register 2	VIII-11
	TM1417PSC	0x0000A1D8	R/W	8,16	Prescaler control register 3	VIII-11
	TMEXPSC8	0x0000A19C	R/W	8,16	External prescaler control register 0	VIII-12
Timer 0	TM0BR	0x0000A188	R/W	8	Timer 0 base register	VIII-13
	TM0BC	0x0000A190	R	8	Timer 0 binary counter	VIII-15
	TM0MD	0x0000A180	R/W	8	Timer 0 mode register	VIII-18
	G3ICR	0x0000890C	R/W	8,16	Group 3 interrupt control register	V-15
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
Timer 1	TM1BR	0x0000A189	R/W	8	Timer 1 base register	VIII-13
	TM1BC	0x0000A191	R	8	Timer 1 binary counter	VIII-15
	TM1MD	0x0000A181	R/W	8	Timer 1 mode register	VIII-19
	G3ICR	0x0000890C	R/W	8,16	Group 3 interrupt control register	V-15
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
Timer 2	TM2BR	0x0000A18C	R/W	8	Timer 2 base register	VIII-13
	TM2BC	0x0000A194	R	8	Timer 2 binary counter	VIII-16
	TM2MD	0x0000A184	R/W	8	Timer 2 mode register	VIII-20
	G4ICR	0x00008910	R/W	8,16	Group 4 interrupt control register	V-16
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
Timer 3	TM3BR	0x0000A18D	R/W	8	Timer 3 base register	VIII-13
	TM3BC	0x0000A195	R	8	Timer 3 binary counter	VIII-16
	TM3MD	0x0000A185	R/W	8	Timer 3 mode register	VIII-21
	G4ICR	0x00008910	R/W	8,16	Group 4 interrupt control register	V-16
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15

	Register	Address	R/W	Access size	Function	Page
Timer 4	TM4BR	0x0000A1A8	R/W	8	TImer 4 base register	VIII-14
	TM4BC	0x0000A1B0	R	8	Timer 4 binary counter	VIII-16
	TM4MD	0x0000A1A0	R/W	8	Timer 4 mode register	VIII-22
	G5ICR	0x00008914	R/W	8,16	Group 5 interrupt control register	V-16
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
Timer 5	TM5BR	0x0000A1A9	R/W	8	Timer 5 base register	VIII-14
	TM5BC	0x0000A1B1	R	8	Timer 5 binary counter	VIII-16
	TM5MD	0x0000A1A1	R/W	8	Timer 5 mode register	VIII-23
	G5ICR	0x00008914	R/W	8,16	Group 5 interrupt control register	V-16
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-13
Timer 6	TM6BR	0x0000A1AC	R/W	8	Timer 6 base register	VIII-14
	TM6BC	0x0000A1B4	R	8	Timer 6 binary counter	VIII-16
	TM6MD	0x0000A1A4	R/W	8	Timer 6 mode register	VIII-24
	G6ICR	0x00008918	R/W	8,16	Group 6 interrupt control register	V-17
	P5MD	0x0000A035	R/W	8	Port 5 output mode register	VII-21
	P5DIR	0x0000A025	R/W	8	Port 5 I/O control register	VII-20
Timer 7	TM7BR	0x0000A1AD	R/W	8	Timer 7 base register	VIII-14
	TM7BC	0x0000A1B5	R	8	Timer 7 binary counter	VIII-17
	TM7MD	0x0000A1A5	R/W	8	Timer 7 mode register	VIII-25
	G6ICR	0x00008918	R/W	8,16	Group 6 interrupt control register	V-17
	P5MD	0x0000A035	R/W	8	Port 5 output mode register	VII-21
	P5DIR	0x0000A025	R/W	8	Port 5 I/O control register	VII-20
Timer 14	TM14BR	0x0000A1C8	R/W	8	Timer 14 base register	VIII-14
	TM14BC	0x0000A1D0	R	8	Timer 14 binary counter	VIII-17
	TM14MD	0x0000A1C0	R/W	8	Timer 14 mode register	VIII-26
	G29ICR	0x00008974	R/W	8,16	Group 29 interrupt control register	V-31
	P8DIR	0x0000A028	R/W	8	Port 8 I/O control register	VII-26
Timer 15	TM15BR	0x0000A1C9	R/W	8	Timer 15 base register	VIII-15
	TM15BC	0x0000A1D1	R	8	Timer 15 binary counter	VIII-17
	TM15MD	0x0000A1C1	R/W	8	Timer 15 mode register	VIII-27
	G29ICR	0x00008974	R/W	8,16	Group 29 interrupt control register	V-31
	P8DIR	0x0000A028	R/W	8	Port 8 I/O control register	VII-26
Timer 16	TM16BR	0x0000A1CC	R/W	8	Timer 16 base register	VIII-15
	TM16BC	0x0000A1D4	R	8	Timer 16 binary counter	VIII-17
	TM16MD	0x0000A1C4	R/W	8	Timer 16 mode register	VIII-28
	G30ICR	0x0000897B	R/W	8,16	Group 30 interrupt control register	V-31
	P1MD	0x0000A031	R/W	8	Port 1 output mode register	VII-11
	P1DIR	0x0000A021	R/W	8	Port 1 I/O control register	VII-11

	Register	Address	R/W	Access size	Function	Page
Timer 17	TM17BR	0x0000A1CD	R/W	8	Timer 17 base register	VIII-15
	TM17BC	0x0000A1D5	R	8	Timer 17 binary counter	VIII-17
	TM17MD	0x0000A1C5	R/W	8	Timer 17 mode register	VIII-29
	G30ICR	0x0000897B	R/W	8,16	Group 30 interrupt control register	V-31
	P1MD	0x0000A031	R/W	8	Port 1 output mode register	VII-11
	P1DIR	0x0000A021	R/W	8	Port 1 I/O control register	VII-11

R/W Readable / Writable
R Readable only
W Writable only

8.2.2 Prescaler Control Registers

When the prescaler output is selected as the count clock source for 8-bit timer, these registers should be controlled.

■ Prescaler Control Register 1 (TM03PSC : 0x0000A198) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TMPSCNE1	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7	TMPSCNE1	Prescaler 1 operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Prescaler Control Register 2 (TM47PSC: 0x0000A1B8) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TMPSCNE2	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7	TMPSCNE2	Prescaler 2 operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Prescaler Control Register 3 (TM1417PSC: 0x0000A1D8) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TMPSCNE3	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Set condition
7	TMPSCNE3	Prescaler 3 operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ External Prescaler Control Register 0 (TMEXPSC8 : 0x0000A19C) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	TM16IN	TM14IN	TM6IN	TM4IN	TM2IN	TM0IN	EX PSCNE
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	-	-	-
6	TM16IN	Timer 16 count clock source selection	0: Can not be used 1: IOCLK/128
5	TM14IN	Timer 14count clock source selection	0: Can not be used 1: IOCLK/128
4	TM6IN	Timer 6 count clock source selection	0: Can not be used 1: IOCLK/128
3	TM4IN	Timer 4 count clock source selection	0: TM4IO pin input 1: IOCLK/128
2	TM2IN	Timer 2 count clock source selection	0: TM2IO pin input 1: IOCLK/128
1	TM0IN	Timer 0 count clock source selection	0: Can not be used 1: IOCLK/128
0	EXPSCNE	Prescaler (1/128) operation enable	0: Operation disabled 1: Operation enabled

When the count clock source is set to TMnI0 pin input or IOCLK/128, select TMnI0 pin input by the TMnCLK[2-0] flag of the timer mode register TMnMD.

8.2.3 Programmable Timer Registers

Timer 0 to timer 7,timer 14 to timer 17 each have 8-bit programmable timer registers.

Programmable timer registers consist of the base register and binary counter.

Timer n base registers set the initial value of the timer n binary counter (TMnBC) and the underflow period. The value of timer n base register (TMnBR) setting is loaded into TMnBC under the following conditions:

- when the TMnLDE flag of the timer n mode register (TMnMD) = 1
- when an underflow occurs

Timer n binary counters are 8-bit readable registers. The counter values can be read.

■ Timer 0 Base Register (TM0BR: 0x0000A188) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 1 Base Register (TM1BR: 0x0000A189) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 2 Base Register (TM2BR: 0x0000A18C) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 3 Base Register (TM3BR: 0x0000A18D) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 4 Base Register (TM4BR: 0x0000A1A8) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 5 Base Register (TM5BR: 0x0000A1A9) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 6 Base Register (TM6BR: 0x0000A1AC) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM6 BR7	TM6 BR6	TM6 BR5	TM6 BR4	TM6 BR3	TM6 BR2	TM6 BR1	TM6 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 7 Base Register (TM7BR: 0x0000A1AD) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM7 BR7	TM7 BR6	TM7 BR5	TM7 BR4	TM7 BR3	TM7 BR2	TM7 BR1	TM7 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 14 Base Register (TM14BR: 0x0000A1C8) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM14 BR7	TM14 BR6	TM14 BR5	TM14 BR4	TM14 BR3	TM14 BR2	TM14 BR1	TM14 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 15 Base Register (TM15BR: 0x0000A1C9) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM15 BR7	TM15 BR6	TM15 BR5	TM15 BR4	TM15 BR3	TM15 BR2	TM15 BR1	TM15 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 16 Base Register (TM16BR: 0x0000A1CC) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM16 BR7	TM16 BR6	TM16 BR5	TM16 BR4	TM16 BR3	TM16 BR2	TM16 BR1	TM16 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 17 Base Register (TM17BR: 0x0000A1CD) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM17 BR7	TM17 BR6	TM17 BR5	TM17 BR4	TM17 BR3	TM17 BR2	TM17 BR1	TM17 BR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 0 Binary Counter (TM0BC: 0x0000A190) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM0 BC7	TM0 BC6	TM0 BC5	TM0 BC4	TM0 BC3	TM0 BC2	TM0 BC1	TM0 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 1 Binary Counter (TM1BC: 0x0000A191) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM1 BC7	TM1 BC6	TM1 BC5	TM1 BC4	TM1 BC3	TM1 BC2	TM1 BC1	TM1 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 2 Binary Counter (TM2BC: 0x0000A194) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM2 BC7	TM2 BC6	TM2 BC5	TM2 BC4	TM2 BC3	TM2 BC2	TM2 BC1	TM2 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 3 Binary Counter (TM3BC: 0x0000A195) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM3 BC7	TM3 BC6	TM3 BC5	TM3 BC4	TM3 BC3	TM3 BC2	TM3 BC1	TM3 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 4 Binary Counter (TM4BC: 0x0000A1B0) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM4 BC7	TM4 BC6	TM4 BC5	TM4 BC4	TM4 BC3	TM4 BC2	TM4 BC1	TM4 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 5 Binary Counter (TM5BC: 0x0000A1B1) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM5 BC7	TM5 BC6	TM5 BC5	TM5 BC4	TM5 BC3	TM5 BC2	TM5 BC1	TM5 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 6 Binary Counter (TM6BC: 0x0000A1B4) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM6 BC7	TM6 BC6	TM6 BC5	TM6 BC4	TM6 BC3	TM6 BC2	TM6 BC1	TM6 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 7 Binary Counter (TM7BC: 0x0000A1B5) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM7 BC7	TM7 BC6	TM7 BC5	TM7 BC4	TM7 BC3	TM7 BC2	TM7 BC1	TM7 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 14 Binary Counter (TM14BC: 0x0000A1D0) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM14 BC7	TM14 BC6	TM14 BC5	TM14 BC4	TM14 BC3	TM14 BC2	TM14 BC1	TM14 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 15 Binary Counter (TM15BC: 0x0000A1D1) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM15 BC7	TM15 BC6	TM15 BC5	TM15 BC4	TM15 BC3	TM15 BC2	TM15 BC1	TM15 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 16 Binary Counter (TM16BC: 0x0000A1D4) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM16 BC7	TM16 BC6	TM16 BC5	TM16 BC4	TM16 BC3	TM16 BC2	TM16 BC1	TM16 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 17 Binary Counter (TM17BC: 0x0000A1D5) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM17 BC7	TM17 BC6	TM17 BC5	TM17 BC4	TM17 BC3	TM17 BC2	TM17 BC1	TM17 BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

8.2.4 Timer Mode Registers

Timer mode registers are readable/writable 8-bit registers that control timer 0 to timer 7 and timer 14 to 17.

■ Timer 0 Mode Register (TM0MD: 0x0000A180) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM0 CNE	TM0 LDE	-	-	-	TM0 CK2	TM0 CK1	TM0 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM0CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM0LDE	Timer initialization	0: Normal operation 1: Initialization TM0BR value is loaded into TM0BC.
5-3	-	-	-
2-0	TM0CK2 TM0CK1 TM0CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Setting prohibited 100: Setting prohibited 101: Timer 1 underflow 110: Timer 2 underflow 111: IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM03PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM0IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 1 Mode Register (TM1MD: 0x0000A181) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM1 CNE	TM1 LDE	-	-	-	TM1 CK2	TM1 CK1	TM1 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM1CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM1LDE	Timer initialization	0: Normal operation 1: Initialization TM1BR value is loaded into TM1BC. Timer output 1 is set to “L” level.
5-3	-	-	-
2-0	TM1CK2 TM1CK1 TM1CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 0 100: Timer 0 underflow 101: Setting prohibited 110: Timer 2 underflow 111: TM1IO pin input (rising edge) When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM03PSC) should be set.

■ Timer 2 Mode Register (TM2MD: 0x0000A184) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM2 CNE	TM2 LDE	-	-	-	TM2 CK2	TM2 CK1	TM2 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM2CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM2LDE	Timer initialization	0: Normal operation 1: Initialization TM2BR value is loaded into TM2BC. Timer output 2 is set to “L” level.
5-3	-	-	-
2-0	TM2CK2 TM2CK1 TM2CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 1 100: Timer 0 underflow 101: Timer 1 underflow 110: Setting prohibited 111: TM2IO pin input (rising edge), IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM03PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM2IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 3 Mode Register (TM3MD: 0x0000A185) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM3 CNE	TM3 LDE	-	-	-	TM3 CK2	TM3 CK1	TM3 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM3CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM3LDE	Timer initialization	0: Normal operation 1: Initialization TM3BR value is loaded into TM3BC. Timer output 3 is set to “L” level.
5-3	-	-	-
2-0	TM3CK2 TM3CK1 TM3CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 2 100: Timer 0 underflow 101: Timer 1 underflow 110: Timer 2 underflow 111: TM3IO pin input (rising edge) When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM03PSC) should be set.

■ Timer 4 Mode Register (TM4MD: 0x0000A1A0) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM4 CNE	TM4 LDE	-	-	-	TM4 CK2	TM4 CK1	TM4 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM4CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM4LDE	Timer initialization	0: Normal operation 1: Initialization TM4BR value is loaded into TM4BC. Timer output 4 is set to “L” level.
5-3	-	-	-
2-0	TM4CK2 TM4CK1 TM4CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Setting prohibited 100: Setting prohibited 101: Timer 5 underflow 110: Timer 6 underflow 111: TM4IO pin input (rising edge), IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM47PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM4IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 5 Mode Register (TM5MD: 0x0000A1A1) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM5 CNE	TM5 LDE	-	-	-	TM5 CK2	TM5 CK1	TM5 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM5CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM5LDE	Timer initialization	0: Normal operation 1: Initialization TM5BR value is loaded into TM5BC. Timer output 5 is set to “L” level.
5-3	-	-	-
2-0	TM5CK2 TM5CK1 TM5CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 4 100: Timer 4 underflow[101: Setting prohibited 110: Timer 6 underflow 111: TM5IO pin input (rising edge) When 1/8 IOCLK or 1/32 IOCLK are used, the prescaler control register (TM47PSC) should be set.

■ Timer 6 Mode Register (TM6MD: 0x0000A1A4) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM6 CNE	TM6 LDE	-	-	-	TM6 CK2	TM6 CK1	TM6 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM6CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM6LDE	Timer initialization	0: Normal operation 1: Initialization TM6BR value is loaded into TM6BC.
5-3	-	-	-
2-0	TM6CK2 TM6CK1 TM6CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 5 100: Timer 4 underflow 101: Timer 5 underflow 110: Setting prohibited 111: IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM47PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM6IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 7 Mode Register (TM7MD: 0x0000A1A5) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM7 CNE	TM7 LDE	-	-	-	TM7 CK2	TM7 CK1	TM7 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM7CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM7LDE	Timer initialization	0: Normal operation 1: Initialization TM7BR value is loaded into TM7BC. Timer output 7 is set to “L” level.
5-3	-	-	-
2-0	TM7CK2 TM7CK1 TM7CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 6 100: Timer 4 underflow[101: Timer 5 underflow 110: Timer 6 underflow 111: TM7IO pin input (rising edge) When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM47PSC) should be set.

■ Timer 14 Mode Register (TM14MD: 0x0000A1C0) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM14 CNE	TM14 LDE	-	-	-	TM14 CK2	TM14 CK1	TM14 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM14CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM14LDE	Timer initialization	0: Normal operation 1: Initialization TM14BR value is loaded into TM14BC.
5-3	-	-	-
2-0	TM14CK2 TM14CK1 TM14CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Setting prohibited 100: Setting prohibited 101: Timer 15 underflow 110: Timer 16 underflow 111: IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM1417PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM14IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 15 Mode Register (TM15MD: 0x0000A1C1) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM15 CNE	TM15 LDE	-	-	-	TM15 CK2	TM15 CK1	TM15 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM15CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM15LDE	Timer initialization	0: Normal operation 1: Initialization TM15BR value is loaded into TM15BC.
5-3	-	-	-
2-0	TM15CK2 TM15CK1 TM15CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 14 100: Timer 14 underflow 101: Setting prohibited 110: Timer 16 underflow 111: Setting prohibited When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM1417PSC) should be set.

■ Timer 16 Mode Register (TM16MD: 0x0000A1C4) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM16 CNE	TM16 LDE	-	-	-	TM16 CK2	TM16 CK1	TM16 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM16CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM16LDE	Timer initialization	0: Normal operation 1: Initialization TM16BR value is loaded into TM16BC.
5-3	-	-	-
2-0	TM16CK2 TM16CK1 TM16CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 15 100: Timer 14 underflow 101: Timer 15 underflow 110: Setting prohibited 111: IOCLK/128 When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM1417PSC) should be set.

When the count clock source is set to IOCLK/128, set the TM16IN flag of the external prescaler control register TMEXPSC8 to “1” and the EXPSCNE flag to “ 1”.

■ Timer 17 Mode Register (TM17MD: 0x0000A1C5) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM17 CNE	TM17 LDE	-	-	-	TM17 CK2	TM17 CK1	TM17 CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Set condition
7	TM17CNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TM17LDE	Timer initialization	0: Normal operation 1: Initialization TM17BR value is loaded into TM17BC. Timer output 17 is set to “L” level.
5-3	-	-	-
2-0	TM17CK2 TM17CK1 TM17CK0	Count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/32 011: Cascading with timer 16 100: Timer 14 underflow 101: Timer 15 underflow 110: Timer 16 underflow 111: TM17IO pin input (rising edge) When 1/8 IOCLK and 1/32 IOCLK are used, the prescaler control register (TM1417PSC) should be set.

8.3 Prescaler

8.3.1 Prescaler Operation

■ Prescaler Operation

Prescaler outputs 1/8, 1/32, and 1/128 dividing clock with using IOCLK as an input clock.

■ Count Clock Source and Prescaler

When selecting IOCLK/8, IOCLK/32, or IOCLK/128 to count clock source of timer, the prescaler should be set up. The following table shows the relationship between count clock sources and controlled registers.

When setting a count clock source to 128 dividing, set count clock source selection of the timer mode register (TM0MD, TM2MD, TM4MD, TM6MD, TM14MD and TM16MD) to IOCLK/128 of “111”.

Table:8.3.1 Count Clock Source and Prescaler

Count clock source	Prescaler setting	Register to be set up
IOCLK (Timer 0 to 7, 14 to 17)	-	-
IOCLK/8 (Timer 0 to 3)	Need	TM03PSC
IOCLK/8 (Timer 4 to 7)	Need	TM47PSC
IOCLK/8 (Timer 14 to 17)	Need	TM1417PSC
IOCLK/32 (Timer 0 to 3)	Need	TM03PSC
IOCLK/32 (Timer 4 to 7)	Need	TM47PSC
IOCLK/32 (Timer 14 to 17)	Need	TM1417PSC
IOCLK/128 (Timer 0,2,4,6,14,16)	Need	TMEXPSC8
Timer n underflow	-	-
TMnIO pin input	-	-

8.3.2 Setup Example

■ Prescaler Setup Example

Count clock source (IOCLK/32) which is output from the prescaler is selected to the count clock of the timer 0.

A setup procedure with a description of each step is shown below:

Setup Procedure	Description
(1) Stop the counter TM0MD(0x0000A180) bp6: TM0LDE=0 bp7: TM0CNE=0	(1) Set the TM0LDE flag and TM0CNE flag of timer 0 mode register (TM0MD) to"0" to stop counting of timer 0.
(2) Set the base register TM0BR(0x0000A188)	(2) Set timer 0 base register (TM0BR) as needed.
(3) Set the prescaler TM03PSC(0x0000A198) bp7: TMPSCNE=1	(3) Set the TMPSCNE flag of the prescaler control register (TM03PSC) to "1".
(4) Select the count clock source TM0MD(0x0000A180) bp2-0: TM0CK2-0=010	(4) Select the count clock source (IOCLK/32) by the TM0CK2 to 0 flag of the TM0MD register.
(5) Initialize timer 0 TM0MD(0x0000A180) bp6: TM0LDE=1	(5) Set the TM0LDE flag of the TM0MD register to "1" to initialize timer 0. The value of theTM0BR register is loaded into the TM0BC counter. After setting, reset the TM0LDE flag to "0".
(6) Start timer operation TM0MD(0x0000A180) bp7: TM0CNE=1	(6) Set the TM0CNE flag of the TM0MD register to "1" to operate timer 0.

8.4 Interval Timer

8.4.1 Interval Timer Operation

Interval timer function is the function that can constantly generate interrupts at regular time intervals.

■ Clock Source Selection

The generation cycle of timer interrupts is set in advance by the clock source selection and the setting value of the base register (TMnBR). The clock source can be selected by the timer as below.

Table:8.4.1 The Clock Source at the Timer Operating and 1 Count Time‘

Clock source	1 count time	Timer 0	Time 1	Timer 2	Timer 3
IOCLK	33ns	O	O	O	O
IOCLK/8	267ns	O	O	O	O
IOCLK/32	1.07µs	O	O	O	O
IOCLK/128	4.27µs	O	-	O	-
Timer 0 underflow	-	-	O	O	O
Timer 1 underflow	-	O	-	O	O
Timer 2 underflow	-	O	O	-	O
1 count time is calculated with 10MHz, 6 multiplication and IOCLK=MCLK/2.					

Clock source	1 count time	Timer 4	Timer 5	Timer 6	Timer 7
IOCLK	33ns	O	O	O	O
IOCLK/8	267ns	O	O	O	O
IOCLK/32	1.07µs	O	O	O	O
IOCLK/128	4.27µs	O	-	O	-
Timer 4 underflow	-	-	O	O	O
Timer 5 underflow	-	O	-	O	O
Timer 6 underflow	-	O	O	-	O
1 count time is calculated with 10MHz, 6 multiplication and IOCLK=MCLK/2.					

Clock source	1 count time	Timer 14	Timer 15	Timer 16	Timer 17
IOCLK	33ns	O	O	O	O
IOCLK/8	267ns	O	O	O	O
IOCLK/32	1.07µs	O	O	O	O
IOCLK/128	4.27µs	O	-	O	-
Timer 14 underflow	-	-	O	O	O
Timer 15 underflow	-	O	-	O	O
Timer 16 underflow	-	O	O	-	O
1 count time is calculated with 10MHz, 6 multiplication and IOCLK=MCLK/2.					

■ Setting a Timer Base Register

Set the generation cycle of a timer interrupt to the base register TMnBR.

$$\text{Timer interrupt} = (\text{TMnBR setting} + 1) \times \text{Count clock source cycle}$$

■ Count Timing of Timer Operation

The binary counter counts down with the selected count source as a count clock. The basic operation of the whole function of 8-bit timer is as follows:

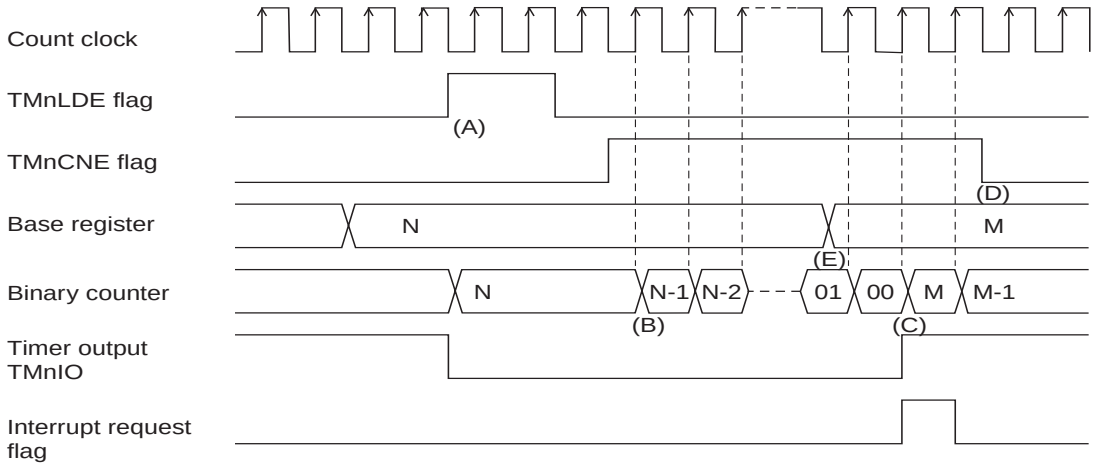


Figure:8.4.1 Count Timing of Timer Operation (1)

(A) When initialization (“1”) is written to the TMnLDE flag, the value of the base register is loaded into the binary counter and the timer output (TMnIO) is reset to “L”. Reset the TMnLDE flag to “0” after setting.

(B) When setting the TMnCNE flag to operation enabled (“1”), the binary counter starts to count down. The count is operated at the rising edge of the count clock.

(C) The underflow interrupt request is generated at the binary counter underflow. The value of the base register is loaded into the binary counter and counting down restarts. The timer output (TMnIO) changes from “L” to “H”.

(D) When the TMnCNE flag is set to operation disabled (“0”), counting down is stopped. The statuses of the binary counter and the timer output (TMnIO) are retained after the timer is stopped, unless the TMnCNE flag is set to be initialized (“1”). The counting down operation can be resumed from the statuses before the timer was stopped if the TMnCNE is set to (“1”).

(E) When the value of the base register is changed during the counting down operation, the value is loaded into the binary counter as initial value at the next underflow generation.

Set TMnLDE to “0” before manipulating the TMnLDE flag.

■ Count Timing When the Underflow of Timer is Selected to the Count Source

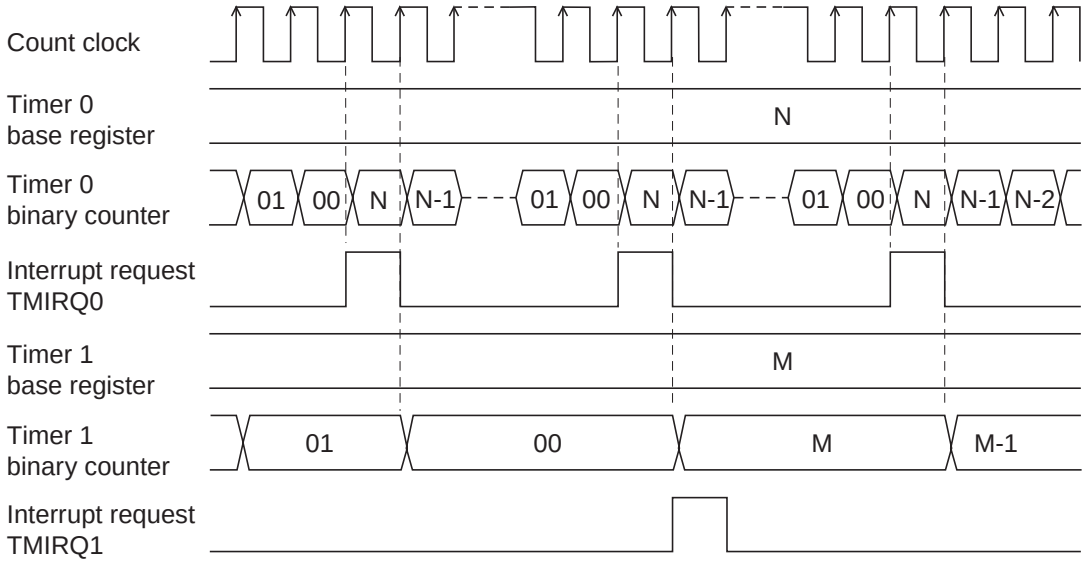


Figure:8.4.2 Count Timing of Timer Operation (2)

8.4.2 Setup Example

■ Interval Timer Setup Example

Timer function can be set by using timer 0 that generates the constant interrupts. Interrupts are generated every 150 dividing (5µs) by selecting the clock source IOCLK. The oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2.

A setup procedure with a description of each step is shown below:

Setup Procedure	Description
(1) Stop the counter TM0MD(0x0000A180) bp6: TM0LDE=0 bp7: TM0CNE=0	(1) Set the TM0LDE flag and TM0CNE flag of timer 0 mode register (TM0MD) to “0” to stop counting of timer 0.
(2) Disable an interrupt G3ICR(0x0000890C) bp8: G3IE0=0	(2) Set the G3IEO flag of the G3ICR register to “0” to disable an interrupt.
(3) Set the interrupt generation cycle TM0BR(0x0000A188)=0x95	(3) Set the interrupt generation cycle to timer 0 base register (TM0BR). The set value is 149 (0x95) due to 150 dividing.
(4) Select the count clock source TM0MD(0x0000A180) bp2-0: TM0CK2-0=000	(4) Select the count clock source (IOCLK) by the TM0CK2 to 0 flag of the TM0MD register.
(5) Initialize timer 0 TM0MD(0x0000A180) bp6: TM0LDE=1	(5) Set the TM0LDE flag of the TM0MD register to “1” to initialize timer 0. The value of the TM0BR register is loaded into the TM0BC counter. Reset the TM0LDE flag to “0” after setting.
(6) Set an interrupt level G3ICR(0x0000890C) bp14-12: G3LV2-0=100	(6) Set an interrupt level by the G3LV2 to 0 flag of the G3ICR register. Clear the request flag if the interrupt request flag is already set.
(7) Enable an interrupt G3ICR(0x0000890C) bp8: G3IE0=1	(7) Set the G3IEO flag of the G3ICR register to “1” to enable an interrupt.
(8) Start timer operation TM0MD(0x0000A180) bp7: TM0CNE=1	(8) Set the TM0CNE flag of the TM0MD register to “1” to operate timer 0.

TM0BC counter starts to count down. When the TM0BC counter generates underflow, the interrupt request flag is set. The value of the TM0BR register is loaded into the value of the TM0BC counter, and the counting down operation restarts.

8.5 Timer Output Function

8.5.1 Timer Output Function Operation

TMnIO pin can output a pulse signal at any frequency.

■ Timer Output Operation

Signals of 2 times of the timer interrupt generation cycle can be output. Output pins are as follows:

Table:8.5.1 Timer and Output Pin

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4	Timer 5	Timer 6	Timer 7	Timer 14	Timer 15	Timer 16	Timer 17
Pulse output pin	-	TM1IO pin (P31)	TM2IO pin (P32)	TM3IO pin (P33)	TM4IO pin (P34)	TM5IO pin (P35)	-	TM7IO pin (P51)	-	-	-	TM17IO pin (P16)

■ Count Timing of Timer Output

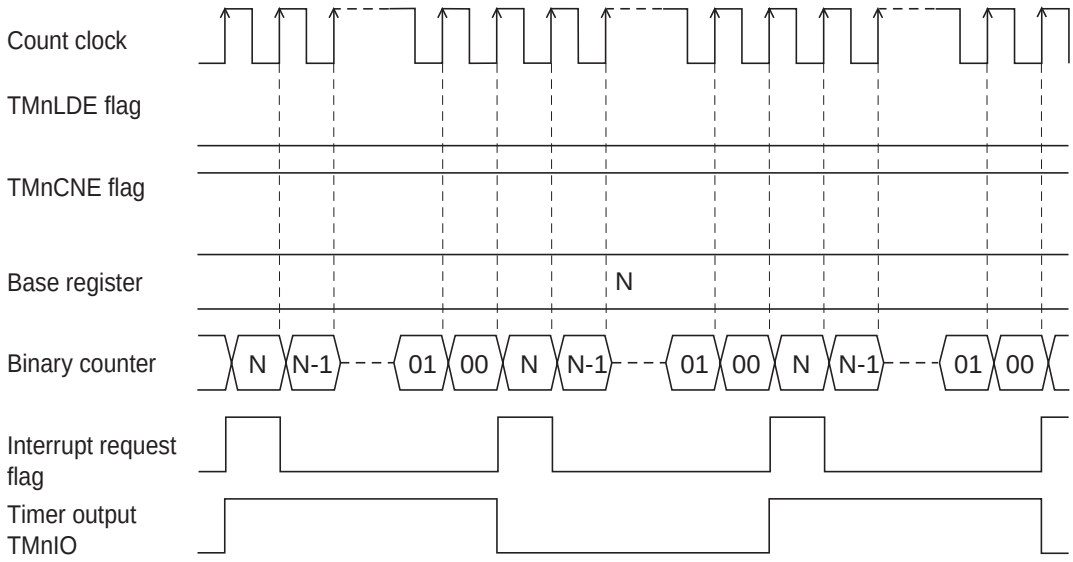


Figure:8.5.1 Count Timing of Timer Output

8.5.2 Setup Example

■ Timer Output Setup Example

The TM1IO pin outputs 100 KHz pulse by using timer 1. In order to output 100 KHz, select IOCLK for a count clock source, and set 1/2 cycle (200 KHz) to the timer 1 base register.

An example setup procedure, with a description of each step is shown below.

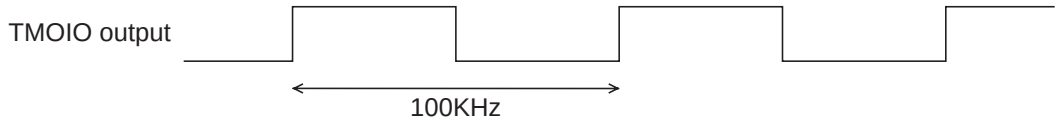


Figure:8.5.2 Output Waveform of TM1IO pin

Setup Procedure	Description
(1) Check the counter stopped TM1MD (0x0000A181) bp6: TM1LDE=0 bp7: TM1CNE=0	(1) Set the TM1LDE flag and the TM1CNE flag of the timer 1 mode register (TM1MD) to “0” to stop timer 1 counting.
(2) Set the TM1IO pin to output and mode P3MD (0x0000A033) bp1: P31M=1 P3DIR (0x0000A023) bp1: P31D=1	(2) Set the P3MD flag of the port 3 mode register (P31M) to “1” for TM1IO pin setting. Set the P31D flag of the port 3 I/O control register (P3DIR) to “1” for output pin setting.
(3) Set 1/2 cycle for timer output TM1BR(0x0000A189)=0x95	(3) Set 1/2 cycle of the timer output to the timer 1 base register (TM1BR). The setting value is 149 (0x95) due to 200KHz. Setting value = (10MHZ × 2/6) / 200KHz -1
(4) Select the count clock source TM1MD(0x0000A181) bp2-0: TM1CK2-0=000	(4) Select IOCLK to the count clock source by the TM1CK2-0 flag of the TM1MD register.
(5) Initialize timer 1 TM1MD(0x0000A181) bp6: TM1LDE=1	(5) Set the TM1LDE flag of the TM1MD register to “1” to initialize timer 1. The value of the TM1BR register is loaded to the TM1BC counter; and, output of TM1IO changes “L”. Reset the TM1LDE flag to “0”.
(6) Start the timer operation TM1MD (0x0000A181) bp7: TM1CNE=1	(6) Set the TM1CNE flag of the TM1MD register to “1” to operate timer 1.

TM1BC starts to count down from 0x95. When an underflow occurs, the signal of theTM1IO output pin is inverted; and, TM1BC starts to count down from 0x95 again.

8.6 Event Count

8.6.1 Operation

Event count operation is to count the rising edge of the TMnIO pin input as count clock.

■ Event Count Operation

When the TMnIO pin is selected to the clock source, the event counter operates. The event count operation means that the binary counter (TMnBC) counts down the external signal input to the TMnIO pin. The underflow interrupt request is generated at the binary counter underflow. The relationship between timers and event input pins is shown below.

Table:8.6.1 TImer and Input Pin

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4	Timer 5	Timer 6	Timer 7	Timer 14	Timer 15	Timer 16	Timer 17
Pulse output pin	-	TM1IO pin (P31)	TM2IO pin (P32)	TM3IO pin (P33)	TM4IO pin (P34)	TM5IO pin (P35)	-	TM7IO pin (P51)	-	-	-	TM17IO pin (P16)

■ Setting the Base Register

Set event count numbers that generate interrupts to the base register TMnBR.

Interrupt generation count number = TMnBR setting + 1

■ Count Timing of TMnIO pin input

TMnIO pin input is sampled by IOCLK. The rising edge of TMnIO pin input is counted, and the binary counter is counted down. The pulse width should be IOCLK × 1.5 or more to detect the rising edge.

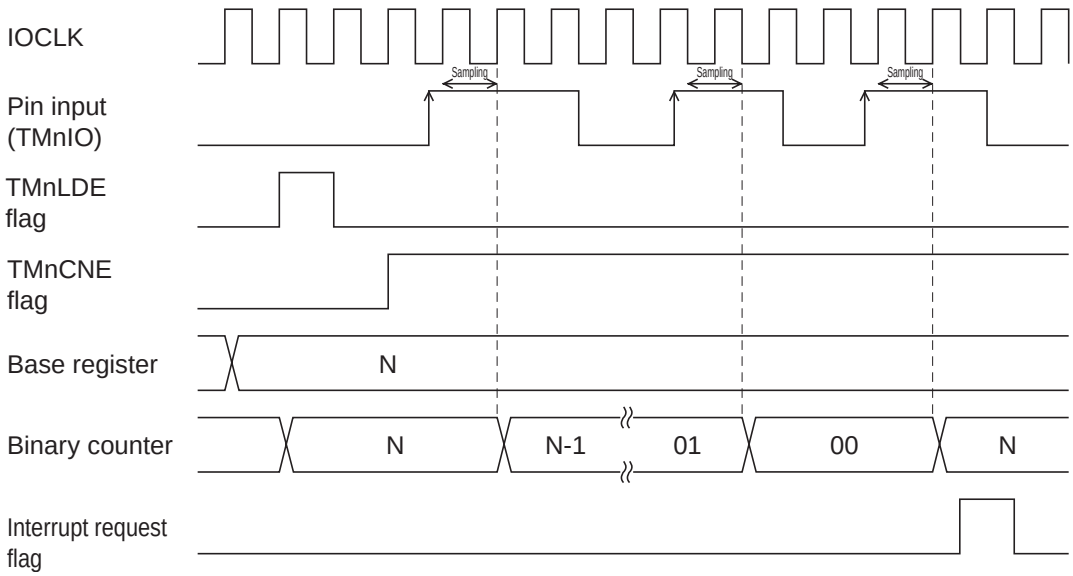


Figure:8.6.1 Count Timing of TMnIO Pin Input

8.6.2 Setup Example

■ Event Count Setup Example

If the rising edge of the TM1IO input pin is detected 5 times with the timer 1, an interrupt is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM1MD(0x0000A181) bp6: TM1LDE=0 bp7: TM1CNE=0	(1) Set the TM1LDE flag and the TM1CNE flag of the timer 1 mode register (TM1MD) to “0” to stop timer 1 counting.
(2) Disable the interrupt G3ICR(0x0000890C) bp9: G3IE1=0	(2) Set the G3IE1 flag of the G3ICR register to “0” to disable the interrupt.
(3) Set the TM1IO pin to input P3DIR(0x0000A023) bp1: P31D=0	(3) Set the P31D flag of the port 3 I/O control register (P3DIR) to “0” to set to the input pin.
(4) Set the interrupt generation cycle TM1BR(0x0000A189)=0x04	(4) Set the interrupt generation cycle to the timer 1 base register (TM1BR). The setting value should be 4 because counting is 5.
(5) Select the count clock source TM1MD(0x0000A181) bp2-0: TM1CK2-0=111	(5) Select the TM1IO pin to the count clock source by the TM1CK2-0 flags of the TM1MD register.
(6) Initialize the timer 1 TM1MD(0x0000A181) bp6: TM1LDE=1	(6) Set the TM1LDE flag of the TM1MD register to “1” to initialize the timer 1. The value of the TM1BR is loaded into the TM1BC counter. Reset the TM1LDE flag to “0” after setting.
(7) Set the interrupt level G3ICR(0x0000890C) bp14-12: G3LV2-0=100	(7) Set the interrupt level by the G3LV2-0 flag of the G3ICR register. If the interrupt request flag has been set already , clear the request flag.
(8) Enable the interrupt G3ICR(0x0000890C) bp9: G3IE1=1	(8) Set the G3IE1 flag of the G3ICR register to “1” to enable the interrupt.
(9) Start the timer operation TM1MD(0x0000A181) bp7: TM1CNE=1	(9) Set the TM1CNE flag of the TM1MD register to “1” to operate the timer 1.

8.7 Cascade Connection

8.7.1 Operation

Cascading timers forms a 16-bit timer, 24-bit timer and 32-bit timer.

■ Cascade Connection Operation (When using timers as a 16-bit timer)

Table:8.7.1 shows timer functions at 16-bit timer cascade connection.

Table:8.7.1 Cascade Connection Operation (When using timers as a 16-bit timer)

16-bit timer	Timer 1 + timer 0	Timer 2 + timer 1	Timer 3 + timer 2	Timer 5 + timer 4	Timer 6 + timer 5	Timer 7 + timer 6
Interrupt source	TM1IRQ	TM2IRQ	TM3IRQ	TM5IRQ	TM6IRQ	TM7IRQ
Interval timer	O	O	O	O	O	O
Timer output	Timer 1	Timer 2	Timer 3	Timer 5	Timer 6	Timer 7
Cascade connection setting register	TM1MD	TM2MD	TM3MD	TM5MD	TM6MD	TM7MD
Count clock source setting register	TM0MD	TM1MD	TM2MD	TM4MD	TM5MD	TM6MD
Count value setting register	TM1BR+TM0BR	TM2BR+TM1BR	TM3BR+TM2BR	TM5BR+TM4BR	TM6BR+TM5BR	TM7BR+TM6BR

16-bit timer	Timer 15 + timer 14	Timer 16 + timer 15	Timer 17 + timer 16
Interrupt source	TM15IRQ	TM16IRQ	TM17IRQ
Interval timer	O	O	O
Timer output	Timer 15	Timer 16	Timer 17
Cascade connection setting register	TM15MD	TM16MD	TM17MD
Count clock source setting register	TM14MD	TM15MD	TM16MD
Count value setting register	TM15BR+TM14BR	TM16BR+TM15BR	TM17BR+TM16BR

■ Cascade Connection Operation (When using timers as a 24-bit timer)

Table:8.7.2 shows timer functions at 24-bit timer cascade connection.

Table:8.7.2 Cascade Connection Operation (When using timers as a 24-bit timer)

24-bit timer	Timer 2 + timer 1 + timer 0	Timer 3 + timer 2 + timer 1	Timer 6 + timer 5 + timer 4	Timer 7 + timer 6 + timer 5
Interrupt source	TM2IRQ	TM3IRQ	TM6IRQ	TM7IRQ
Interval timer	O	O	O	O
Timer output	TImer 2	Timer 3	Timer 6	Timer 7
Event counter	Timer 0	Timer 1	Timer 4	Timer 5
Cascade connection setting register	TM2MD TM1MD	TM3MD TM2MD	TM6MD TM5MD	TM7MD TM6MD
Count clock source setting register	TM0MD	TM1MD	TM4MD	TM5MD
Count value setting register	TM2BR+TM1BR+TM0BR	TM3BR+TM2BR+TM1BR	TM6BR+TM5BR+TM4BR	TM7BR+TM6BR+TM5BR

24-bit timer	Timer 16 + timer 15 + timer 14	Timer 17 + timer 16 + timer 15
Interrupt source	TM16IRQ	TM17IRQ
Interval timer	O	O
Timer output	TImer 16	Timer 17
Event counter	Timer 14	Timer 15
Cascade connection setting register	TM16MD TM15MD	TM17MD TM16MD
Count clock source setting register	TM14MD	TM15MD
Count value setting register	TM16BR+TM15BR+TM14BR	TM17BR+TM16BR+TM15BR

■ Cascade Connection Operation (When using timers as a 32-bit timer)

Table:8.7.3 shows timer functions at 32-bit timer cascade connection.

Table:8.7.3 Cascade Connection Operation (When using timers as a 32-bit timer)

32-bit timer	Timer 3 + timer 2 + timer 1 + timer 0	Timer 7 + timer 6 + timer 5 + timer 4	Timer 17 + timer 16 + timer 15 + timer 14
Interrupt source	TM3IRQ	TM7IRQ	TM17IRQ
Interval timer	O	O	O
TImer output	Timer 3	Timer 7	Timer 17
Event counter	Timer 0	Timer 4	Timer 14
Cascade connection setting register	TM3MD TM2MD TM1MD	TM7MD TM6MD TM5MD	TM17MD TM16MD TM15MD
Count clock source setting register	TM0MD	TM4MD	TM14MD
Count value setting register	TM3BR+TM2BR+TM1BR+TM0BR	TM7BR+TM6BR+TM5BR+TM4BR	TM17BR+TM16BR+TM15BR+TM14BR

■ Count Timing of Cascade Connection

Figure:8.7.1 shows timing when cascaded timer 1 and timer 0 count down as a 16-bit timer.

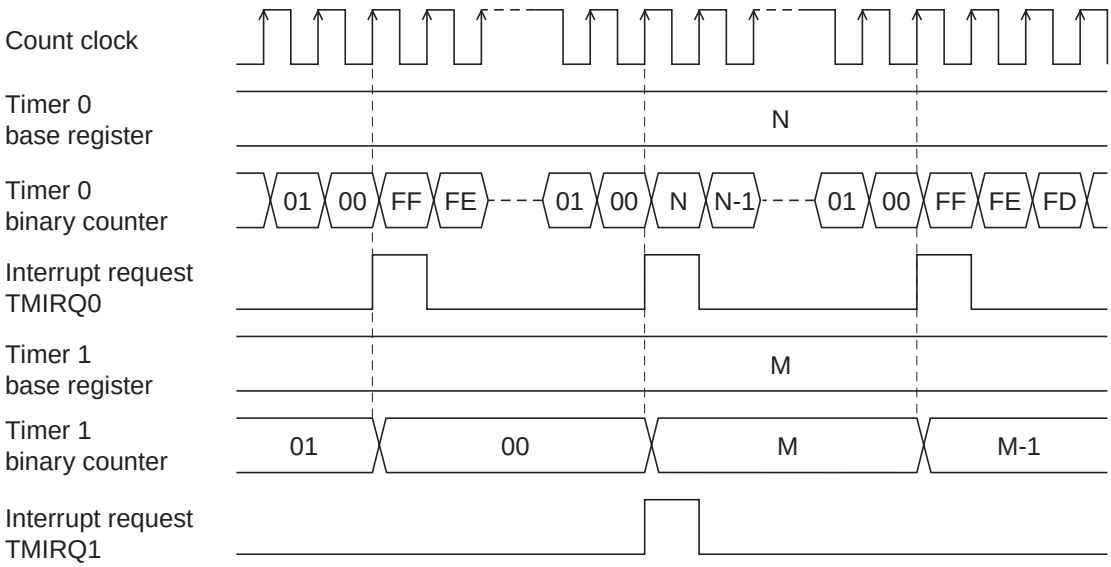


Figure:8.7.1 Count Timing of Cascade Connection

In reading out value of binary counter during timer operation with 8-bit timer in cascade connection, the value of binary counter may not be correctly read out.

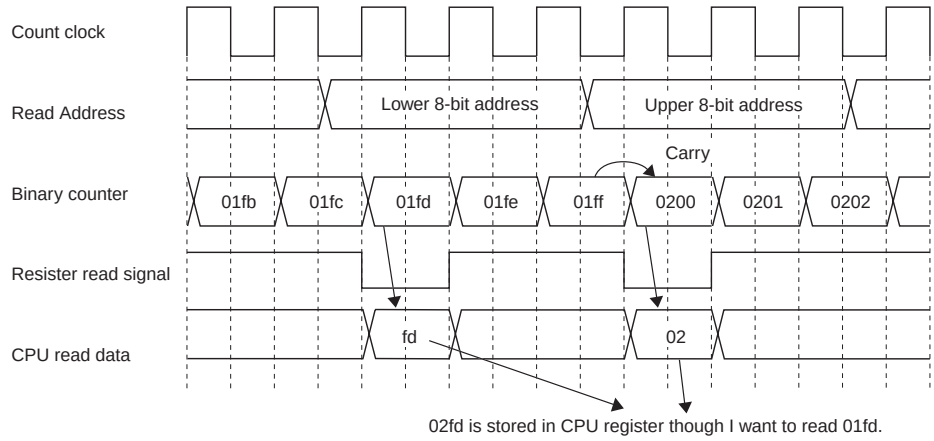
There are multiple binary counters of 8-bit timer, but all binary counters connectable in cascade are not allocated to continuous addresses. Binary counter can be read out with 8, 16 and 32-bit access instruction. But binary counter in cascade connection may not be read out at a time according to the combination of the number of binary counters connected in cascade.
Therefore, if raised from the lower 8 bits to the upper 8bits during several-time readout, correct value cannot be read out.

Example of 8-bit Timer Address Map (TMnBC:binary counter)

Adderss	x = F	x = E	x = D	x = C	x = B	x = A	x = 9	x = 8	x = 7	x = 6	x = 5	x = 4	x = 3	x = 2	x = 1	x = 0
x'0000A18X			TM3BR	TM2BR			TM1BR	TM0BR			TM3MD	TM2MD			TM1MD	TM0MD
x'0000A19X								TM03PSC			TM3BC	TM2BC			TM1BC	TM0BC
x'0000A1AX			TM7BR	TM6BR			TM5BR	TM4BR			TM7MD	TM6MD			TM5MD	TM4MD
x'0000A1BX								TM47PSC			TM7BC	TM6BC			TM5BC	TM4BC

The address of the binary counter is continuous. not continuous.

Image chart when value of binary counter is read
by two 8-bit accesses with 16-bit timer that connects 8-bit timer in cascade.



(1) In case of 16-bit cascade connection 1 (In case the lower 8 bit timer addresses are even)
In 8-bit access instruction, the value of 16 bit binary counter cannot be read out at a time.
Therefore, if the digit is raised from the lower 8 bits to the upper 8 bits, correct value cannot be read out.
In 16-bit access instruction, correct value can be read out.

(2) In case of 16-bit cascade connection 2 (In case the lower 8 bit timer addresses are odd)
As each timer address is discontinuous, the value of binary counter cannot be read out at a time in either 16 or 32-bit access instruction.
Stop the timer in order to read out the correct value.

(3) In case of 24-bit cascade connection, 32-bit cascade connection
As each timer address is discontinuous, the value of binary counter cannot be read out at a time even if 32-bit access instruction is used.
Stop the timer in order to read out the correct value.

■ Selecting the Count Source

Select any desired count source for the lowest-order timer. Set the count clock source for high-order timers (except the lowest-order timer) to “cascading”.

For example, when using timers 0 and 1 as a 16-bit timer, set a desired count clock source for timer 0 and the count clock source for timer 1 to “cascading”. When using timers 1, 2 and 3 as a 32-bit timer , set a desired count clock source for timer 0 and the count clock source for timer 1 to “cascading”.

■ Setting the Timer Base Register

Set a timer division ratio in timer base register (TMnBR).
Timer interrupt cycle = (TMnBR setting + 1) × Count clock source cycle
For example, when using timers 0 and 1 as a 16-bit timer and setting the interrupt cycle to “0x2000”, “0x1FFF(0x2000-1)” should be set the TMnBR register. Set “0x1F” to the upper TM1BR register and “0xFF” to the lower TM0BR register. It is possible to set the TMnBR register by 16-bit access simultaneously when using timer 1 + timer 0, timer 3 + timer 2, timer 5 + timer 4, timer 7 + timer 6, timer 15 + timer 14 or timer 17 + timer 16 as a 16-bit timer. (Not when timer 2 + timer 1, timer 6 + timer 5 and timer 16 + timer 15 are cascaded as a 24-bit timer or 32-bit timer.)

■ Initializing the timer

Set the TMnLDE flags of all cascaded timers to “1” to initialize the timers. (It is not necessary to set all registers at the same time.)

■ Enabling Counting Operation

When enabling timer counting operation, enable the counting operation of the cascaded timers in sequence starting from the highest-order timer, or enable the counting operation for all of the cascaded timers simultaneously.

■ Stopping Counting Operation

When stopping timer counting operation, stop the counting operation of the cascaded timers in sequence starting from the lowest-order timer, or stop the counting operation for all of the cascaded timers simultaneously.

■ Timer Outputs

The timer output from the highest of the cascaded timers can be used. Operation of the timer output from the lower cascaded timers is not guaranteed.

■ Interrupt Requests

The interrupt requests from the highest of the cascaded timers can be used. The interrupt requests from the lower cascaded timers are not generated, but set timers to interrupts disabled.

■ Changing the Time Base Register during Counting Operation

When timer 1 + timer 0, timer 3 + timer 2, timer 5 + timer 4, timer 7 + timer 6 , timer 15 + timer 14, or timer 17 + timer 16 are used as a 16-bit timer, the TMnBR register during counting operation can be changed via 16-bit access.When using other combination as a 16-bit timer or 32-bit timer, avoid load timing to the binary counter.

Combined 8-bit access registers can be used with 16-bit access at cascade connection. (when the addresses of the registers are consecutive)

8.7.2 Setup Example

■ Cascade Connection Setup Example

Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 0 and timer 1, as a 16-bit timer is shown. An interrupt is generated 30000 times every 1 ms by selecting clock source IOCLK. Oscillation frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM1MD(0x0000A181) bp6: TM0LDE=0 bp7: TM0CNE=0 TM0MD(0x0000A180) bp6: TM0LDE=0 bp7: TM0CNE=0	(1) Set the TM1LDE flag and the TM1CNE flag of the timer 1 mode register (TM1MD) to “0” to stop the counter. Set the TM0LDE flag and TM0CNE flag of the timer 0 mode register (TM0MD) to “0” to stop the timer 1 counting.
(2) Disable the interrupt G3ICR(0x0000890C) bp8: G3IE0=0 bp9: G3IE1=0	(2) Set the G3IEO flag of the G3ICR register to “0” to disable the timer 0 underflow interrupt. Set the G3IE1 flag of the G3ICR register to “0” to disable the timer 1 underflow interrupt.
(3) Set the interrupt generation cycle TM1BR(0x0000A189)=0x75 TM0BR(0x0000A188)=0x2F	(3) Set the interrupt generation cycle to the timer 0 base register (TM0BR) and timer 1 base register (TM1BR). It is set to 29999 (0x752F) due to 30000 dividing.
(4) Select the count clock source TM1MD(0x0000A181) bp2-0: TM1CK2-0=011 TM0MD(0x0000A180) bp2-0: TM0CK2-0=000	(4) Select the count clock source (cascading with the timer 0) by the TM1CK2-0 flag of the TM1MD register. Select the count clock source (IOCLK) by the TM0CK2-0 flag of the TM0MD register.
(5) Initialize the timer 0 and 1 TM1MD(0x0000A181) bp6: TM1LDE=1 TM0MD(0x0000A180) bp6: TM0LDE=1	(5) Set the TM1LDE flag of the TM1MD register to “1” to initialize the timer 1. Set the TM0LDE flag of the TM0MD register to “1” to initialize the timer 0. The value of the TM1BR register is loaded into the TM1BC counter; and, the value of the TM0BR register is loaded into the TM0BC counter. Reset the TM1LDE flag and the TM0LDE flag to “0” after the setting.
(6) Set the interrupt level G3ICR(0x0000890C) bp14-12: G3LV2-0=100	(6) Set the interrupt level by the G3LV2-0 flag of the G3ICR register. If any interrupt request flag may be already set, clear all request flags.
(7) Enable the interrupt G3ICR(0x0000890C) bp9: G3IE1=1	(7) Set the G3IE1 flag of the G3ICR register to “1” to enable the interrupt. Leave the G3IE0 as it is “0” with interrupts disabled.

Setup Procedure	Description
(8) Start the timer operation TM1MD(0x0000A181) bp7: TM1CNE=1 TM0MD(0x0000A180) bp7: TM0CNE=1	(8) Set the TM1CNE flag of the TM1MD register to “1” to operate the timer 1 of the upper timer. Set the TM0CNE flag of the TM0MD register to “1” to operate the timer 0.

TM1BC+TM0BC counter counts down as a 16-bit counter.

When TM1BC+TM0BC counter generates the underflow, the interrupt request flag (G3IR1) is set and the value of TM1BR and TM0BR register is loaded to TM1BC and TM0BC counter; and, the counter starts to count down again.

Chapter 9 16-bit Timer

9

9.1 Overview

This LSI contains 6 general-purpose 16-bit timers (Timer 8, timer 9, timer 10, timer 11, timer 12, and timer 13).

9.1.1 Functions

Table: 9.19. shows the function of each timer.

Table:9.1.1 16-bit Timer Functions

	Timer 8	Timer 9	Timer 10	Timer 11	Page
Interrupt cause	NTMHIRQ8 NTMAIRQ8 NTMBIRQ8	NTMHIRQ9 NTMAIRQ9 NTMBIRQ9	NTMHIRQ10 NTMAIRQ10 NTMBIRQ10	NTMHIRQ11 NTMAIRQ11 NTMBIRQ11	-
Interval timer	O	O	O	O	VIII-39
Event count	O	O	O	O	VIII-43
Up/down count	O	O	O	O	VIII-48
Timer output	O	O	O	O	VIII-52
PWM output	O	O	O	O	VIII-57
Input capture	O	O	O	O	VIII-63
1-shot output	O	O	O	O	VIII-66
External trigger activation	O	O	O	O	VIII-68
A/D conversion start	-	-	-	-	VIII-72
Count clock source	IOCLK IOCLK/8 IOCLK/64 Timer 2 underflow TM8BIO pin input	IOCLK IOCLK/8 IOCLK/64 Timer 3 underflow TM9BIO pin input	IOCLK IOCLK/8 Timer 0 underflow Timer 1 underflow TM10BI0 pin input	IOCLK IOCLK/8 Timer 4 underflow Timer 5 underflow TM11IO1 pin input	VIII-39

	Timer 12	Timer 13	Page
Interrupt cause	NTMHIRQ12 NTMAIRQ12 NTMBIRQ12	NTMHIRQ13 NTMAIRQ13 NTMBIRQ13	-
Interval timer	O	O	VIII-39
Event count	-	-	VIII-43
Up/down count	O	O	VIII-48
Timer output	-	-	VIII-52
PWM output	-	-	VIII-57
Input capture	-	-	VIII-63
1-shot output	-	-	VIII-66
External trigger activation	PWM0 only	PWM1 only	VIII-68
A/D conversion start	O	O	VIII-72
Count clock source	IOCLK,MCLK IOCLK/8,MCLK/8 Timer 6 underflow Timer 7 underflow	IOCLK,MCLK IOCLK/8,MCLK/8 Timer 6 underflow Timer 7 underflow	VIII-39

9.1.2 Connection

■ 16-bit Timer Connection Diagram (TImer 8, timer 9)

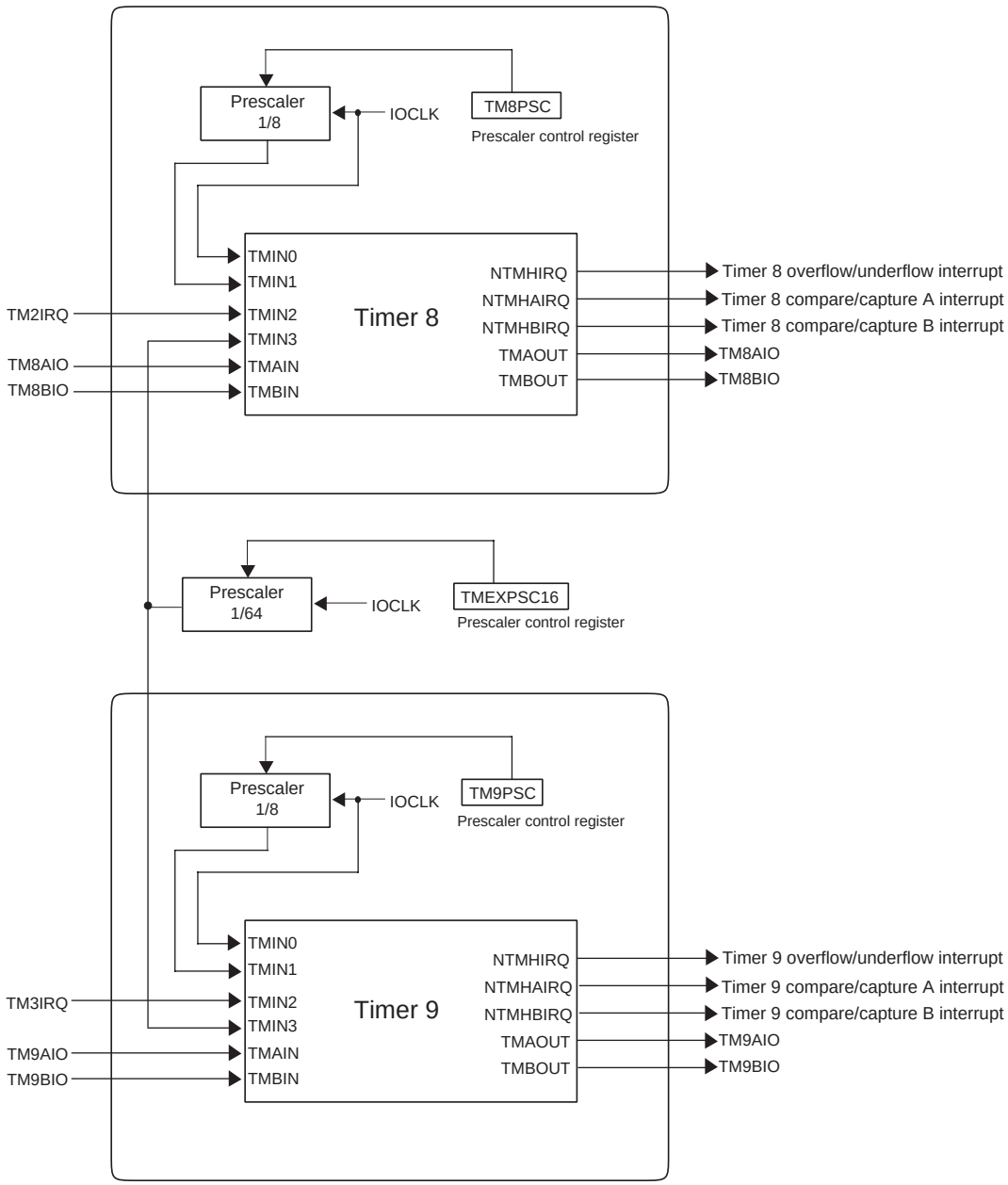


Figure:9.1.1 16-bit Timer Connection Diagram (Timer 8, 9)

■ 16-bit Timer Connection Diagram (TImer 10, 11)

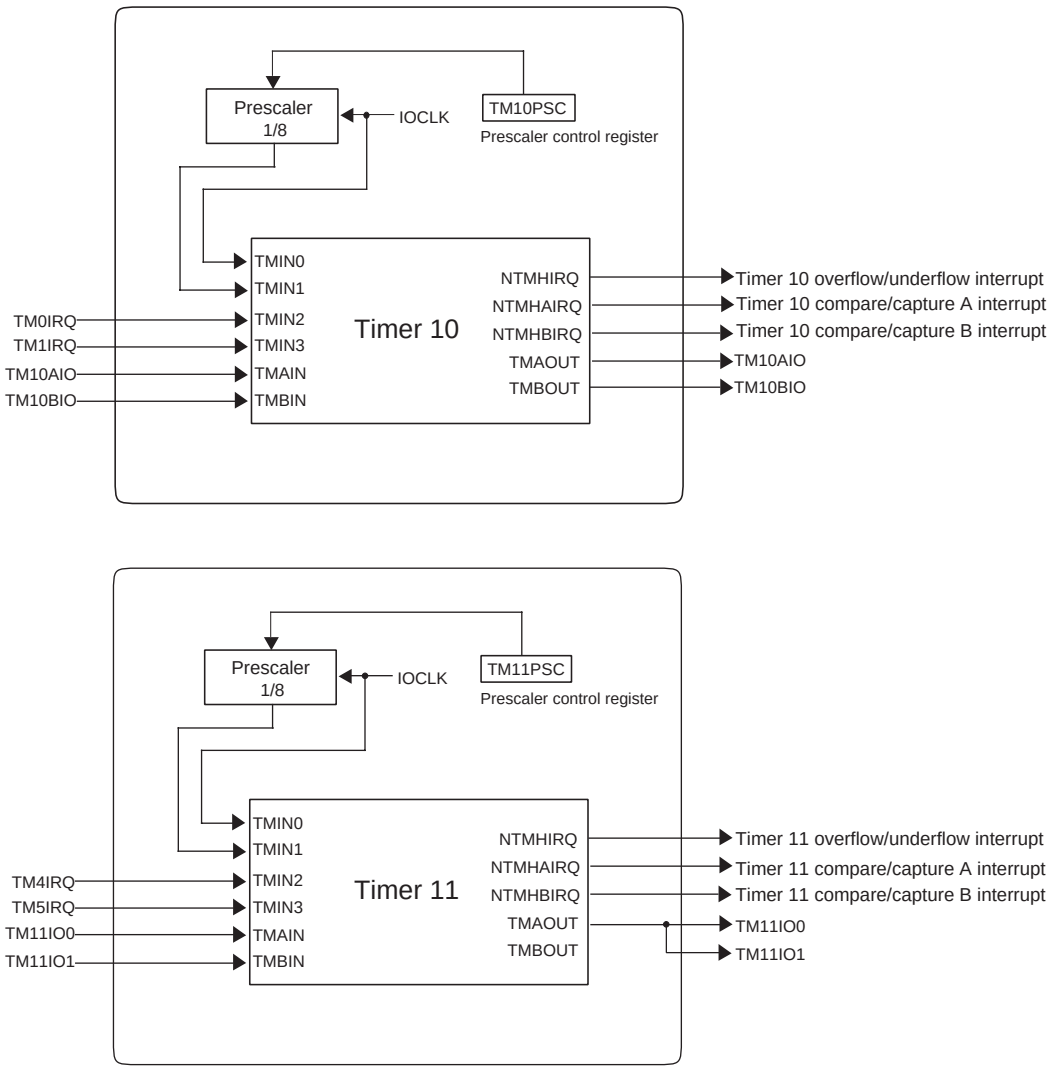


Figure:9.1.2 16-bit Timer Connection Diagram (TImer 10, 11)

■ 16-bit Timer Connection Diagram (TImer 12, 13)

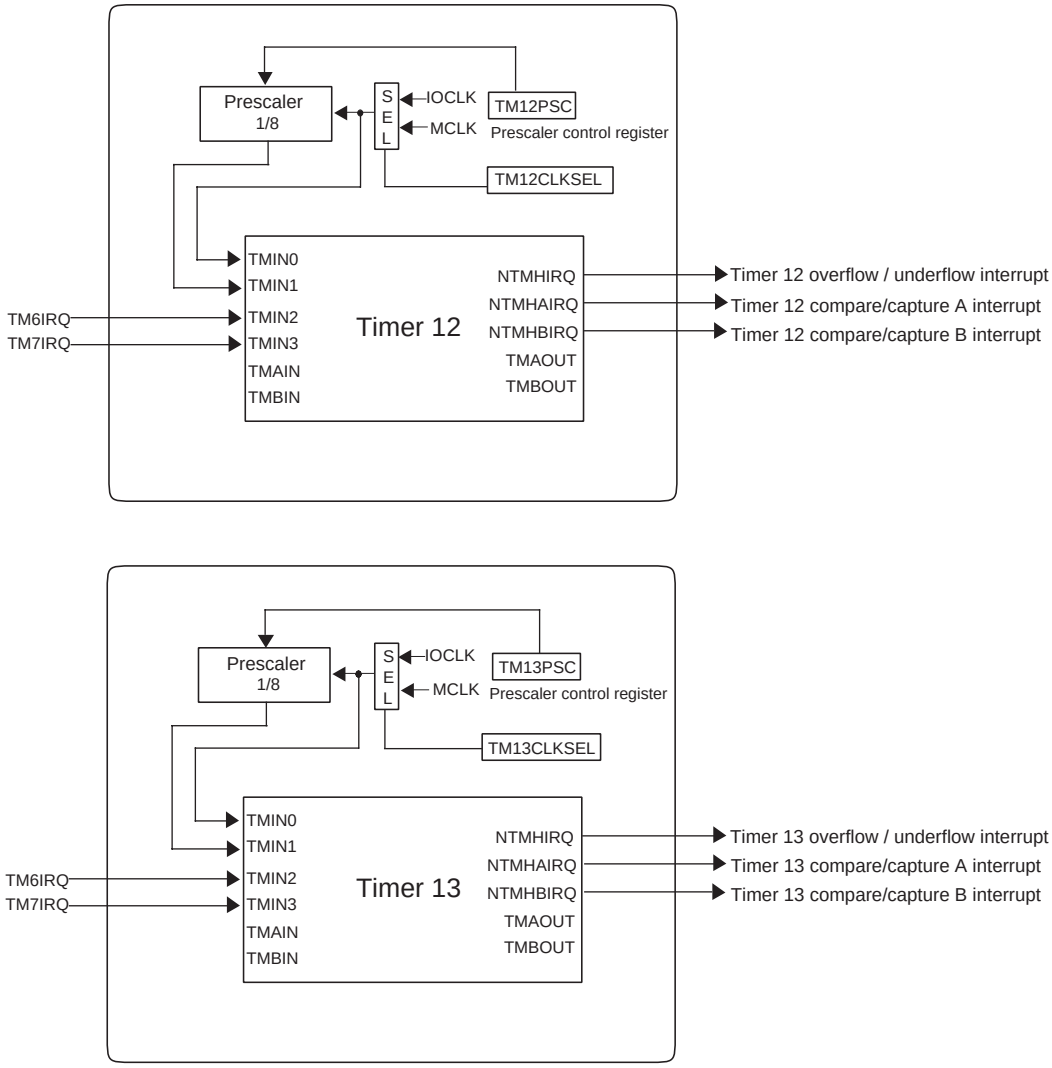


Figure:9.1.3 16-bit Timer Connection Diagram (TImer 12, 13)

9.1.3 Block Diagram

■ 16-bit TImer Block Diagram

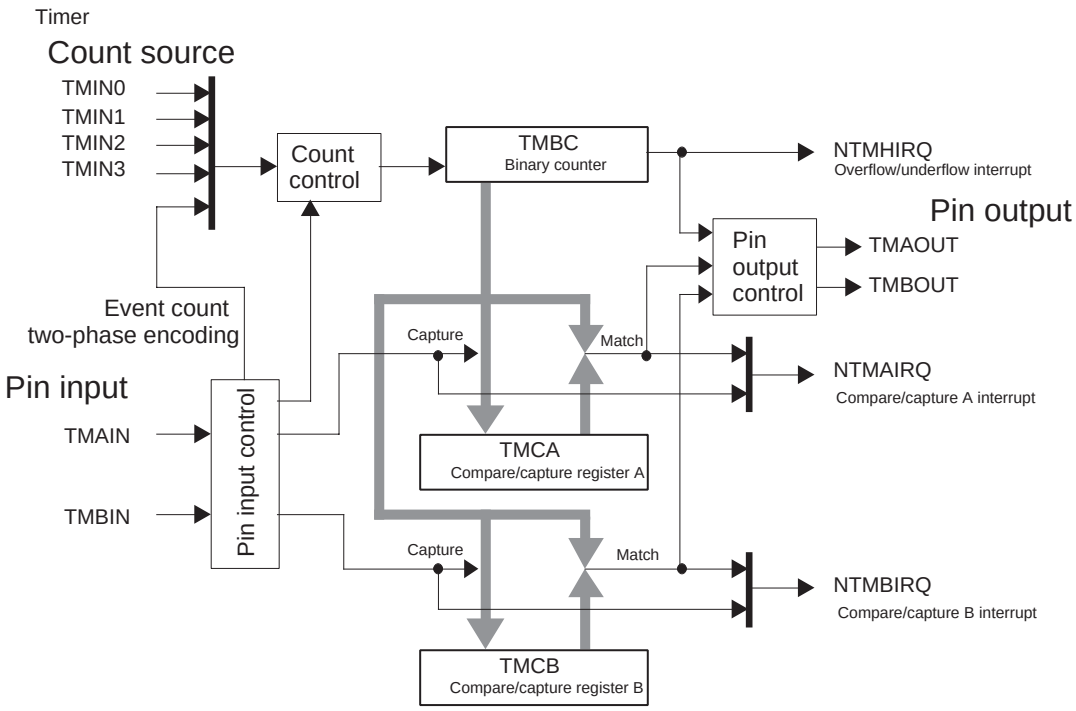


Figure:9.1.4 16-bit TImer Block Diagram

9.2 Control registers

Timer 8 to timer 13 are composed of the prescaler control register (TMnPSC), the binary counter (TMnBC), compare/capture A register (TMnCA) and compare/capture B register (TMnCB), and are controlled by the mode register (TMnMD), compare/capture A mode register (TMnMDA) and compare/capture B mode register (TMnMDB). When the prescaler output is selected to a count clock source, control of the prescaler control register is necessary.

9.2.1 Registers

Table: 9.2.1 shows the registers that control 16-bit timers.

Table:9.2.1 16-bit Timer Control Registers

	Register	Address	R/W	Access size	Description	Page
Prescaler	TMEXPSC16	0x0000A218	R/W	8,16	External prescaler control register 1	IX-11
Timer 8	TM8PSC	0x0000A214	R/W	8,16	Timer 8 prescaler control register	IX-9
	TM8CA	0x0000A208	R/W	16	Timer 8 compare/capture A register	IX-15
	TM8CB	0x0000A20C	R/W	16	Timer 8 compare/capture B register	IX-18
	TM8BC	0x0000A210	R	16	Timer 8 binary counter	IX-13
	TM8MD	0x0000A200	R/W	8,16	Timer 8 mode register	IX-20
	TM8MDA	0x0000A204	R/W	8	Timer 8 compare/capture A mode register	IX-26
	TM8MDB	0x0000A205	R/W	8	Timer 8 compare/capture B mode register	IX-32
	G7ICR	0x0000891C	R/W	8,16	Group 7 interrupt control register	V-17
	P3MD	0x0000A033	R/W	8	Port 3 output mode register	VII-16
	P3DIR	0x0000A023	R/W	8	Port 3 I/O control register	VII-15
Timer 9	TM9PSC	0x0000A234	R/W	8,16	Timer 9 prescaler control register	IX-9
	TM9CA	0x0000A228	R/W	16	Timer 9 compare/capture A register	IX-17
	TM9CB	0x0000A22C	R/W	16	Timer 9 compare/capture B register	IX-18
	TM9BC	0x0000A230	R	16	Timer 9 binary counter	IX-14
	TM9MD	0x0000A220	R/W	8,16	Timer 9 mode register	IX-21
	TM9MDA	0x0000A224	R/W	8	Timer 9 compare/capture A mode register	IX-27
	TM9MDB	0x0000A225	R/W	8	Timer 9 compare/capture B mode register	IX-33
	G8ICR	0x00008920	R/W	8,16	Group 8 interrupt control register	V-18
	P4MD	0x0000A034	R/W	8	Port 4 output mode register	VII-18
	P4DIR	0x0000A024	R/W	8	Port 4 I/O control register	VII-18

	Register	Address	R/W	Access size	Description	Page
Timer 10	TM10PSC	0x0000A254	R/W	8,16	Timer 10 prescaler control register	IX-10
	TM10CA	0x0000A248	R/W	16	Timer 10 compare/capture A register	IX-17
	TM10CB	0x0000A24C	R/W	16	Timer 10 compare/capture B register	IX-18
	TM10BC	0x0000A250	R	16	Timer 10 binary counter	IX-14
	TM10MD	0x0000A240	R/W	8,16	Timer 10 mode register	IX-22
	TM10MDA	0x0000A244	R/W	8	Timer 10 compare/capture A mode register	IX-28
	TM10MDB	0x0000A245	R/W	8	Timer 10 compare/capture B mode register	IX-34
	G9ICR	0x00008924	R/W	8,16	Group 9 interrupt control register	V-19
	P4MD	0x0000A034	R/W	8	Port 4 output mode register	VII-18
	P4DIR	0x0000A024	R/W	8	Port 4 I/O control register	VII-18
Timer 11	TM11PSC	0x0000A274	R/W	8,16	Timer 11 prescaler control register	IX-10
	TM11CA	0x0000A268	R/W	16	Timer 11 compare/capture A register	IX-17
	TM11CB	0x0000A26C	R/W	16	Timer 11 compare/capture B register	IX-18
	TM11BC	0x0000A270	R	16	Timer 11 binary counter	IX-14
	TM11MD	0x0000A260	R/W	8,16	Timer 11 mode register	IX-23
	TM11MDA	0x0000A264	R/W	8	Timer 11 compare/capture A mode register	IX-29
	TM11MDB	0x0000A265	R/W	8	Timer 11 compare/capture B mode register	IX-35
	G10ICR	0x00008928	R/W	8,16	Group 10 interrupt control register	V-20
	P7MD	0x0000A037	R/W	8	Port 7 output mode register	VII-25
	P7DIR	0x0000A027	R/W	8	Port 7 I/O control register	VII-22
Timer 12	TM12PSC	0x0000A294	R/W	8,16	Timer 12 prescaler control register	IX-10
	TM12CLKSEL	0x0000A298	R/W	8,16	Timer 12 clock source selection register	IX-12
	TM12CA	0x0000A288	R/W	16	Timer 12 compare A register	IX-17
	TM12CB	0x0000A28C	R/W	16	Timer 12 compare B register	IX-18
	TM12BC	0x0000A290	R	16	Timer 12 binary counter	IX-14
	TM12MD	0x0000A280	R/W	8,16	Timer 12 mode register	IX-24
	TM12MDA	0x0000A284	R/W	8	Timer 12 compare A mode register	IX-30
	TM12MDB	0x0000A285	R/W	8	Timer 12 compare B mode register	IX-36
	G11ICR	0x0000892C	R/W	8,16	Group 11 interrupt control register	V-21
Timer 13	TM13PSC	0x0000A2B4	R/W	8,16	Timer 13 prescaler control register	IX-11
	TM13CLKSEL	0x0000A2B8	R/W	8,16	Timer 13 clock source selection register	IX-12
	TM13CA	0x0000A2A8	R/W	16	Timer 13 compare A register	IX-17
	TM13CB	0x0000A2AC	R/W	16	Timer 13 compare B register	IX-18
	TM13BC	0x0000A2B0	R	16	Timer 13 binary counter	IX-14
	TM13MD	0x0000A2A0	R/W	8,16	Timer 13 mode register	IX-25
	TM13MDA	0x0000A2A4	R/W	8	Timer 13 compare A mode register	IX-31
	TM13MDB	0x0000A2A5	R/W	8	Timer 13 compare B mode register	IX-36
	G12ICR	0x00008930	R/W	8,16	Group 12 interrupt control register	V-22

R/W Readable / Writable
R Readable
W Writable

9.2.2 Prescaler Control Registers

These registers need to be controlled when the prescaler output is selected to the count clock source of the16-bit timer.

■ Timer 8 Prescaler Control Register (TM8PSC: 0x0000A214) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At rest	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 9 Prescaler Control Register (TM9PSC: 0x0000A234) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 10 Prescaler Control Register (TM10PSC: 0x0000A254) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 11 Prescaler Control Register (TM11PSC: 0x0000A274) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 12 Prescaler Control Register (TM12PSC: 0x0000A294) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 13 Prescaler Control Register (TM13PSC: 0x0000A2B4) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ External Prescaler Control Register 1 (TMEXPSC16: 0x0000A218) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM PSCNE	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TMPSCNE	Prescaler operation enable	0: Operation disabled 1: Operation enabled
6-0	-	-	-

■ Timer 12 Clock Source Selection Register (TM12CLKSEL: 0x0000A298) [8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM 12CLK	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TM12CLK	Clock source selection	0: IOCLK 1: MCLK
6-0	-	-	-

■ Timer 13 Clock Source Selection Register (TM13CLKSEL: 0x0000A2B8)[8, 16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM 13CLK	-	-	-	-	-	-	-
At reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	TM13CLK	Clock source selection	0: IOCLK 1: MCLK
6-0	-	-	-

9.2.3 Programmable Timer Registers

Timer 8 to timer 11 each have 16-bit programmable timer registers. Programmable timer registers are composed of the binary counter (TMnBC), the compare/capture A register (TMnCA) and the compare/capture B register (TMnCB).

■ Timer 8 Binary Counter (TM8BC: 0x0000A210) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

This is a binary counter of timers and a 16-bit readable only register. Table:9.2.2 shows updated timing (0x0000 clear, etc.) of the binary counter.

Table:9.2.2 The Updated Timing of Binary Counter and Update Value

	TMCLE flag (TMnMD)=0	TMCLE flag (TMnMD)=1
When initializing a timer (when the TMLDE flag of the TMnMD register is set to “1”)	TMnBC←0x0000	TMnBC←0x0000
Count clock up (down)	TMnBC←TMnBC+1 (TMnBC←TMnBC-1)	TMnBC←TMnBC+1 (TMnBC←TMnBC-1)
TMnBC overflow	TMnBC←0x0000	TMnBC←0x0000
TMnBC underflow	TMnBC←0xFFFF	TMnBC←0xTMnCA
Count up (down) from the TMnBC and the TMnCA match	TMnBC←TMnBC+1 (TMnBC←TMnBC-1)	TMnBC←0x0000
Count up (down) from the TMnBC and the TMnCB match	No change	No change
At the TMnCA capture	No change	TMnBC←0x0000
At the TMnCB capture	No change	No change

■ Timer 9 Binary Counter (TM9BC: 0x0000A230) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

■ Timer 10 Binary Counter (TM10BC: 0x0000A250) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

■ Timer 11 Binary Counter (TM11BC: 0x0000A270) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

■ Timer 12 Binary Counter (TM12BC: 0x0000A290) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

■ Timer 13 Binary Counter (TM13BC: 0x0000A2B0) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

■ Timer 8 Compare/Capture A Register (TM8CA: 0x0000A208) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a register which has compare operation and capture operation. For the appropriate use of both operations, this register is set by the TMAM1-0 flag of the timer compare capture A(B) register. For compare operation, select the compare capture register to be used as double buffer or single buffer. For capture operation, set the both-edge or one-edge of an input pin to the capture timing.

1. When the compare/capture register is set to compare operation
   The interrupt request (TMAIRQ, TMBIRQ) is generated at the time when the binary counter (TMnBC) and the compare capture register (TMnCA, TMnCB) match. Figure: 9.2.1 shows the block diagram of the compare capture/register.

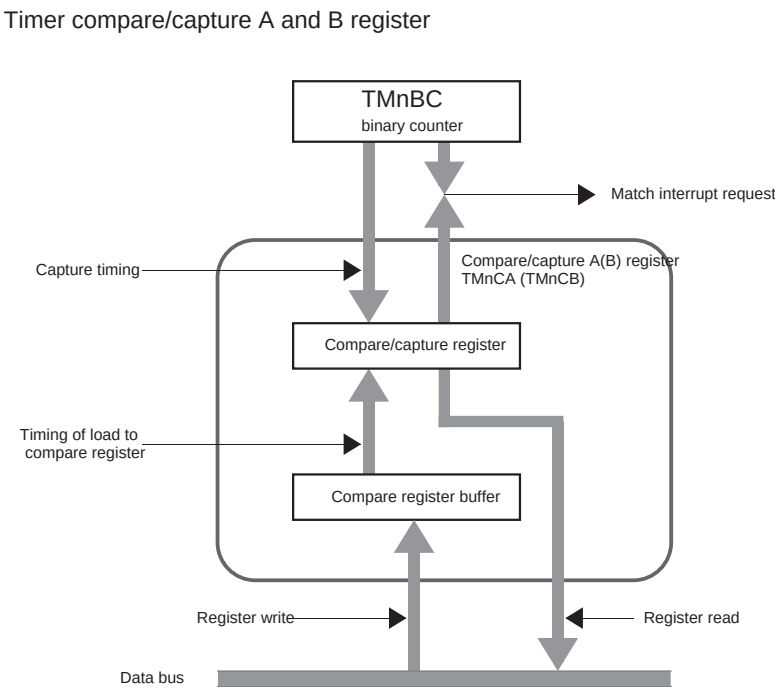


Figure:9.2.1 Block Diagram of Compare/Capture Register

When the compare capture register is set to the double buffer, the value of the TMnCA (TMnCB) is retained in the compare register buffer once; so, when the it is read again after writing to the TMnCA (TMnCB), the previous value may be returned. Table: 9.2.3 shows the timing when the compare/capture register is updated at double buffer.

Table:9.2.3 Updated Timing of Compare/Capture Register (At Double Buffer)

	TMLCE flag (TMnMD)=0	TMLCE flag (TMnMD)=1
When initializing a timer (when the TMLDE flag of the TMnMD register is set to “1”)	TMnCA←TMnCBUFF *1 TMnCB←TMnCBUFF	TMnCA←TMnCBUFF TMnCB←TMnCBUFF
Count clock up (down)	-	-
TMnBC overflow	TMnCA←TMnCBUFF TMnCB←TMnCBUFF	-
TMnBC underflow	TMnCA←TMnCBUFF TMnCB←TMnCBUFF	-
Counting up (down) when the TMnBC and the TMnCA match	-	TMnCA←TMnCBUFF TMnCB←TMnCBUFF *2
Counting up (down) when the TMnBC and the TMnCB match	-	-
At the TMnCA capture	-	TMnBC←TMnCBUFF *3
At the TMnCB capture	-	-

*1 TMnCBUFF: compare register buffer
*2 When the TMnCA is set to the compare register
*3 When the TMnCA is set to the capture register

TMnCBUFF: compare register buffer

2. When the compare/capture register is set to capture operation
   The value of the TMnBC is captured into TMnCA (TMnCB) by inputting the edge selected to the TMAIN (TMBIN) pin; and, the interrupt request (TMAIRQ, TMBIRQ) is generated.

■ Timer 9 Compare/Capture A Register (TM9CA: 0x0000A228) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 10 Compare/Capture A Register (TM10CA: 0x0000A248) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 11 Compare/Capture A Register (TM11CA: 0x0000A268) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 12 Compare A Register (TM12CA: 0x0000A288) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 13 Compare A Register (TM13CA: 0x0000A2A8) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 8 Compare/Capture B Register (TM8CB: 0x0000A20C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 9 Compare/Capture B Register (TM9CB: 0x0000A22C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 10 Compare/Capture B Register (TM10CB: 0x0000A24C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 11 Compare/Capture B Register (TM11CB: 0x0000A26C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 12 Compare B Register (TM12CB: 0x0000A28C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 13 Compare B Register (TM13CB: 0x0000A2AC) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.2.4 Timer Mode Registers

These are readable/writable registers which control the timer 8 to timer 13. The timer compare/capture A mode register controls the compare/capture A register, and the timer compare/capture B mode register controls the compare/capture B register.

■ Timer 8 Mode Register (TM8MD: 0x0000A200) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

<table>
<tr><th>bp</th><th>Flag</th><th>Description</th><th>Setting condition</th></tr>
<tr><td>15</td><td>TMXF</td><td>Timer operation display</td><td>0: Timer stopped
1: Timer operating</td></tr>
<tr><td>14</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>13</td><td>TMTGE</td><td>Timer external trigger enable</td><td>0: Timer activation disabled by external trigger. (trigger input ignored)
1: Timer start when the falling edge is input
(when timer A pin polarity selection bit is “0”)
Timer start when the rising edge is input
(when timer A pin polarity selection bit is “1”)</td></tr>
<tr><td>12</td><td>TMONE</td><td>Timer 1-shot operation enable</td><td>0: 1-shot operation disabled (timer does not stop)
1: 1-shot operation enabled (timer stops when TMBC and TMCA match)</td></tr>
<tr><td>11</td><td>TMCLE</td><td>Timer binary counter enable</td><td>0: Clear operation disabled
1: Clear operation enabled
When the TMCA is set to a compare register
TMBC is cleared when the TMBC and the TMCA match.
When the TMCA is set to a capture register
TMBC is cleared when captured to TMCA.</td></tr>
<tr><td>10</td><td>TMCGE</td><td>Timer count control input enable</td><td>0: Count control disabled by the TMAIN pin input
1: Refer to the following table.
<table>
<tr><th colspan="3">Timer A pin polarity selection bit</th></tr>
<tr><td>TMAIN pin input</td><td>"0"</td><td>"1"</td></tr>
<tr><td>"L"</td><td>Stop counting</td><td>Counting</td></tr>
<tr><td>"H"</td><td>Counting</td><td>Stop counting</td></tr>
</table></td></tr>
<tr><td>9-8</td><td>TMUD1
TMUD0</td><td>Up/down counting selection</td><td>00: Up counting
01: Down counting
10: Up counting (when “H” level is input to the TMAIN pin)
Down counting (when “L” level is input the TMAIN pin)
11: Up counting (when “L” level is input the TMAIN pin)
Down counting (when “H” level is input to the TMAIN pin)
When the 2-phase encoding (1-fold, 4-fold) is selected as the count clock source, set “00”.</td></tr>
<tr><td>7</td><td>TMCNE</td><td>Timer operation enable</td><td>0: Operation disabled
1: Operation enabled</td></tr>
<tr><td>6</td><td>TMLDE</td><td>Timer initialization</td><td>0: Normal operation
1: Initialization
TMBC=0x0000
When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.</td></tr>
<tr><td>5-3</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2-0</td><td>TMCK2
TMCK1
TMCK0</td><td>Timer count clock source selection</td><td>000: IOCLK
001: IOCLK/8
010: IOCLK/64
011: Timer 2 underflow
100: 2-phase encoding (1-fold)
101: 2-phase encoding (4-fold)
110: TMBIN pin input (both edges)
111: TMBIN pin input (single edge)
When pin input (single edge) is selected by the timer, the edge selected by the B pin polarity selection bit of the TMMDB register is counted.
When using IOCLK/8 and IOCLK/64, operation must be enabled respectively by the prescaler control registers (TMPSCNE) and (TMEXPSC16).</td></tr>
</table>

■ Timer 9 Mode Register (TM9MD: 0x0000A220) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	TMXF	Timer operation display	0: Timer stopped 1: Timer operating
14	-	-	-
13	TMTGE	Timer external trigger enable	0: Timer activation disabled by external trigger. (trigger input ignored) 1: Timer start when the falling edge is input (when timer A pin polarity selection bit is “0”) Timer start when the rising edge is input (when timer A pin polarity selection bit is “1”)
12	TMONE	Timer 1-shot operation enable	0: 1-shot operation disabled (timer does not stop) 1: 1-shot operation enabled (timer stops when TMBC and TMCA match)
11	TMCLE	Timer binary counter enable	0: Clear operation disabled 1: Clear operation enabled When the TMCA is set to a compare register TMBC is cleared when the TMBC and the TMCA match. When the TMCA is set to a capture register TMBC is cleared when captured to TMCA.
10	TMCGE	Timer count control input enable	0: Count control disabled by the TMAIN pin input 1: Refer to the following table.

	Timer A pin polarity selection bit	
TMAIN pin input	"0"	"1"
"L"	Stop counting	Counting
"H"	Counting	Stop counting

bp	Flag	Description	Setting condition
9-8	TMUD1 TMUD0	Up/down counting selection	00: Up counting 01: Down counting 10: Up counting (when “H” level is input to the TMAIN pin) Down counting (when “L” level is input the TMAIN pin) 11: Up counting (when “L” level is input the TMAIN pin) Down counting (when “H” level is input to the TMAIN pin) When the 2-phase encoding (1-fold, 4-fold) is selected as the count clock source, set “00”.
7	TMCNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TMLDE	Timer initialization	0: Normal operation 1: Initialization TMBC=0x0000 When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.
5-3	-	-	-
2-0	TMCK2 TMCK1 TMCK0	Timer count clock source selection	000: IOCLK 001: IOCLK/8 010: IOCLK/64 011: Timer 3 underflow 100: 2-phase encoding (1-fold) 101: 2-phase encoding (4-fold) 110: TMBIN pin input (both edges) 111: TMBIN pin input (single edge) When pin input (single edge) is selected by the timer, the edge selected by the B pin polarity selection bit of the TMMDB register is counted. When using IOCLK/8 and IOCLK/64, operation must be enabled respectively by the prescaler control registers (TMPSCNE) and (TMEXPSC16).

■ Timer 10 Mode Register (TM10MD: 0x0000A240) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	TMXF	Timer operation display	0: Timer stopping 1: Timer operating
14	-	-	-
13	TMTGE	Timer external trigger enable	0: Timer activation disabled by external trigger. (trigger input ignored) 1: Timer start when the falling edge is input (when timer A pin polarity selection bit is “0”) Timer start when the rising edge is input (when timer A pin polarity selection bit is “1”)
12	TMONE	Timer 1-shot operation enable	0: 1-shot operation disabled (timer does not stop) 1: 1-shot operation enabled (timer stops when TMBC and TMCA match)
11	TMCLE	Timer binary counter enable	0: Clear operation disabled 1: Clear operation enabled When the TMCA is set to a compare register TMBC is cleared when the TMBC and the TMCA match. When the TMCA is set to a capture register TMBC is cleared when captured to TMCA.
10	TMCGE	Timer count control input enable	0: Count control disabled by the TMAIN pin input 1: Refer to the following table.

	Timer A pin polarity selection bit	
TMAIN pin input	"0"	"1"
"L"	Stop counting	Counting
"H"	Counting	Stop counting

bp	Flag	Description	Setting condition
9-8	TMUD1 TMUD0	Up/down counting selection	00: Up counting 01: Down counting 10: Up counting (when “H” level is input to the TMAIN pin) Down counting (when “L” level is input the TMAIN pin) 11: Up counting (when “L” level is input the TMAIN pin) Down counting (when “H” level is input to the TMAIN pin) When the 2-phase encoding (1-fold, 4-fold) is selected as the count clock source, set “00”.
7	TMCNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TMLDE	Timer initialization	0: Normal operation 1: Initialization TMBC=0x0000 When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.
5-3	-	-	-
2-0	TMCK2 TMCK1 TMCK0	Timer count clock source selection	000: IOCLK 001: IOCLK/8 010: Timer 0 underflow 011: Timer 1 underflow 100: 2-phase encoding (1-fold) 101: 2-phase encoding (4-fold) 110: TMBIN pin input (both edges) 111: TMBIN pin input (single edge) When pin input (single edge) is selected by the timer, the edge selected by the B pin polarity selection bit of the TMMDB register is counted. When using IOCLK/8, operation must be enabled by the prescaler control registers (TMPSCNE).

■ Timer 11 Mode Register (TM11MD: 0x0000A260) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	TMXF	Timer operation display	0: Timer stopping 1: Timer operating
14	-	-	-
13	TMTGE	Timer external trigger enable	0: Timer activation disabled by external trigger (trigger input ignored) 1: Timer start when the falling edge is input (when timer A pin polarity selection bit is “0”) Timer start when the rising edge is input (when timer A pin polarity selection bit is “1”)
12	TMONE	Timer 1-shot operation enable	0: 1-shot operation disabled (timer does not stop) 1: 1-shot operation enabled (timer stops when TMBC and TMCA match)
11	TMCLE	Timer binary counter enable	0: Clear operation disabled 1: Clear operation enabled When the TMCA is set to a compare register TMBC is cleared when the TMBC and the TMCA match. When the TMCA is set to a capture register TMBC is cleared when captured to TMCA.
10	TMCGE	Timer count control input enable	0: Count control disabled by the TMAIN pin input 1: Refer to the following table.

	Timer A pin polarity selection bit	
TMAIN pin input	"0"	"1"
"L"	Stop counting	Counting
"H"	Counting	Stop counting

bp	Flag	Description	Setting condition
9-8	TMUD1 TMUD0	Up/down counting selection	00: Up counting 01: Down counting 10: Up counting (when “H” level is input to the TMAIN pin) Down counting (when “L” level is input the TMAIN pin) 11: Up counting (when “L” level is input the TMAIN pin) Down counting (when “H” level is input to the TMAIN pin) When the 2-phase encoding (1-fold, 4-fold) is selected as the count clock source, set “00”.
7	TMCNE	Timer operation enable	0: Operation disabled 1: Operation enabled
6	TMLDE	Timer initialization	0: Normal operation 1: Initialization TMBC=0x0000 When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.
5-3	-	-	-
2-0	TMCK2 TMCK1 TMCK0	Timer count clock source selection	000: IOCLK 001: IOCLK/8 010: Timer 4 underflow 011: Timer 5 underflow 100: 2-phase encoding (1-fold) 101: 2-phase encoding (4-fold) 110: TMBIN pin input (both edges) 111: TMBIN pin input (single edge) When pin input (single edge) is selected by the timer, the edge selected by the B pin polarity selection bit of the TMMDB register is counted. When using IOCLK/8, operation must be enabled by the prescaler control registers (TMPSCNE).

■ Timer 12 Mode Register (TM12MD: 0x0000A280) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	TMXF	Timer operation display	0: Timer stopping 1: Timer operating
14	-	-	-
13	TMTGE	Timer external trigger enable	0:Timer activation disabled by PWM0 1: Timer activation enabled by PWM0 When timer activation is enable by PWM0, set the activation trigger polarity selection of the timer 12 compare A mode register to “1”.
12	TMONE	Timer 1-shot operation enable	0 : 1-shot operation disabled (Timer does not stop.) 1: 1-shot operation enabled (Timer stops when the TMBC and the TMCA match.)
11	TMCLE	Timer binary counter enable	0: Clear operation disabled 1: Clear operation enabled When the TMCA is set to a compare register TMBC is cleared when the TMBC and the TMCA match. When the TMCA is set to a capture register TMBC is cleared when captured to TMCA.
10	TMCGE	Reserved	Always set to “0”
9-8	TMUD1 TMUD0	Up/down counting selection	00: Up counting 01: Down counting 10: Setting prohibited 11: Setting prohibited
7	TMCNE	TImer operation enable	0: Operation disabled 1: Operation enabled
6	TMLDE	Timer initialization	0: Normal operation 1: Initialization TMBC=0x0000 When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.
5-3	-	-	-
2-0	TMCK2 TMCK1 TMCK0	Timer count clock source selection	000: IOCLK, MCLK 001: IOCLK/8, MCLK/8 010: Timer 6 underflow 011: Timer 7 underflow 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited When using IOCLK/8, operation must be enabled by the prescaler control registers (TMPSCNE). When using MCLK, select MCLK by the clock source selection register (TMnCLK).

■ Timer 13 Mode Register (TM13MD: 0x0000A2A0) [8, 16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0
At reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	TMXF	Timer operation display	0: Timer stopping 1: Timer operating
14	-	-	-
13	TMTGE	Timer external trigger enable	0:Timer activation disabled by PWM1 1: Timer activation enabled by PWM1 When timer activation is enable by PWM1, set the activation trigger polarity selection of the timer 13 compare A mode register to “1”.
12	TMONE	Timer 1-shot operation enable	0 : 1-shot operation disabled (Timer does not stop.) 1: 1-shot operation enabled (Timer stops when the TMBC and the TMCA match.)
11	TMCLE	Timer binary counter enable	0: Clear operation disabled 1: Clear operation enabled When the TMCA is set to a compare register TMBC is cleared when the TMBC and the TMCA match. When the TMCA is set to a capture register TMBC is cleared when captured to TMCA.
10	TMCGE	Reserved	Always set to “0”
9-8	TMUD1 TMUD0	Up/down counting selection	00: Up counting 01: Down counting 10: Setting prohibited 11: Setting prohibited
7	TMCNE	TImer operation enable	0: Operation disabled 1: Operation enabled
6	TMLDE	Timer initialization	0: Normal operation 1: Initialization TMBC=0x0000 When the TMCA and TMCB are set to the compare register of the double buffer, the value is loaded into the compare register from the buffer. Pin output is initialized.
5-3	-	-	-
2-0	TMCK2 TMCK1 TMCK0	Timer count clock source selection	000: IOCLK, MCLK 001: IOCLK/8, MCLK/8 010: Timer 6 underflow 011: Timer 7 underflow 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited When using IOCLK/8, operation must be enabled by the prescaler control registers (TMPSCNE). When using MCLK, select MCLK by the clock source selection register (TMnCLK).

■ Timer 8 Compare/Capture A Mode Register (TM8MDA: 0x0000A204) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMAM1 TMAM0	Timer compare/capture A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer A pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer A pin polarity selection is ignored.		
5	TMAEG	Timer A pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Falling edge
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Rising edge
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMACE	Timer capture A operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMA01 TMA00	Timer A output waveform selection	00: Set when TMBC and TMCA match, reset when TMBC and TMCB match 01: Set when TMBC and TMCA match, reset when TMBC overflows 10: Set when TMBC and TMCA match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCA match)		

■ Timer 9 Compare/Capture A Mode Register (TM9MDA: 0x0000A224) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMAM1 TMAM0	Timer compare/capture A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer A pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer A pin polarity selection is ignored.		
5	TMAEG	Timer A pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Falling edge
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Rising edge
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMACE	Timer capture A operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMA01 TMA00	Timer A output waveform selection	00: Set when TMBC and TMCA match, reset when TMBC and TMCB match 01: Set when TMBC and TMCA match, reset when TMBC overflows 10: Set when TMBC and TMCA match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCA match)		

■ Timer 10 Compare/Capture A Mode Register (TM10MDA: 0x0000A0244) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMAM1 TMAM0	Timer compare/capture A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer A pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer A pin polarity selection is ignored.		
5	TMAEG	Timer A pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Falling edge
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Rising edge
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMACE	Timer capture A operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMA01 TMA00	Timer A output waveform selection	00: Set when TMBC and TMCA match, reset when TMBC and TMCB match 01: Set when TMBC and TMCA match, reset when TMBC overflows 10: Set when TMBC and TMCA match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCA match)		

■ Timer 11 Compare/Capture A Mode Register (TM11MDA: 0x0000A264) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMAM1 TMAM0	Timer compare/capture A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer A pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer A pin polarity selection is ignored.		
5	TMAEG	Timer A pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Falling edge
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count control	Counts when “H” level is input
				Activation trigger	Rising edge
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMACE	Timer capture A operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMA01 TMA00	Timer A output waveform selection	00: Set when TMBC and TMCA match, reset when TMBC and TMCB match 01: Set when TMBC and TMCA match, reset when TMBC overflows 10: Set when TMBC and TMCA match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCA match)		

■ Timer 12 Compare A Mode Register (TM12MDA: 0x0000A284) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition
7-6	TMAM1 TMAM0	Timer compare A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Setting prohibited 11: Setting prohibited
5	TMAEG	Activation trigger polarity selection	0: Rising edge 1: Falling edge Set to “1” for timer activation by PWM0
4	TMACE	Reserved	Always set to “0”
3-2	-	-	-
1-0	TMA01 TMA00	Reserved	Always set to “00”

■ Timer 13 Compare A Mode Register (TM13MDA: 0x0000A2A4) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM A01	TM A00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition
7-6	TMAM1 TMAM0	Timer compare A operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Setting prohibited 11: Setting prohibited
5	TMAEG	Activation trigger polarity selection	0: Rising edge 1: Falling edge Set to “1” for timer activation by PWM0
4	TMACE	Reserved	Always set to “0”
3-2	-	-	-
1-0	TMA01 TMA00	Reserved	Always set to “00”

■ Timer 8 Compare/Capture B Mode Register (TM8MDB: 0x0000A205) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMBM1 TMBM0	Timer compare/capture B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer B pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer B pin polarity selection is ignored.		
5	TMBEG	Timer B pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count source	Rising edge (when single edge is selected)
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count source	Falling edge (when single edge is selected)
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMBCE	Timer capture B operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMB01 TMB00	Timer B output waveform selection	00: Set when TMBC and TMCB match, reset when TMBC and TMCA match 01: Set when TMBC and TMCB match, reset when TMBC overflows 10: Set when TMBC and TMCB match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCB match)		

■ Timer 9 Compare/Capture B Mode Register (TM9MDB: 0x0000A225) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMBM1 TMBM0	Timer compare/capture B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer B pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer B pin polarity selection is ignored.		
5	TMBEG	Timer B pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count source	Rising edge (when single edge is selected)
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count source	Falling edge (when single edge is selected)
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMBCE	Timer capture B operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMB01 TMB00	Timer B output waveform selection	00: Set when TMBC and TMCB match, reset when TMBC and TMCA match 01: Set when TMBC and TMCB match, reset when TMBC overflows 10: Set when TMBC and TMCB match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCB match)		

■ Timer 10 Compare/Capture B Mode Register (TM10MDB: 0x0000A245) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMBM1 TMBM0	Timer compare/capture B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer B pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer B pin polarity selection is ignored.		
5	TMBEG	Timer B pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count source	Rising edge (when single edge is selected)
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count source	Falling edge (when single edge is selected)
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMBCE	Timer capture B operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMB01 TMB00	Timer B output waveform selection	00: Set when TMBC and TMCB match, reset when TMBC and TMCA match 01: Set when TMBC and TMCB match, reset when TMBC overflows 10: Set when TMBC and TMCB match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCB match)		

■ Timer 11 Compare/Capture B Mode Register (TM11MDB: 0x0000A265) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition		
7-6	TMBM1 TMBM0	Timer compare/capture B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Capture register (single-edge operation) Capture at the edge selected by timer B pin polarity selection bit. 11: Capture register (both-edge operation) Selection by timer B pin polarity selection is ignored.		
5	TMBEG	Timer B pin polarity selection	0	Capture	Rising edge (when single edge is selected)
				Count source	Rising edge (when single edge is selected)
				Pin output	Positive polarity output “L” level when reset, “H” level when set
			1	Capture	Falling edge (when single edge is selected)
				Count source	Falling edge (when single edge is selected)
				Pin output	Negative polarity output “H” level when reset, “L” level when set
4	TMBCE	Timer capture B operation enable	0: Capture operation disabled (pin input is ignored) 1: Capture operation enabled		
3-2	-	-	-		
1-0	TMB01 TMB00	Timer B output waveform selection	00: Set when TMBC and TMCB match, reset when TMBC and TMCA match 01: Set when TMBC and TMCB match, reset when TMBC overflows 10: Set when TMBC and TMCB match (reset only when timer is initialized) 11: Timer output (output is inverted when TMBC and TMCB match)		

■ Timer 12 Compare B Mode Register (TM12MDB: 0x0000A285) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition
7-6	TMBM1 TMBM0	Timer compare B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Setting prohibited 11: Setting prohibited
5	TMBEG	Reserved	Always set to “0”
4	TMBCE	Reserved	Always set to “0”
3-2	-	-	-
1-0	TMB01 TMB00	Reserved	Always set to “00”

■ Timer 13 Compare B Mode Register (TM13MDB: 0x0000A2A5) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM B01	TM B00
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R/W	R/W

bp	Flag	Description	Setting condition
7-6	TMBM1 TMBM0	Timer compare B operation mode selection	00: Compare register (double buffer) 01: Compare register (single buffer) 10: Setting prohibited 11: Setting prohibited
5	TMBEG	Reserved	Always set to “0”
4	TMBCE	Reserved	Always set to “0”
3-2	-	-	-
1-0	TMB01 TMB00	Reserved	Always set to “00”

9.3 Prescaler

9.3.1 Prescaler Operation

■ Prescaler operation

Prescaler outputs IOCLK/8 and IOCLK/64 with using IOCLK as an input clock and MCLK/8 with using MCLK as an input clock.

■ Count Source and Prescaler

When IOCLK/8, IOCLK/64 or MCLK/8 is selected as a timer count source, the setting of the prescaler is necessary. Table: 9.3.1 shows the count clock source and controlled registers.

Table:9.3.1 Count Source and Prescaler

Count clock source	Setting of prescaler	Set register
IOCLK (Timer 8 to 13)	-	-
IOCLK/8 (Timer 8)	O	TM8PSC
IOCLK/8 (Timer 9)	O	TM9PSC
IOCLK/8 (Timer 10)	O	TM10PSC
IOCLK/8 (Timer 11)	O	TM11PSC
IOCLK/8 (Timer 12)	O	TM12PSC
IOCLK/8 (Timer 13)	O	TM13PSC
IOCLK/64 (Timer 8)	O	TMEXPPSC16
IOCLK/64 (Timer 9)	O	TMEXPPSC16
MCLK (Timer 12 to 13))	-	TMnCLKSEL
MCLK/8 (Timer 12)	O	TM12PSC, TM12CLKSEL
MCLK/8 (Timer 13)	O	TM13PSC, TM13CLKSEL
Timer n underflow	-	-
TImer pin input	-	-

When selecting MCLK or MCLK/8, the setting of the TMnCLKSEL register is necessary.

9.3.2 Setup Example

■ Setup Example

Timer function can be set by using timer 8 that generates the constant interrupts. Interrupts are generated every 1 ms by selecting the clock source IOCLK/8 and using the prescaler function. The oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below:

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop counting of the timer 8
(2) Set the compare/capture register TM8CA(0x0000A208)=0x0EA5	(2) Set the interrupt generation cycle to the timer 8 compare/capture A register (TM8CA). The setting is 3749 (0x0EA5) due to 3750 counts.
(3) Set the prescaler TM8PSC(0x0000A214) bp7: TMPSCNE=1	(3) Set the TMPSCNE flag of the prescaler control register (TM8PSC) to “1” to enable the prescaler operation.
(4) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=001	(4) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(5) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(5) Select the timer up count by the TMUD1-0 flag of the TM8MD register.
(6) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(6) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(7) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1 -0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(8) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(8) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register buffer is loaded into the TM8CA register. Reset the TMLDE flag to “0” after setting.
(9) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(9) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

9.4 Interval Timer

9.4.1 Interval Timer Function Operation

Interval timer function is the function which can generate the interrupts repeatedly at regular time intervals.

■ Clock Source Selection

The generation cycle of timer interrupts is set in advance by the clock source selection and the setting value of the base register (TMnBR). The clock source can be selected by the timer as below.

Table:9.4.1 Clock Source at Timer Operating and 1 Count Time

Clock source	1 count time	Timer 8	Timer 9	Timer 10	Timer 11
IOCLK	33.3 ns	O	O	O	O
IOCLK/8	266.7 ns	O	O	O	O
IOCLK/64	2.1 µs	O	O	-	-
Timer underflow	-	Timer 2	Timer 3	Timer 0 Timer 1	Timer 4 Timer 5
Pin output	-	TM8BIO	TM9BIO	TM10BIO	TM11IO1

Clock source	1 count time	Timer 12	Timer 13
IOCLK	33.3 ns	O	O
IOCLK/8	266.7 ns	O	O
MCLK	16.7 ns	O	O
MCLK/8	133.3 ns	O	O
Timer underflow	-	Timer 6 Timer 1	Timer 6 Timer 7
Pin output	-	-	-

*1 count time is calculated with the oscillation frequency as 10 MHz, 6 multiplication and IOCLK/=MCLK/2.

■ Count Timing of Timer Operation

The binary counter counts up with the selected count source as a count clock. Table: 9.4.2 shows operation condition and Figure: 9.4.1 shows count timing.

Table:9.4.2 Operation Condition

Operation condition	Setting description
Timer up or down selection	Up count
Timer compare/capture A mode operation mode selection	Compare register (double buffer)
Timer counter clear enable	Clear operation enabled

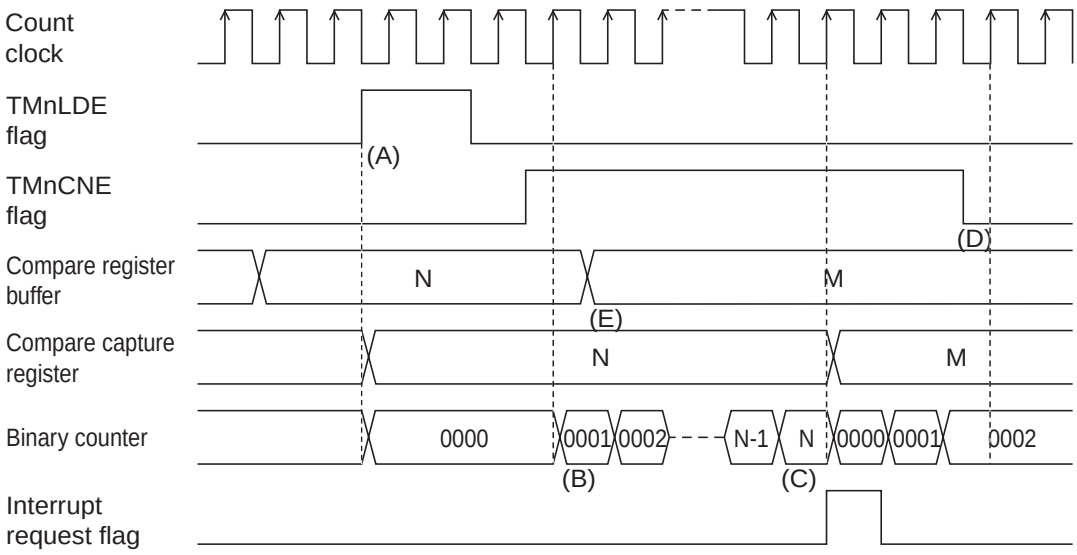


Figure:9.4.1 Count Timing of Timer Operation

(A) When initialization (“1”) is written to the TMLDE flag, the value of the compare register buffer is loaded into the compare/capture register, and the binary counter is initialized to 0x0000. The pin output (TMnOUT) is reset to “L”. Reset the TMnLDE flag to “0” after setting.

(B) When the TMCNE flag is set to the operation enabled (“1”), the binary counter starts to count up. The binary counter counts at the rising edge of the count clock.

(C) The timer compare/capture interrupt request is generated when counting up is started from matching of the binary counter and the compare/capture register. The binary counter is initialized to 0x0000 and starts to count up again.

(D) When the TMCNE flag is set to the operation disabled (“0”), counting up is stopped. The status of the binary counter is retained after the timer is stopped, if the TMLDE flag is not set to be initialized (“1”).When the TMCNE flag is set to operation enabled (“1”), counting up can be restarted from the status just before the timer was stopped.

(E) When the value of the compare register buffer is changed during the counting up operation, the value of the compare register buffer is loaded into the compare/capture register at the next counting up operation from matching condition of the binary counter and compare/capture register.

9.4.2 Setup Example

■ Interval Timer Setup Example

Timer function can be set by using timer 8 that generates the constant interrupts. Interrupts are generated every 1 ms by selecting the clock source IOCLK. The oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop the timer 8 counting.
(2) Disable the interrupt G7ICR(0x0000891C) bp8: G7IE1=0	(2) Set the G7IE1 flag of the G7ICR register to “0” to disable the interrupt.
(3) Set the interrupt generation cycle TM8CA(0x0000A208)=0x752F	(3) Set the interrupt generation cycle to the timer 8 compare/capture A register (TM8CA). The setting is 29999 (0x752F) due to 30000 counts.
(4) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(4) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(5) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(5) Select the timer up count by the TMUD1-0 flag of the TM8MD register.
(6) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(6) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(7) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1 -0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(8) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(8) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register buffer is loaded into the TM8CA register. Reset the TMLDE flag to “0” after setting.
(9) Set the interrupt level G7ICR(0x0000891C) bp14-12: G7LV2-0=100	(9) Set the interrupt level by the G7LV2-0 flag of the G7ICR register. When the interrupt request flag may be set already, clear the request flag.
(10) Enable the interrupt G7ICR(0x0000891C) bp8: G7IE1=1	(10) Set the G7IE1 flag of the G7ICR register to “1” to enable the interrupt.

Setup Procedure	Description
(11) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(11) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

TM8BC counter starts to count up. When the TM8BC counter and the TM8CA match, the timer 8 compare/capture A interrupt is generated at the rising edge of the next count clock. The interrupt request flag is set and the value of the TM8BC counter is initialized to 0x0000 and starts to count up again.

Timer interrupt generation cycle = (TMnCA setting + 1) × Count clock source

9.5 Event Count

9.5.1 Event Count Operation

Event count operation is to count the edge selected by the TMnBIN pin as a count clock. Also, it can mask (stop counting) the count clock by the TMnAIN pin.

■ Event Count Operation

When the TMnBIN pin is selected to a clock source, the event counter operates. The event count operation means that the binary counter (TMnBC) counts up (or count down) the external signal input to the TMnIO pin as a count clock

■ Event Count Input Pin

Table: 9.5.1 shows event count input pins.

Table:9.5.1 Event Count Input Pin

	Timer 8	Timer 9	Timer 10	Timer 11	Timer 12	Timer 13
Input pin	TM8BIO	TM9BIO	TM10BIO	TM11IO1	-	-

When pins are used as event count input, the settings of the following registers are necessary.

Table:9.5.2 Setting Input Pin

	Port output mode register	Port I/O control register
TM8BIO	P3MD(P37M)	P3DIR(P37D)
TM9BIO	P4MD(P43M)	P4DIR(P43D)
TM10BIO	P4MD(P47M)	P4DIR(P47D)
TM11IO1	P7MD(P73M)	P7DIR(P73D)

The settings of the following registers are necessary for the count edges of event input pins.

When the count edge is single edge, the setting of the TMBEG flag of the timer compare/capture B mode register is necessary.

Table:9.5.3 Setting Count Edge of Event Input Pin

	Timer mode register	Timer compare/capture B mode register
TM8BIO	TM8MD(TMCK2 to 0)	TM8MDB(TMBEG)
TM9BIO	TM9MD(TMCK2 to 0)	TM9MDB(TMBEG)
TM10BIO	TM10MD(TMCK2 to 0)	TM10MDB(TMBEG)
TM11IO1	TM11MD(TMCK2 to 0)	TM11MDB(TMBEG)

■ Count Timing of Event Count Operation

TMnBIN pin input is sampled by IOCLK. The edge selected by the TMnBIN pin input is counted, and the binary counter counts up. The pulse width should be IOCLK × 1.5 or more for detecting the edge. Table: 9.5.4 shows operation condition and Figure: 9.5.1 the count timing.

Table:9.5.4 Operation Condition

Operation condition	Setting description
Input edge	Rising edge
Timer up/down selection	Up counting
Timer compare/capture A operation mode selection	Compare register (single buffer)
Timer counter clear enable	Clear operation enabled

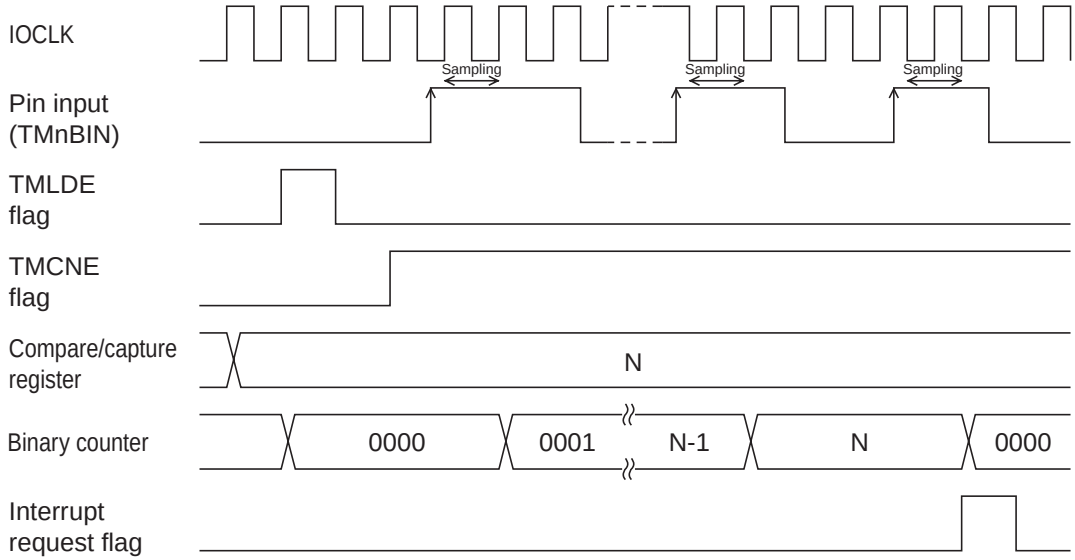


Figure:9.5.1 Count Timing of Event Count Operation

■ Setting the Count Control Input

The count clock of the binary counter can masked based on the input level of the TMnMAIN pin. The timer count control input is enabled by setting the TMCGE flag of the timer mode register (TMnMD) to “1”. The input level for masking is set by the TMAEG flag of the timer compare/capture A mode register (TMnMDA). Table: 9.5.5 shows the relationship between the input level and TMAEG flag.

Table:9.5.5 Input Level and TMAEG flag

TMnAIN pin	TMAEG flag (TMnMDA register)	
	0	1
"H"	Normal operation (counting)	Count clock masked (stop counting)
"L"	Count clock masked (stop counting)	Normal operation (counting)

■ Count Timing of Count Control Input

Count timing of count control input is shown below. The TMAEG flag is set to “0”.

When the TMnAIN pin is set to “L”, counting up stops.

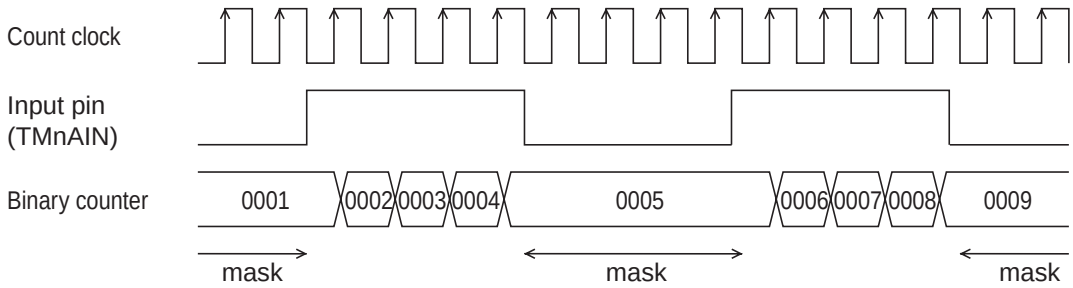


Figure:9.5.2 Count Timing of Count Control Input

■ Setting the Compare Register

Event count numbers are set for generating interrupts to the compare/capture register TMnCA (B).

Interrupt generation count numbers = TMnCA (B) + 1 (time)

9.5.2 Setup Example

■ Event Count Setup Example

If the rising edge of the TM8BIO input pin is detected 5 times with the timer 8, an interrupt is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop the timer 8 counting.
(2) Disable the interrupt G7ICR(0x0000891C) bp8: G7IE1=0	(2) Set the G7IE1 flag of the G7ICR register to “0” to disable the interrupt.
(3) Set the interrupt generation cycle TM8CA(0x0000A208)=0x0004	(3) Set the interrupt generation cycle to the timer 8 compare/capture register (TM8CA). The setting value is 4(0x0004) due to 5 times.
(4) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=111	(4) Select the count clock source(TM8BIO pin) by the TMCK2-0 flag of the TM8MD register.
(5) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(5) Select the timer up count by the TMUD1-0 flag of the TM8MD register.
(6) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(6) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(7) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1 -0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(8) Select the timer B pin polarity TM8MDB(0x0000A205) bp5: TMBEG=0	(8) Set the edge (rising edge or falling edge) at single edge of the input pin of the count clock source to “0” by the TMBEG flag of the timer 8 compare/capture B mode register(TM8MDB); then, set the rising edge.
(9) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(9) Set the TMLDE flag of the TM8MD register to “1” to initialize the binary counter. Reset the TMLDE flag to “0” after setting.
(10) Set the interrupt level G7ICR(0x0000891C) bp14-12: G7LV2-0=100	(10) Set the interrupt level by the G7LV2-0 flag of the G7ICR register. If the interrupt request flag has been set already , clear the request flag.

Setup Procedure	Description
(11) Enable the interrupt G7ICR(0x0000891C) bp8: G7IE1=1	(11) Set the G7IEO flag of the G7ICR register to “1” to enable the interrupt.
(12) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(12) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

9.6 Up/Down Counting

9.6.1 Up/Down Counting Operation

Up/down counting is the function that the binary counter counts up or down according to the condition of the input pin.

■ Input Pin

Table: 9.6.1 shows the pins for up/down counting.

Table:9.6.1 Timer and Up/Down Counting Input Pin

	Timer 8	Timer 9	Timer 10	Timer 11	Timer 12	Timer 13
Input pin	TM8AIO TM8BIO	TM9AIO TM9BIO	TM10AIO TM10BIO	TM11IO0 TM11IO1	-	-

When pins are used as up/down count input, the settings of the following registers are necessary.

Table:9.6.2 Setting Input Pin

	Port output mode register	Port I/O control register
TM8AIO	P3MD(P36M)	P3DIR(P36D)
TM8BIO	P3MD(P37M)	P3DIR(P37D)
TM9AIO	P4MD(P42M)	P4DIR(P42D)
TM9BIO	P4MD(P43M)	P4DIR(P43D)
TM10AIO	P4MD(P46M)	P4DIR(P46D)
TM10BIO	P4MD(P47M)	P4DIR(P47D)
TM11IO0	P7MD(P72M)	P7DIR(P72D)
TM11IO1	P7MD(P73M)	P7DIR(P73D)

■ Setting Up/Down Counting (1-fold, 2-phase encoding)

Select “1-fold and 2-phase encoding” by the timer count clock source selection of the timer mode register (TMnMD). The binary counter counts up at the rising edge of the TMnBIN pin when the TMnAIN pin is set to “1” and counts down at the falling edge as indicated in the following table. When the TMnAIN pin is “L”, counting is not operated. When “1-fold and 2-phase encoding” is set, The TMUD1-0 flag of the TMnMD register is set to “00” to specify up counting.

Table:9.6.3 Operation Condition of 1-fold, 2-phase encoding

TMnAIN pin	TMnBIN pin	
	↑	↓
"H"	Up counting	Down counting
"L"	-	-

■ Setting Up/Down Counting (4-fold, 2-phase encoding)

Select “4-fold and 2-phase encoding” by the timer count clock source selection of the timer mode register (TMnMD). The counting up/down condition is as shown in the following table. When “4-fold and 2-phase encoding” is set, the TMUD1-0 flag of the TMnMD register is set to “00” to specify up counting.

Table:9.6.4 Setting Condition of 4-fold, 2-phase encoding

TMnAIN pin	TMnBIN pin			
	"H"	"L"	↑	↓
"H"	-	-	Up counting	Down counting
"L"	-	-	Down counting	Up counting
↑	Down counting	Up counting	-	-
↓	Up counting	Down counting	-	-

■ Setting Up/Down Counting (Count Clock)

The binary counters counts up or down by the condition of the input pin at the timing of the count clock.

Select “10, or “11” by the timer up/down selection of the timer mode register (TMnMD). The counting up/down condition is as shown in the following table.

Table:9.6.5 Operation Condition of Count Clock

TMnAIN pin	At count clock timing	
	TMUD1 to 0 flag (TMnMD register)	
	10	11
"H"	Up counting	Down counting
"L"	Down counting	Up counting

■ Count TIming of Up/Down Counting

It is indicated that the count timing goes up or down according to the input pin (TMnAIN pin) at the timing of the count clock.

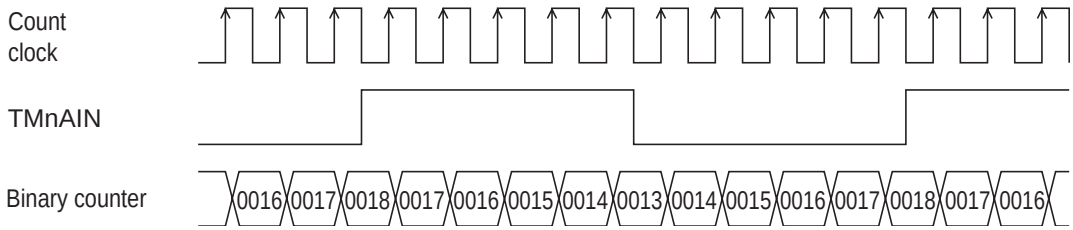


Figure:9.6.1 Count Timing of Up/Down Counting (TMUD1-0=”11”)

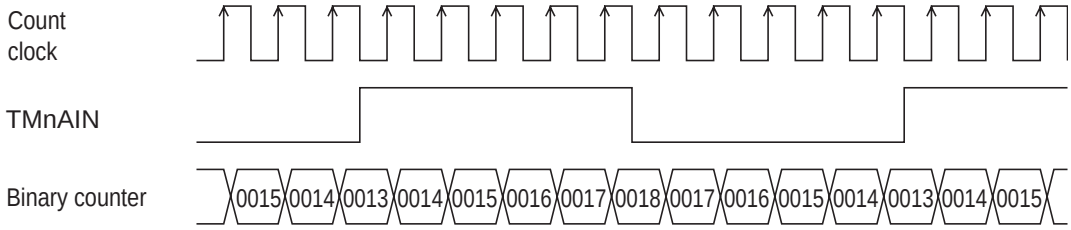


Figure:9.6.2 Count Timing of Up/Down Counting (TMUD1-0=”10”)

9.6.2 Setup Example

■ Up/Down Counting Setup Example

The binary counter counts up when the external input signal(TM8AIO) is “H” and counts down when it is “L” at timing of the timer 8 count clock. The count clock is IOCLK, and the oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register (TM8MD) to the timer 8 counting.
(2) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(2) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(3) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=10	(3) Set the TMUD1-0 flag of the TM8MD register to “10”; and, select up counting when the TMnAIN pin is at “H” level and down counting when the TMnAIN pin is input at “L” level input.
(4) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(4) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC register. The TM8BC counter is cleared.
(5) Set the input pin (pin function) P3MD(0x0000A033) bp6: P36M=1	(5) Set the P36M flag of the port 3 output mode register (P3MD) to “1” to set the port to pin function.
(6) Set the input pin (I/O function) P3DIR(0x0000A023) bp0: P36D=0	(6) Set the P36D flag of the port 3 I/O control register (P3DIR) to “0” to set the port to the input pin.
(7) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(7) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the binary counter (TM8BC) is initialized to 0x0000. Reset the TMLDE flag to “0” after setting.
(8) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(8) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

The binary counter counts up when the TM8AIO pin is set to “H”, and counts down when the TM8AIO pin is set to “L”. The binary counts up or down according to the condition of the pin.

9.7 Timer Output

9.7.1 Timer Output Operation

Timer output is the function which inverts output levels of pins every regular cycles.

■ Output Pin

Table; 9.7.1 shows timer output pins.

Table:9.7.1 Timer and Timer Output Pin

	Timer 8	TImer 9	Timer 10	Timer 11	Timer 12	Timer 13
Output pin	TM8AIO TM8BIO	TM9AIO TM9BIO	TM10AIO TM10BIO	TM11IO0 TM11IO1	-	-

When pins are used as timer output, the settings of the following registers are necessary.

Table:9.7.2 Setting Output Pin

	Port output mode register	Port I/O control register
TM8AIO	P3MD(P36M)	P3DIR(P36D)
TM8BIO	P3MD(P37M)	P3DIR(P37D)
TM9AIO	P4MD(P42M)	P4DIR(P42D)
TM9BIO	P4MD(P43M)	P4DIR(P43D)
TM10AIO	P4MD(P46M)	P4DIR(P46D)
TM10BIO	P4MD(P47M)	P4DIR(P47D)
TM11IO0	P7MD(P72M)	P7DIR(P72D)
TM11IO1	P7MD(P73M)	P7DIR(P73D)

■ Setting Timer Output

Select “timer output” by the timer output waveform selection flag of the timer compare/capture mode register. Timer pin polarity selection is the flag which sets the initial value of pin output. When it is set to “0”, the initial value is “L” and when it is set to “1”, the initial value is “H”. The registers and flags that set output pins are shown below.

Table:9.7.3 Selecting Timer Output Waveform and Timer Pin Polarity

	TImer output waveform selection	Timer pin polarity selection
TM8AIO	TM8MDA(TMAO1-0)	TM8MDA(TMAEG)
TM8BIO	TM8MDB(TMBO1-0)	TM8MDB(TMBEG)
TM9AIO	TM9MDA(TMAO1-0)	TM9MDA(TMAEG)
TM9BIO	TM9MDB(TMBO1-0)	TM9MDB(TMBEG)
TM10AIO	TM10MDA(TMAO1-0)	TM10MDA(TMAEG)
TM10BIO	TM10MDB(TMBO1-0)	TM10MDB(TMBEG)
TM11IO0	TM11MDA(TMAO1-0)	TM11MDA(TMAEG)
TM11IO1	TM11MDA(TMAO1-0)	TM11MDA(TMAEG)

■ Count TIming of Timer Output

Counting up starts from matching condition of the binary counter and the compare/capture register, the output pin is inverted to operate timer output. Table; 9.7.4 shows the preconditions for count timing of timer output and Figure; 9.7.1 shows count timing.

Table:9.7.4 Precondition for Count Timing of Timer Output

Operation condition	Setting description
TImer up/down selection	Up counting
TImer compare/capture operation mode selection	Compare register (single buffer)
Timer output waveform selection	TImer output
Timer pin polarity selection	Positive polarity output (“L” level at reset)
Timer counter clear enable	Clear operation enabled

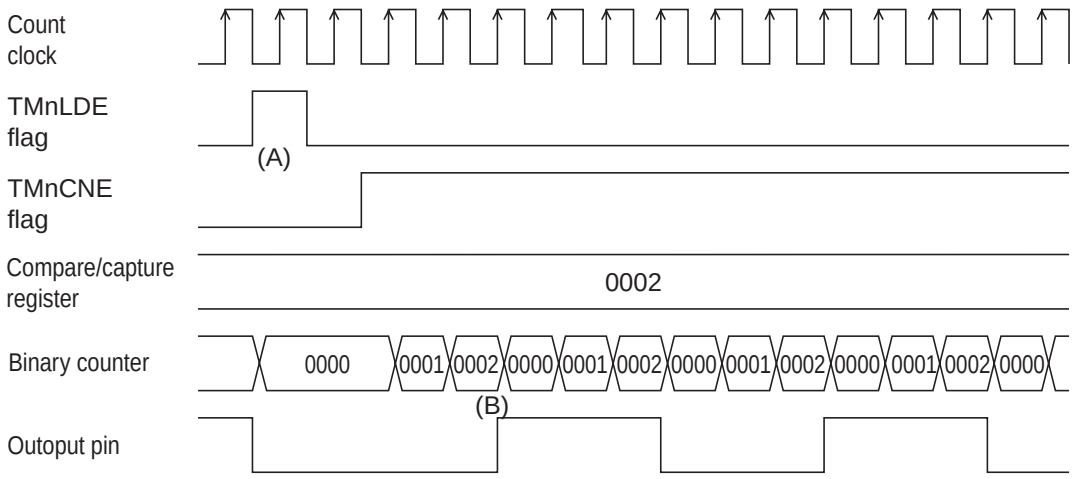


Figure:9.7.1 Count Timing of Timer Output

(A) When initialization (“1”) is written to the TMLDE flag, the binary counter is initialized to 0x0000. The pin output (TMnOUT) is initialized to the value which is set by the timer pin polarity selection of the timer compare/capture mode register. Reset the TMLDE flag to “0” after setting.

(B) Counting up starts from matching condition of the binary counter and the compare/capture register, the output pin is inverted. The binary counter is initialized to 0x0000 and restarts the counting up operation.

9.7.2 Setup Example

■ TImer Output Setup Example

The output pin (TM8AIO) using timer 8 outputs waveforms as shown below (repeating “L” output for 1ms and “H” output for the next 1ms). IOCLK is selected as clock source to match the binary counter and the compare/capture register for every 1 ms. The oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

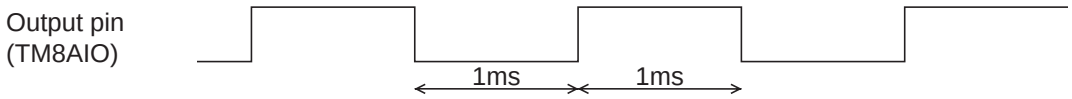


Figure:9.7.2 Timer Output Setup Example

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop the timer 8 counting.
(2) Set the repeating cycle TM8CA(0x0000A208)=0x752F	(2) Set the repeating cycle to the timer 8 compare/capture A register (TM8CA). The setting value is 29999 (0x752F) due to 30000 counts.
(3) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(3) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(4) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(4) Select the timer up counting by the TMUD1-0 flag of the TM8MD register.
(5) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(5) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(6) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(6) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1-0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(7) Select the timer A pin polarity TM8MDA(0x0000A204) bp5: TMAEG=0	(7) Set the TMAEG flag of the TM8MDA register to “0” to set the initial condition of the pin output to “L”. When the initial condition of the pin output is set to “H”, set the flag to “1”.
(8) Select the timer A output waveform TM8MDA(0x0000A204) bp1-0: TMAO1-0=11	(8) Set the timer A output waveform selection to the timer output by the TMA01-0 flag of the TM8MDA register.

Setup Procedure	Description
(9) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(9) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register buffer is loaded into the TM8CA register. Reset the TMLDE flag to “0” after setting.
(10) Set the output pin (pin function) P3MD(0x0000A033) bp6: P36M=1	(10) Set the P36M flag of the port 3 output mode register (P3MD) to “1” to set the port to the pin function.
(11) Set the output pin (I/O function) P3DIR(0x0000A023) bp6: P36D=1	(11) Set the P36D flag of the port 3 I/O control register (P3DIR) to “1” to set the I/O control to the output pin.
(12) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(12) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

TM8BC counter counts up. When the TM8BC counter and the TM8CA register match, the condition of the output pin (TM8AIO) is inverted at the rising edge of the next count clock.

The value of the TM8BC counter is initialized to 0x0000 and starts to count up again.

$$\text{Timer output cycle} = (\text{TMnCA value} + 1) \times \text{Count clock source cycle} \times 2$$

9.8 PWM Output

9.8.1 PWM Output Operation

PWM output is the function that pins output the standard PWM output, which is determined by the overflow timing of the binary counter and match timing of the timer binary counter and the compare register.

■ Output Pin

Table: 9.8.1 shows PWM output pins.

Table:9.8.1 Timer and PWM Output Pin

	Timer 8	Timer 9	Timer 10	Timer 11	Timer 12	Timer 13
Output pins	TM8AIO TM8BIO	TM9AIO TM9BIO	TM10AIO TM10BIO	TM11IO0 TM11IO1	-	-

When pins are used as PWM output, the settings of the following registers are necessary.

Table:9.8.2 Setting Output PIn

	Port output mode register	Port I/O control register
TM8AIO	P3MD(P36M)	P3DIR(P36D)
TM8BIO	P3MD(P37M)	P3DIR(P37D)
TM9AIO	P4MD(P42M)	P4DIR(P42D)
TM9BIO	P4MD(P43M)	P4DIR(P43D)
TM10AIO	P4MD(P46M)	P4DIR(P46D)
TM10BIO	P4MD(P47M)	P4DIR(P47D)
TM11IO0	P7MD(P72M)	P7DIR(P72D)
TM11IO1	P7MD(P73M)	P7DIR(P73D)

■ Setting PWM Output

Select the timer output waveform selection flag of the timer compare/capture mode register.

When TM8AIO, TM9AIO, TM10AIO, TM11IO0 and TM11IO1 pins are used,
Set when TMnBC and TMnCA match, and reset when TMnBC and TMnCB match.
Set when TMnBC and TMnCA match, and reset when TMnBC overflows.
When TM8BIO, TM9BIO and TM10BI0 pins are used,
Set when TMnBC and TMnCB match, and reset when TMnBC and TMnCA match.
Set when TMnBC and TMnCB match, and reset when TMnBC overflows.

Timer pins polarity selection is a flag which is set the condition of the pin output. When it is set to “0”, the initial value is “L”, and when it is set to “1”, the initial value is “H” and the polarity at the outputs is inverted. The registers and flags set to the pins at output are shown below.

Table:9.8.3 Selecting Timer Output Waveform and Timer Pin Polarity

	Timer output waveform selection	Timer pin polarity selection
TM8AIO	TM8MDA(TMAO1-0)	TM8MDA(TMAEG)
TM8BIO	TM8MDB(TMBO1-0)	TM8MDB(TMBEG)
TM9AIO	TM9MDA(TMAO1-0)	TM9MDA(TMAEG)
TM9BIO	TM9MDB(TMBO1-0)	TM9MDB(TMBEG)
TM10AIO	TM10MDA(TMAO1-0)	TM10MDA(TMAEG)
TM10BIO	TM10MDB(TMBO1-0)	TM10MDB(TMBEG)
TM11IO0	TM11MDA(TMAO1-0)	TM11MDA(TMAEG)
TM11IO1	TM11MDA(TMAO1-0)	TM11MDA(TMAEG)

■ Count Timing of PWM Output (1)

The polarity for output pins changes by matching of the binary counter and the compare/capture A register and matching of the binary counter and the compare/capture B register. Table 9.8.4 shows the preconditions for PWM output count timing, and Figure; 9.8.1 shows count timing.

Table:9.8.4 Preconditions of Count TIming of PWM Output

Operation condition	Setting description
TImer up/down selection	Up counting
TImer compare/capture operation mode selection	Compare register (single buffer)
Timer output waveform selection	Set when TMnBC and TMnCB match Reset when TMnBC and TMnCA match
Timer pin polarity selection	Positive polarity output (TMnAEG=0) Negative polarity output (TMnAEG=1)
Timer counter clear enable	Clear operation enabled

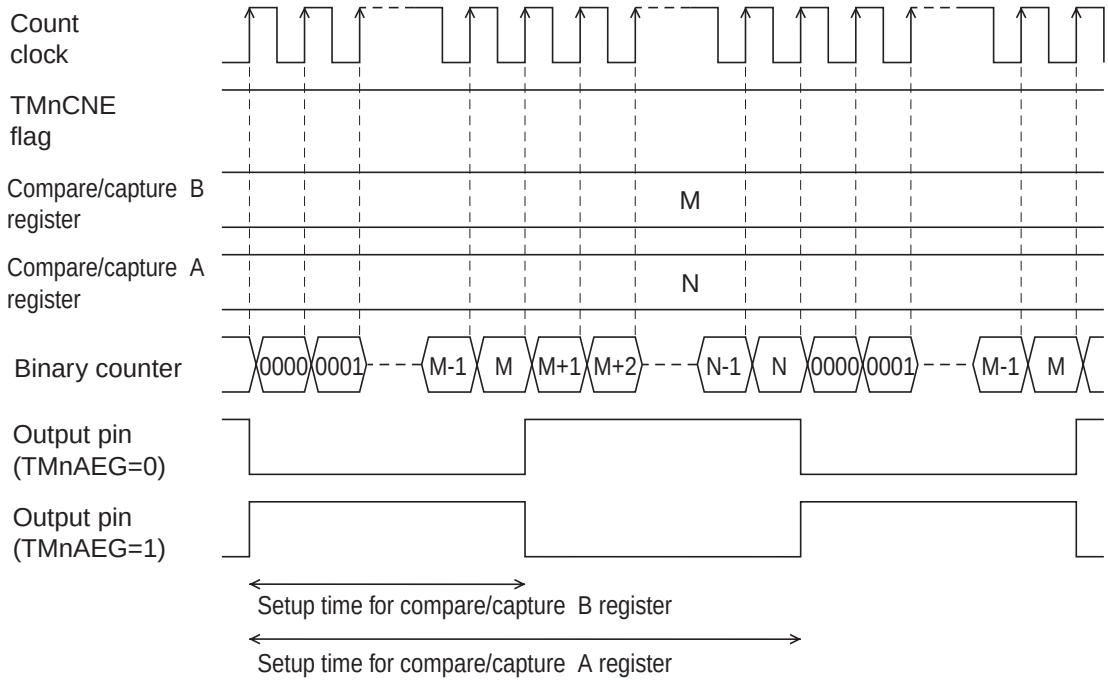


Figure:9.8.1 Count Timing of PWM Output (1)

■ Count Timing of PWM Output (2)

The output pin polarity changes by matching of the binary counter and the compare/capture A register and the overflow of the binary counter. Table; 9.8.5 shows the preconditions for count timing of PWM output, and Figure; 9.8.2 shows count timing.

Table:9.8.5 Preconditions of Count timing of PWM Output

Operation condition	Setting description
Timer up/down selection	Up counting
Timer compare/capture operation mode selection	Compare register (single buffer)
Timer output waveform selection	Set when TMnBC and TMnCA match Reset when TMnBC overflows
TImer pin polarity selection	Positive polarity output (TMnAEG=0) Negative polarity output (TMnAEG=1)
TImer counter clear enable	Clear operation disabled

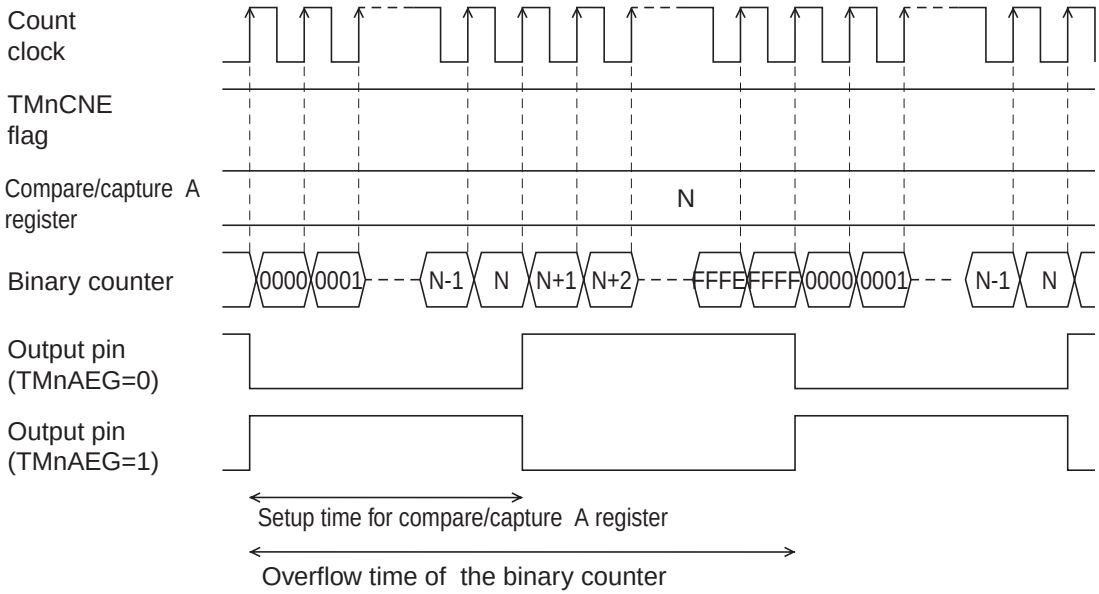


Figure:9.8.2 Count TIming of PWM Output (2)

9.8.2 Setup Example

■ PWM Output Setup Example

The output pin (TM8AIO) using timer 8 outputs waveforms as shown below (repeating “L” output for 1.5 ms and “H” output for the next 0.5 ms). IOCLK is selected as clock source to match the binary counter and the compare/capture B register for every 1.5 ms and to match the binary counter and the compare/capture A register for every 2 ms. The oscillator frequency is set to 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

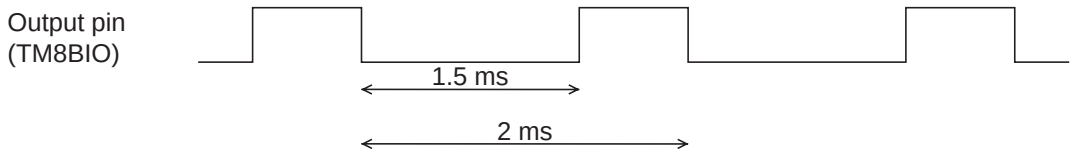


Figure:9.8.3 PWM Output Setup Example

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register to “0” to stop counting of the timer 8.
(2) Set the repeating cycle TM8CB(0x0000A20C)=0xAFC7	(2) Set the repeating cycle to the timer 8 compare/capture B register (TM8CB). Due to 45000 counts, the setting value is 44999(0xAFC7).
(3) Set the repeating cycle TM8CA(0x0000A208)=0xEA5F	(3) Set the repeating cycle to the timer 8 compare/capture A register (TM8CA). Due to 60000 counts, the setting value is 59999(0xEA5F). The setting value indicates “L+H” period.
(4) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(4) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(5) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(5) Select the timer up counting by the TMUD1-0 flag of the TM8MD register.
(6) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(6) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(7) Select the timer compare/capture B operation mode TM8MDB(0x0000A205) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1-0 flag of the timer 8 compare/capture B mode register (TM8MDB).

Setup Procedure	Description
(8) Select the timer B pin polarity TM8MDB(0x0000A205) bp5: TMBEG=0	(8) Set the TMBEG flag of the TM8MDB register to “0” to set the initial condition of pin output to “L”. Set it to “1” when the initial condition of the pin output is set to “H”.
(9) Select the timer B output waveform TM8MDB(0x0000A205) bp1-0: TMB1-0=00	(9) Set the timer B output waveform selection when the TMBC and TMCB match and reset when the TMBC and TMCA match by the TMB01-0 flag of the TM8MDB register.
(10) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(10) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register A buffer is loaded into the TM8CA register, and the value of the compare register B buffer is loaded into the TM8CB register. Reset the TMLDE flag to “0” after setting.
(11) Set the output pin (pin function) P3MD(0x0000A033) bp7: P37M=1	(11) Set the P37M flag of the port 3 output mode register (P3MD) to “1” to set the port to pin function.
(12) Set the output pin (I/O function) P3DIR(0x0000A023) bp7: P37D=1	(12) Set the P37D flag of the port 3 I/O control register (P3DIR) to “1” to set the I/O control to the output pin.
(13) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(13) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

TM8BC counter counts up. When the TM8BC counter and the TM8CB register match, the output pin (TM8BIO) is set to “H” at the rising edge of the next count clock. When the TM8BC counter and the TM8CA register match, the output pin (TM8BIO) is set to “L” at the rising edge of the next count clock. The value of the TM8BC counter is initialized to 0x0000 and counting up restarts.

9.9 Input Capture

9.9.1 Input Capture Operation

Input capture function reads the value of the binary counter into the compare/capture register at the trigger set by the external input signal (both edge, rising edge, falling edge).

■ Setting Input Capture

Set the TMACE flag of the timer compare/capture mode register to “1” to enable capture operation. Select whether to capture at the both edge or single edge of the input signal by the TMAM1-0 flag. If the single edge is selected, select the falling edge or rising edge by the TMAEG flag.

■ Setting Input Pin

Table: 9.9.1 shows the pins which can use input capture operation.

Table:9.9.1 TImer and Input Capture Input Pin

	Timer 8	Timer 9	Timer 10	Timer 11	Timer 12	Timer 13
Input pin	TM8AIO TM8BIO	TM9AIO TM9BIO	TM10AIO TM10BIO	TM11IO0 TM11IO1	-	-

When pins are used as input capture operation, the settings of the registers in the following table are necessary.

Table:9.9.2 Setting Input Pin

	Port output mode register	Port I/O control register
TM8AIO	P3MD(P36M)	P3DIR(P36D)
TM8BIO	P3MD(P37M)	P3DIR(P37D)
TM9AIO	P4MD(P42M)	P4DIR(P42D)
TM9BIO	P4MD(P43M)	P4DIR(P43D)
TM10AIO	P4MD(P46M)	P4DIR(P46D)
TM10BIO	P4MD(P47M)	P4DIR(P47D)
TM11IO0	P7MD(P72M)	P7DIR(P72D)
TM11IO1	P7MD(P73M)	P7DIR(P73D)

■ Count TIming of Input Capture

Table: 9.9.1 shows the timing that the value of the binary counter is read into the compare/capture register at the both edge of the input signal.

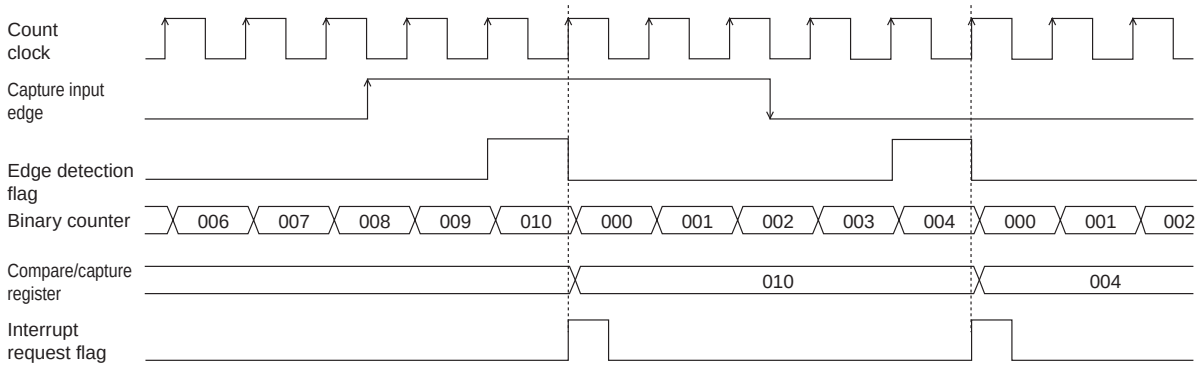


Figure:9.9.1 Count TIming of Input Capture

9.9.2 Setup Example

■ Input Capture Setup Example

The value of the binary counter is read at the rising edge of the external input signal (TM8AIO), and the pulse width can be measured. The oscillation frequency is 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

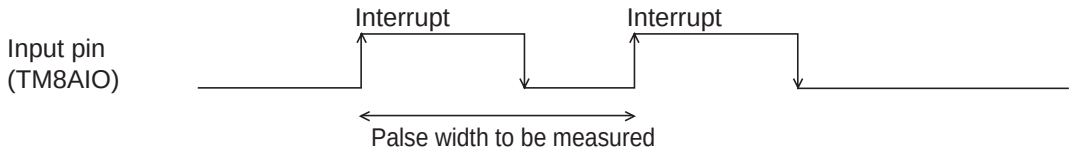


Figure:9.9.2 Input Capture Setup Example One

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register (TM8MD) to stop counting of the timer 8.
(2) Disable the interrupt G7ICR(0x0000891C) bp8: G7IE1=0	(2) Set the G7IE1 flag of the G7ICR register to “0” to disable the interrupt.
(3) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(3) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(4) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(4) Select the timer up counting by the TMUD1-0 flag of the TM8MD register.

Setup Procedure	Description
(5) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(5) Set the TMCLE flag of the TM8MD register to “1” to enable the clear operation of the TM8BC counter. When the value of the TM8BC is captured to the TM8CA register, the TM8BC counter is cleared.
(6) Set the timer capture A operation enabled TM8MDA(0x0000A204) bp4: TMACE=1	(6) Set the TMACE flag of the timer 8 compare/capture A mode register (TM8MDA) to “1” to enable the capture operation.
(7) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=10	(7) Select the capture register (one edge) by the TMAM1-0 flag of the TM8MDA register.
(8) Select the timer A pin polarity TM8MDA(0x0000A204) bp5: TMAEG=0	(8) Set the TMAEG flag of the TM8MDA register to “0” to select the rising edge.
(9) Set the I/O pin (pin function) P3MD(0x0000A033) bp6: P36M=1	(9) Set the P36M flag of the port 3 output mode register (P3MD) to set the port to pin function.
(10) Set the Input pin (I/O function) P3DIR(0x0000A023) bp6: P36D=0	(10) Set the P36D flag of the port 3 I/O control register (P3DIR) to “0” to set I/O control to the input pin.
(11) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(11) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The binary counter (TM8BC) is initialized to 0x0000. Reset the TMLDE flag to “0” after setting.
(12) Set the interrupt level G7ICR(0x0000891C) bp14-12: G7LV2-0=100	(12) Set the interrupt level by the G7LV2-0 flag of the G7ICR register. When the interrupt request flag has been set already, clear the request flag.
(13) Enable the interrupt G7ICR(0x0000891C) bp8: G7IE1=1	(13) Set the G7IE1 flag of the G7ICR register to “1” to enable the interrupt.
(14) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(14) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

When the compare/capture register is read in the interrupt processing after the second timer operation activation, the pulse width can be measured. As the TMCLE flag of the TM8MD register is set to “1”, the binary counter is initialized to 0x0000 at the next count clock after transferring the value of the binary counter to the compare/capture register at the rising edge of the input signal.

The pulse width can be measured by the value of the compare/capture register and the clock source type.

9.10 1-Shot Output

9.10.1 1-Shot Output Operation

1-shot output is to count only one time at a certain period of time.

■ Setting One Shot Output

1-shot operation is set by setting the TM0NE flag of the timer mode register (TMnMD) to “1”. 1-shot operation stops the timer by matching the binary counter and the timer compare/capture A register

■ Count Timing of One Shot Output (TMCLE flag= 0)

The binary counter stops at the next count clock after the value of the binary counter matches the value of the compare/capture register, and the TMXF flag is set to “0”. The setting value of the binary counter is “setting + 1” of the compare/capture register.

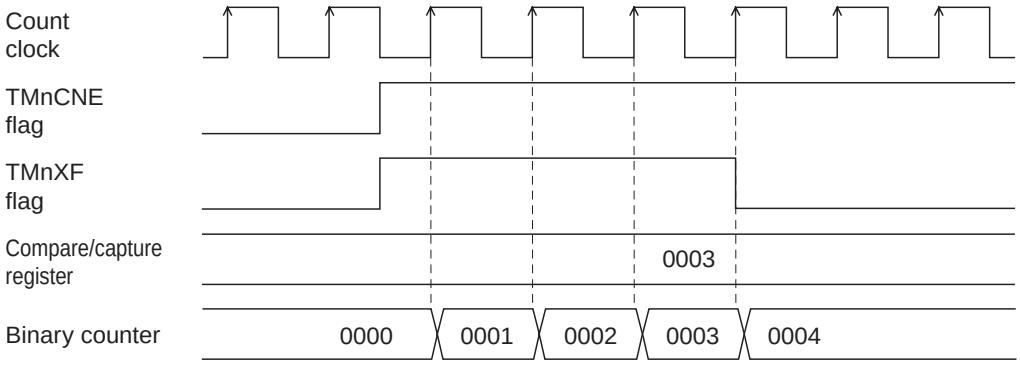


Figure:9.10.1 Count Timing of One Shot Output (TMCLE flag= 0)

■ Count Timing of One Shot Output (TMCLE flag= 1)

The binary counter stops operating at the next count clock after the binary and the compare/capture register match, and the TMXF flag is set to “0”. The binary counter is cleared to 0x0000. Set the TMCNE flag to “1” again after setting “0” to restart.

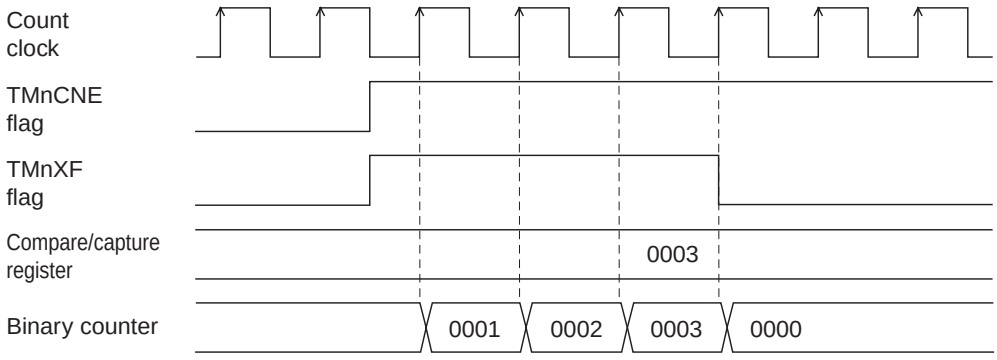


Figure:9.10.2 Count Timing of One Shot Output (TMCLE flag= 1)

9.10.2 Setup Example

■ 1-Shot Output Setup Example

As taking an example of the timer 8, it is explained that timers can operate 1 ms one time. Select IOCLK as clock source to match the binary counter and the compare/capture register after 1ms . The oscillation frequency is 10 MHz, 6 multiplication and IOCLK=MCLK/2. A setup procedure with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop the timer 8 counting.
(2) Set the count cycle TM8CA(0x0000A208)=0x752F	(2) Set the count cycle to the timer 8 compare/capture A register (TM8CA). Due to 30000 counts, the setting value is 29999 (0x752F).
(3) Select the count clock source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(3) Select the TMCK2-0 flag of the TM8MD register to the count clock source (IOCLK).
(4) Select the timer up/down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(4) Select the timer up counting by the TMUD1-0 flag of the TM8MD register.
(5) Set the timer counter clear enabled TM8MD(0x0000A200) bp11: TMCLE=1	(5) Set the TMCLE flag of the TM8MD register to “1” to enable clear operation of the TM8MD counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(6) Set the 1-shot operation enabled TM8MD(0x0000A200) bp12: TMONE=1	(6) Set the TMONE flag of the TM8MD register to “1” to enable1-shot operation.
(7) Select the timer compare/capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1-0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(8) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(8) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register buffer is loaded into the TM8CA register. Reset the TMLDE flag to “0” after setting.
(9) Start the timer operation TM8MD(0x0000A200) bp7: TMCNE=1	(9) Set the TMCNE flag of the TM8MD register to “1” to operate the timer 8.

TM8BC counter counts up. When the TM8BC counter and the TM8CA register match, the timer operation stops at the rising edge of the next count clock. The TMXF flag indicates “0”. The value of the TM8BC counter is initialized to 0x0000 and counting up stops. Set the TMCNE flag to “1” again after setting it to “0” again to restart.

9.11 External Trigger

9.11.1 External Trigger Operation

External trigger is to activate timers by external input pins.

■ Setting External Trigger Operation

Timers can be activated with the external trigger by setting the TMTGE flag of the timer mode register (TMnMD) to “1”. The TMAEG flag of the timer compare/capture A register sets whether timer is activated at the falling edge, or it is activated at rising edge of the input pin. The flag is “0” at the rising edge and “1” at the falling edge.

■ Setting Input Pin

Table:9.11.1 shows the pins which can use the external trigger.

Table:9.11.1 Timer and Input Capture Input PIn

	TImer 8	Timer 9	Time 10	Timer 11	Timer 12	Timer 13
Input pin	TM8AIO	TM9AIO	TM10AIO	TM11IO0	-	-

When pins are used as external trigger, the settings of the following registers are necessary.

Table:9.11.2 Setting Input PIn

	Port output mode register	Port I/O control register
TM8AIO	P3MD(P36M)	P3DIR(P36D)
TM9AIO	P4MD(P42M)	P4DIR(P42D)
TM10AIO	P4MD(P46M)	P4DIR(P46D)
TM11IO0	P7MD(P72M)	P7DIR(P72D)

■ Count Timing of External Trigger (TMCLE flag= 0)

When the TMCLE flag is set to “0” and the binary counter stops at the rising edge of the next count clock of matching the binary counter and the compare/capture register, the binary counter is the setting value of the compare/capture register + 1. When the activation trigger is fed to the pin again, the binary counter restarts to count up.

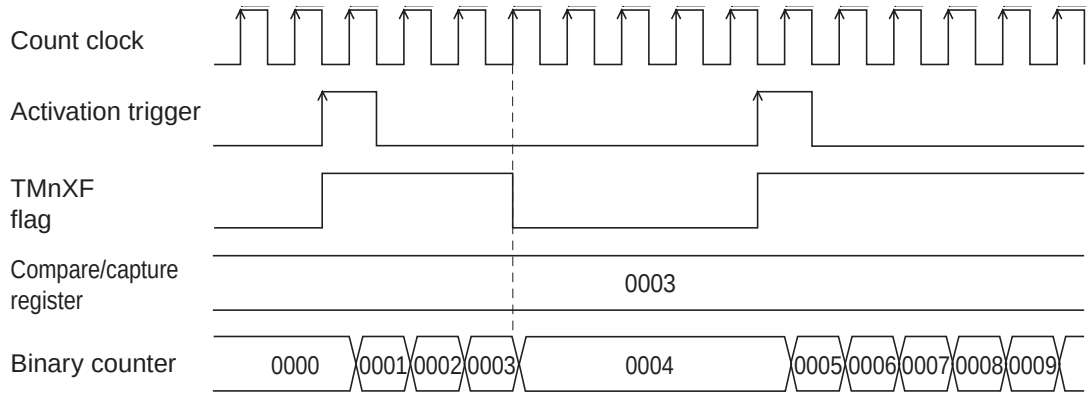


Figure:9.11.1 Count Timing of External Trigger (TMCLE flag= 0)

■ Count Timing of External Trigger (TMCLE flag= 1)

When the TMCLE flag is set to “1” and the binary counter stops at the rising edge of the next count clock of matching the binary counter and the compare/capture register, the binary counter is 0x0000. When the activation trigger is fed to the pin again, the binary counter restarts to count up.

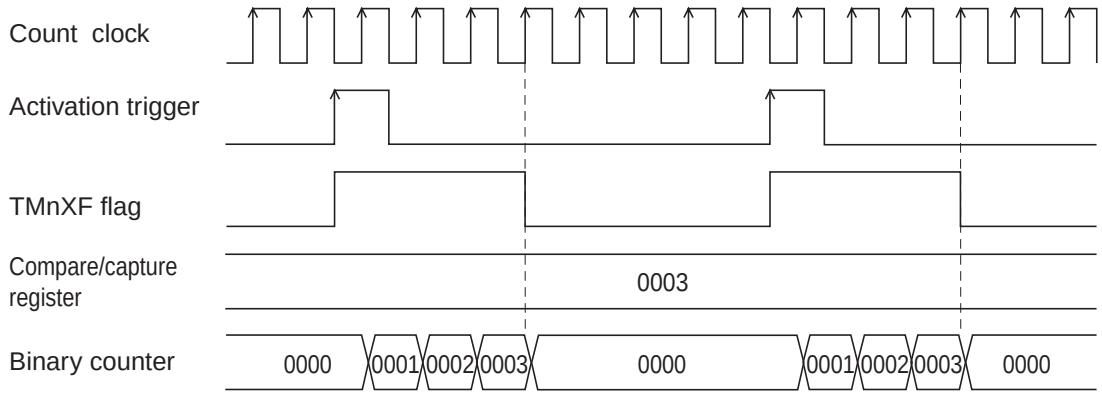


Figure:9.11.2 Count Timing of External Trigger (TMCLE flag= 1)

9.11.2 Setup Example

■ External Trigger Setup Example

Timer 8 can be activated at the rising edge of the external input pin (TM8AIO) . The count clock operates in 1 ms with selecting IOCLK. After 1 ms operation, the count clock stops timer operation and operates for 1 ms again at the rising edge of the external input pin as well.

The count clock generates matching the binary counter and the compare/capture register. The oscillation frequency is 10 MHz, 6 multiplication and IOCLK=MCLK/2. An setup procedure with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM8MD(0x0000A200) bp6: TMLDE=0 bp7: TMCNE=0	(1) Set the TMLDE flag and the TMCNE flag of the timer 8 mode register (TM8MD) to “0” to stop the timer 8 counting.
(2) Set the repeating cycle TM8CA(0x0000A208)=0x752F	(2) Set the repeating cycle to the timer 8 compare/capture A register (TM8CA). The setting value is 29999 (0x752F) due to 30000.
(3) Select the count source TM8MD(0x0000A200) bp2-0: TMCK2-0=000	(3) Select the count clock source (IOCLK) by the TMCK2-0 flag of the TM8MD register.
(4) Select the timer up or down TM8MD(0x0000A200) bp9-8: TMUD1-0=00	(4) Select the timer up counting by the TMUD1-0 flag of the TM8MD register.
(5) Set the timer counter clear enable TM8MD(0x0000A200) bp11: TMCLE=1	(5) Set the TMCLE flag of the TM8MD register to “1” to enable clear operation of the TM8BC counter. When the TM8CA register and the TM8BC counter match, the TM8BC counter is cleared.
(6) Set the timer external trigger enable TM8MD(0x0000A200) bp13: TMTGE=1	(6) Set the TMTGE flag of the TM8MD register to “1” to enable timer activation from the external input pin.
(7) Select the timer compare capture A operation mode TM8MDA(0x0000A204) bp7-6: TMAM1-0=00	(7) Set the function of the timer 8 compare/capture register to the compare register (double buffer) by the TMAM1-0 flag of the timer 8 compare/capture A mode register (TM8MDA).
(8) Select the timer A pin polarity TM8MDA(0x0000A204) bp5: TMAEG=1	(8) Set the TMAEG flag of the TM8MDA register to “1”. The timer is activated at the rising edge of the input pin.
(9) Set the input pin (pin function) P3MD(0x0000A033) bp0: P36M=1	(9) Set the P36M flag of the port 3 output mode register (P3MD) to “1” to set pin function.

Setup Procedure	Description
(10) Set the output pin (I/O function) P3DIR(0x0000A023) bp0: P36D=0	(10) Set the P36D flag of the port 3 I/O control register (P3MD) to “0” to set the I/O control to the input pin.
(11) Initialize the timer 8 TM8MD(0x0000A200) bp6: TMLDE=1	(11) Set the TMLDE flag of the TM8MD register to “1” to initialize the timer 8. The value of the compare register buffer is loaded into the TM8CA register. Reset the TMLDE flag to “0” after setting.

When detecting the rising edge of the external input pin (TM8AIO), the TM8BC counter counts up. When the TM8BC counter matches the TM8CA register, the timer stops at the rising edge of the next count clock. The value of theTM8BC counter is initialized to 0x0000.

When detecting the rising edge of the external input pin (TM8AIO) again, the TM8BC counter restarts to count up.

9.12 A/D Converter Start

9.12.1 Operation

A/D converter can be started using the interrupts of the timer 12 and timer 13.

Table:9.12.1 Interrupt Factors which Can Start A/D Converter

A/D	Factor
AD0	Timer 12 compare/capture A interrupt
	Timer 12 compare/capture B interrupt
	Timer 13 compare/capture A interrupt
	Timer 13 compare/capture B interrupt
AD1	Timer 12 compare/capture A interrupt
	Timer 12 compare/capture B interrupt
	Timer 13 compare/capture A interrupt
	Timer 13 compare/capture B interrupt
AD2	Timer 12 compare/capture A interrupt
	Timer 12 compare/capture B interrupt
	Timer 13 compare/capture A interrupt
	Timer 13 compare/capture B interrupt

Refer to [14-3-1 Operation ■A/D Converter Start] for further details.

9.12.2 Setup Example

A/D conversion results can be obtained by inputting analog voltage through the ADIN00 and ADIN01 pins. Conversion is performed regularly by matching the timer 12 compare A.

Table:9.12.2 Condition Example of Multiple Channel A/D Conversion

Setting item	Setting description
Input pin	ADIN00 pin ADIN01 pin ADIN02 pin
Operation mode	Multiple channel / one time for each
A/D converter start trigger	Timer 12 compare/capture A
A/D converter start cycle	1ms
IOCLK	30MHz

Refer to [14-3-2 Setup Example ■Setup Example of Multiple Channels/One-Time Conversion for Each] for the setting procedure and description.

Chapter 10 Motor Control PWM

10

10.1 Overview

This LSI incorporates 2 complementary 3-phase PWM (PWM0, PWM1) for motor control applications.

10.1.1 Functions

Table:10.1.1 Functions PWM for Motor Control

	PWM0	PWM1	Page
Interrupt cause	PWM0UFIRQ, PWM0CPIRQ	PWM1UFIRQ,PWM1CPIRQ	-
3-phase PWM	U-phase, V-phase, W-phase	U-phase, V-phase, W-phase	-
Waveform mode	Triangular wave, Saw-tooth wave	Triangular wave, Saw-tooth wave	X-19
Dead Time setting	O	O	X-24
H/L level output	O	O	X-25
A/D conversion start	O (AD0, AD1, AD2)	O (AD0, AD1, AD2)	XIV-28
16-bit timer start	O(TM12)	O(TM13)	-
Output timing setting	O	O	X-27

10.1.2 Block Diagram

■ Motor Control PWM Block Diagram

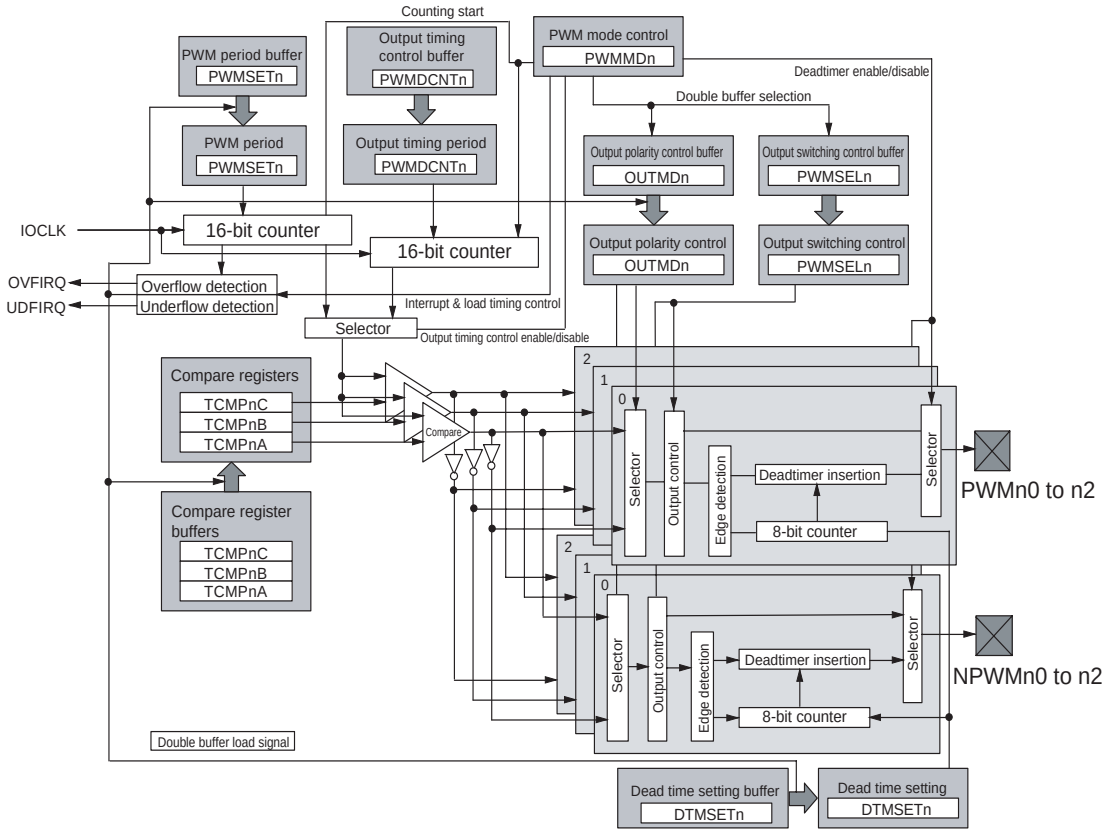


Figure:10.1.1 Motor Control PWM Block Diagram

10.2 Control Registers

10.2.1 Control Registers for Motor Control PWM

Table: 10.2.1 shows registers which control PWM for motor control applications.

Table:10.2.1 Control Registers for Motor Control PWM

	Register	Address	R/W	Access size	Description	Page
PWM0	PWMMD0	0x0000A300	R/W	8,16	PWM0 mode control register	X-5
	OUTMD0	0x0000A304	R/W	8,16	PWM0 output polarity control register	X-7
	PWMSEL0	0x0000A308	R/W	8,16	PWM0 output control register	X-9
	PWMSET0	0x0000A30C	R/W	16	PWM0 period setting register	X-11
	TCMP0A	0x0000A310	R/W	16	PWM00 phase value to be compared setting register	X-12
	TCMP0B	0x0000A314	R/W	16	PWM01 phase value to be compared setting register	X-12
	TCMP0C	0x0000A318	R/W	16	PWM02 phase value to be compared setting register	X-12
	DTMSET0	0x0000A31C	R/W	8,16	PWM0 dead time setting register	X-14
	PWMBC0	0x0000A320	R	16	PWM0BC value read register	X-15
	BCSTR0	0x0000A324	R	8,16	PWM0BC value read register	X-16
	PWMDCNT0	0x0000A328	R/W	8,16	PWM0 output timing control register	X-17
	G16ICR	0x00008940	R/W	8,16	Group 16 interrupt control register	V-24
	P5MD	0x0000A035	R/W	8	Port 5 output mode register	VII-21
	P5DIR	0x0000A025	R/W	8	Port 5 I/O control register	VII-20
PWM1	PWMMD1	0x0000A330	R/W	8,16	PWM1 mode control register	X-6
	OUTMD1	0x0000A334	R/W	8,16	PWM1 output polarity control register	X-7
	PWMSEL1	0x0000A338	R/W	8,16	PWM1 output control register	X-9
	PWMSET1	0x0000A33C	R/W	16	PWM1 period setting register	X-11
	TCMP1A	0x0000A340	R/W	16	PWM11 phase value to be compared setting register	X-12
	TCMP1B	0x0000A344	R/W	16	PWM11 phase value to be compared setting register	X-12
	TCMP1C	0x0000A348	R/W	16	PWM12 phase value to be compared setting register	X-12
	DTMSET1	0x0000A34C	R/W	8,16	PWM1 dead time setting register	X-14
	PWMBC1	0x0000A350	R	16	PWM1BC value read register	X-16
	BCSTR1	0x0000A354	R	8,16	PWM1BC value read register	X-17
	PWMDCNT1	0x0000A358	R/W	8,16	PWM1 output timing control register	X-17
	G17ICR	0x00008944	R/W	8,16	Group 17 interrupt control register	V-25
	P6MD	0x0000A036	R/W	8	Port 6 output mode register	VII-23
	P6DIR	0x0000A026	R/W	8	Port 6 I/O control register	VII-22
PWM0, 1	PWMOFF	0x0000A360	R/W	8,16	PWM pin protection control register	X-18

R/W Readable / Writable
R Readable only
W Writable only

10.2.2 PWM Mode Control Registers

PWM mode control registers are used to set various modes for the motor control block.

■ PWM0 Mode Control Register (PWMMD0: 0x0000A300) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	SYNEN0	SFTEN0	CLKSEL0	TMSTAEN0	TMSTBEN0	SDSELA0	SDSELB0	PCRAEN0	PCRBEN0	INTAEN0	INTBEN0	DTEN0	ORMD0	TCEN0	WAVEMD0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	-	-	-
14	SYNEN0	Simultaneous starting function of PWM0 and PWM1 enable	0: Disabled 1: Enabled
13	SFTEN0	Output timing varying function enable	0: Disabled 1: Enabled
12	CLKSEL0	Count clock switch	0: IOCLK 1: Setting prohibited
11	TMSTAEN0	TM12 external trigger activation enable (PWM binary counter underflow)	0: Disabled 1: Enabled
10	TMSTBEN0	TM12 external trigger activation enable (PWM binary counter overflow)	0: Disabled 1: Enabled
9	SDSELA0	OUTMD0 buffer mode	0: Single-buffer mode 1: Double-buffer mode
8	SDSELB0	PWMSEL0 buffer mode.	0: Single-buffer mode 1: Double-buffer mode
7	PCRAEN0	Double buffer load timing enable (PWM binary counter underflow)	0: Disabled 1: Enabled
6	PCRBEN0	Double buffer load timing enable (PWM binary counter overflow)	0: Disabled 1: Enabled
5	INTAEN0	Timer interrupt timing enable (PWM binary counter underflow).	0: Disabled 1: Enabled
4	INTBEN0	Timer interrupt timing enable (PWM binary counter overflow).	0: Disabled 1: Enabled
3	DTEN0	Dead Time insertion	0: No dead time 1: Dead Time
2	ORMD0	Dead Time insertion logic	0: Positive logic (H active) 1: Negative logic (L active)
1	TCEN0	PWM counting operation enable	0: Disabled 1: Enabled
0	WAVEMD0	PWM waveform mode	0: Triangular wave 1: Saw-tooth wave

■ PWM1 Mode Control Register (PWMMD1: 0x0000A330) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	SYNEN1	SFTEN1	CLKSEL1	TMSTAEN1	TMSTBEN1	SDSELA1	SDSELB1	PCRAEN1	PCRBEN1	INTAEN1	INTBEN1	DTEN1	ORMD1	TCEN1	WAVEMD1
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	-	-	-
14	SYNEN1	Simultaneous starting function of PWM0 and PWM1 enable	0: Disabled 1: Enabled
13	SFTEN1	Output timing varying function enable	0: Disabled 1: Enabled
12	CLKSEL1	Count clock switch	0: IOCLK 1: Setting prohibited
11	TMSTAEN1	TM13 external trigger activation enable (PWM binary counter underflow)	0: Disabled 1: Enabled
10	TMSTBEN1	TM13 external trigger activation enable (PWM binary counter overflow)	0: Disabled 1: Enabled
9	SDSELA1	OUTMD1 buffer mode	0: Single-buffer mode 1: Double-buffer mode
8	SDSELB1	PWMSEL1 buffer mode.	0: Single-buffer mode 1: Double-buffer mode
7	PCRAEN1	Double buffer load timing enable (PWM binary counter underflow)	0: Disabled 1: Enabled
6	PCRBEN1	Double buffer load timing enable (PWM binary counter overflow)	0: Disabled 1: Enabled
5	INTAEN1	Timer interrupt timing enable (PWM binary counter underflow).	0: Disabled 1: Enabled
4	INTBEN1	Timer interrupt timing enable (PWM binary counter overflow).	0: Disabled 1: Enabled
3	DTEN1	Dead Time insertion	0: No dead time 1: Dead Time
2	ORMD1	Dead Time insertion logic	0: Positive logic (H active) 1: Negative logic (L active)
1	TCEN1	PWM counting operation enable	0: Disabled 1: Enabled
0	WAVEMD1	PWM waveform mode	0: Triangular wave 1: Saw-tooth wave

10.2.3 PWM Output Polarity Control Registers

PWM output polarity control register selects polarity for each of the PWM outputs.

This register can select double-buffer or single-buffer mode by the SDSELAn flag of the PWM mode control register (PWMMDn). When double-buffer mode is selected, the value of OUTMDn is loaded into the register at the timing selected with PWMMDn register. When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing; thus, ensuring smooth use of double buffer from the initial state where the PWM counter starts.

■ PWM0 Output Polarity Control Register (OUTMD0: 0x0000A304) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	PXDTNW0	PXDTW0	PXDTNV0	PXDTV0	PXDTNU0	PXDTU0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-6	-	-	-
5	PXDTNW0	Output polarity for NPWM02	0: Positive phase 1: Negative phase
4	PXDTW0	Output polarity for PWM02	0: Positive phase 1: Negative phase
3	PXDTNV0	Output polarity for NPWM01	0: Positive phase 1: Negative phase
2	PXDTV0	Output polarity for PWM01	0: Positive phase 1: Negative phase
1	PXDTNU0	Output polarity for NPWM00	0: Positive phase 1: Negative phase
0	PXDTU0	Output polarity for PWM0	0: Positive phase 1: Negative phase

■ PWM1 Output Polarity Control Register (OUTMD1: 0x0000A334) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	PXDTNW1	PXDTW1	PXDTNV1	PXDTV1	PXDTNU1	PXDTU1
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-6	-	-	-
5	PXDTNW1	Output polarity for NPWM12	0: Positive phase 1: Negative phase
4	PXDTW1	Output polarity for PWM12	0: Positive phase 1: Negative phase
3	PXDTNV1	Output polarity for NPWM11	0: Positive phase 1: Negative phase
2	PXDTV1	Output polarity for PWM11	0: Positive phase 1: Negative phase
1	PXDTNU1	Output polarity for NPWM10	0: Positive phase 1: Negative phase
0	PXDTU1	Output polarity for PWM10	0: Positive phase 1: Negative phase

10.2.4 PWM Output Control Registers

PWM output control register is used to switch between 2 output sources, PWM output or H/L level output.

This register can select double-buffer or single-buffer mode by the SDSELBn flag of the PWM mode control register (PWMMDn). When double-buffer mode is selected, the value of PWMSELn is loaded into the register at the timing selected with PWMMDn register. When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing.

■ PWM0 Output Control Register (PWMSEL0: 0x0000A308) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	PSELN02	PSEL02	PSELN01	PSEL01	PSELN00	PSEL00	OTLVN02	OTLV02	OTLVN01	OTLV01	OTLVN00	OTLV00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-12	-	-	-
11	PSELN02	NPWM02 output sources	0: PWM output 1: H/L level output
10	PSEL02	PWM02 output sources	0: PWM output 1: H/L level output
9	PSELN01	NPWM01 output sources	0: PWM output 1: H/L level output
8	PSEL01	PWM01 output sources	0: PWM output 1: H/L level output
7	PSELN00	NPWM00 output sources	0: PWM output 1: H/L level output
6	PSEL00	PWM00 output sources	0: PWM output 1: H/L level output
5	OTLVN02	NPWM02 H/L level output	0: L level output 1: H level output
4	OTLV02	PWM02 H/L level output	0: L level output 1: H level output
3	OTLVN01	NPWM01 H/L level output	0: L level output 1: H level output
2	OTLV01	PWM01 H/L level output	0: L level output 1: H level output
1	OTLVN00	NPWM00 H/L level output	0: L level output 1: H level output
0	OTLV00	PWM00 H/L level output	0: L level output 1: H level output

■ PWM1 Output Control Register (PWMSEL1: 0x0000A338) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	PSELN12	PSEL12	PSELN11	PSEL11	PSELN10	PSEL10	OTLVN12	OTLV12	OTLVN11	OTLV11	OTLVN10	OTLV10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-12	-	-	-
11	PSELN12	NPWM12 output sources	0: PWM output 1: H/L level output
10	PSEL12	PWM12 output sources	0: PWM output 1: H/L level output
9	PSELN11	NPWM11 output sources	0: PWM output 1: H/L level output
8	PSEL11	PWM11 output sources	0: PWM output 1: H/L level output
7	PSELN10	NPWM10 output sources	0: PWM output 1: H/L level output
6	PSEL10	PWM10 output sources	0: PWM output 1: H/L level output
5	OTLVN12	NPWM12 H/L level output	0: L level output 1: H level output
4	OTLV12	PWM12 H/L level output	0: L level output 1: H level output
3	OTLVN11	NPWM11 H/L level output	0: L level output 1: H level output
2	OTLV11	PWM11 H/L level output	0: L level output 1: H level output
1	OTLVN10	NPWM10 H/L level output	0: L level output 1: H level output
0	OTLV10	PWM10 H/L level output	0: L level output 1: H level output

10.2.5 PWM Period Setting Registers

PWM period setting register is used to determine the period for 3-phase of PWM0 and PWM1.

This register needs to be set only when double-buffer mode is selected. The value of PWMSETn is loaded into the register at the timing selected with the PWM mode control register (PWMMDn). When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing.

■ PWM0 Period Setting Register (PWMSET0: 0x0000A30C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	PMSET0F	PMSET0E	PMSET0D	PMSET0C	PMSET0B	PMSET0A	PMSET09	PMSET08	PMSET07	PMSET06	PMSET05	PMSET04	PMSET03	PMSET02	PMSET01	PMSET00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	PMSET0F to PMSET00	Setting PWM0 period.	Set the PWM0 16-bit counter period.

■ PWM1 Period Setting Register (PWMSET1: 0x0000A33C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	PMSET1F	PMSET1E	PMSET1D	PMSET1C	PMSET1B	PMSET1A	PMSET19	PMSET18	PMSET17	PMSET16	PMSET15	PMSET14	PMSET13	PMSET12	PMSET11	PMSET10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	PMSET1F to PMSET10	Setting the PWM1 period.	Set the PWM1 16-bit counter period.

10.2.6 PWM Phase Value to be Compared Setting Registers

PWM phase value to be compared setting register is used to determine the timing at which 3-phase output of PWM0 and PWM1 is to change. This register needs to be set only when double-buffer mode is selected. The value of TCMPn is loaded into the register at the timing selected with the PWM mode control register (PWM-MDn). When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing.

■ PWM00 Phase Value to be Compared Setting Register (TCMP0A: 0x0000A310) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP A0F	TCP A0E	TCP A0D	TCP A0C	TCP A0B	TCP A0A	TCP A09	TCP A08	TCP A07	TCP A06	TCP A05	TCP A04	TCP A03	TCP A02	TCP A01	TCP A00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPA0F to TCPA00	Timing at which PWM00 phase output is to change setting	Setting a value of PWM00 phase to be compared with the PWM0 binary counter

■ PWM01 Phase Value to be Compared Setting Register (TCMP0B: 0x0000A314) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP B0F	TCP B0E	TCP B0D	TCP B0C	TCP B0B	TCP B0A	TCP B09	TCP B08	TCP B07	TCP B06	TCP B05	TCP B04	TCP B03	TCP B02	TCP B01	TCP B00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPB0F to TCPB00	Timing at which PWM01 phase output is to change setting	Setting a value of PWM01 phase to be compared with the PWM0 binary counter

■ PWM02 Phase Value to be Compared Setting Register (TCMP0C: 0x0000A318) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP C0F	TCP C0E	TCP C0D	TCP C0C	TCP C0B	TCP C0A	TCP C09	TCP C08	TCP C07	TCP C06	TCP C05	TCP C04	TCP C03	TCP C02	TCP C01	TCP C00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPC0F to TCPC00	Timing at which PWM02 phase output is to change setting	Setting a value of PWM02 phase to be compared with the PWM0 binary counter

■ PWM10 Phase Value to be Compared Setting Register (TCMP1A: 0x0000A340) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP A1F	TCP A1E	TCP A1D	TCP A1C	TCP A1B	TCP A1A	TCP A19	TCP A18	TCP A17	TCP A16	TCP A15	TCP A14	TCP A13	TCP A12	TCP A11	TCP A10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPA1F to TCPA10	Timing at which PWM10 phase output is to change setting	Setting a value of PWM10 phase to be compared with the PWM1 binary counter

■ PWM11 Phase Value to be Compared Setting Register (TCMP1B: 0x0000A344) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP B1F	TCP B1E	TCP B1D	TCP B1C	TCP B1B	TCP B1A	TCP B19	TCP B18	TCP B17	TCP B16	TCP B15	TCP B14	TCP B13	TCP B12	TCP B11	TCP B10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPB1F to TCPB10	Timing at which PWM11 phase output is to change setting	Setting a value of PWM11 phase to be compared with the PWM1 binary counter

■ PWM12 Phase Value to be Compared Setting Register (TCMP1C: 0x0000A348) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	TCP C1F	TCP C1E	TCP C1D	TCP C1C	TCP C1B	TCP C1A	TCP C19	TCP C18	TCP C17	TCP C16	TCP C15	TCP C14	TCP C13	TCP C12	TCP C11	TCP C10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-0	TCPC1F to TCPC10	Timing at which PWM12 phase output is to change setting	Setting a value of PWM12 phase to be compared with the PWM1 binary counter

10.2.7 Dead Time Setting Registers

Dead Time setting register is used to set dead time of PWM0 and PWM1. Dead Time is designed to insert on time delay into each of the upper and lower phases when the signal is inverted at PWM output. The dead time counter functions in synchronization with clock set by the PWM mode control register ‘PWMMDn) and counts 1 every 2 clock cycles. The dead time or delay time is calculated with “setting × 2 + 1”. Thus, when “00” is set, 1 clock cycle of dead time is inserted if dead time is enabled. This register needs to be set only when double-buffer mode is selected. The value of DTMSETn is loaded into the register at the timing selected with the PWM mode control register (PWMMDn). When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing.

■ PWM0 Dead Time Setting Register (DTMSET0: 0x0000A31C) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	DTST07	DTST06	DTST05	DTST04	DTST03	DTST02	DTST01	DTST00
At reset	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-8	-	-	-
7-0	DTST07 to DTST00	Setting PWM0 dead time	Setting dead time value to 8-bit dead timer counter

■ PWM1 Dead Time Setting Register (DTMSET1: 0x0000A34C) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	DTST17	DTST16	DTST15	DTST14	DTST13	DTST12	DTST11	DTST10
At reset	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-8	-	-	-
7-0	DTST17 to DTST10	Setting PWM1 dead time	Setting dead time value to 8-bit dead timer counter

10.2.8 Output Timing Control Registers

Output timing control register is used to control the timing of PWM pin output. Output timing variable function is a function for pin output at any timing in 1 cycle of PWM. This register needs to be set only when double-buffer mode is selected. The value of PWMDCNTn is loaded into the register at the timing selected with the PWM mode control register (PWMMDn). When the PWM counter is not running, the double-buffer value is loaded into the register as is regardless of the specified read timing.

This register needs to be set only when single-buffer mode is selected.

■ PWM0 Output Timing Control Register (PWMDCNT0: 0x0000A328) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	SDIR0	STIM07	STIM06	STIM05	STIM04	STIM03	STIM02	STIM01	STIM00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-9	-	-	-
8	SDIR0	Shift direction of PWM0 output waveform setting	0: Shift ahead 1: Shift back
7-0	STIM07 to STIM00	Shift time of PWM0 output waveform setting	Setting the time when PWM0 output waveform is shifted by the value of PWM count

■ PWM1 Output Timing Control Register (PWMDCNT1: 0x0000A358) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	SDIR1	STIM17	STIM16	STIM15	STIM14	STIM13	STIM12	STIM11	STIM10
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-9	-	-	-
8	SDIR1	Shift direction of PWM1 output waveform setting	0: Shift ahead 1: Shift back
7-0	STIM17 to STIM10	Shift time of PWM1 output waveform setting	Setting the time when PWM1 output waveform is shifted by the value of PWM count

10.2.9 BC Value Read Registers

BC value read register is used to read the binary counter value of PWM0 and PWM1.

■ PWM0 BC Value Read Register (PWMBC0: 0x0000A320) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	PWM0BC15	PWM0BC14	PWM0BC13	PWM0BC12	PWM0BC11	PWM0BC10	PWM0BC09	PWM0BC08	PWM0BC07	PWM0BC06	PWM0BC05	PWM0BC04	PWM0BC03	PWM0BC02	PWM0BC01	PWM0BC00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-0	PWM0BC15 to PWM0BC00	Reading the PWM0 binary counter value	Reading the PWM0 binary counter value

■ PWM1 BC Value Read Register (PWMBC1: 0x0000A350) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	PWM1BC15	PWM1BC14	PWM1BC13	PWM1BC12	PWM1BC11	PWM1BC10	PWM1BC09	PWM1BC08	PWM1BC07	PWM1BC06	PWM1BC05	PWM1BC04	PWM1BC03	PWM1BC02	PWM1BC01	PWM1BC00
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-0	PWM1BC15 to PWM1BC00	Reading the PWM1 binary counter value	Reading the PWM1 binary counter value

10.2.10 BC Status Read Registers

BC status read register is used to read the binary counter's counting status of PWM0 and PWM1.

■ PWM0 BC Status Read Register (BCSTR0: 0x0000A324) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PWM0STR
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-1	-	-	-
0	PWM0STR	Reading the PWM0 binary counter's counting status	0: Counting down 1: Counting up

■ PWM1 BC Status Read Register (BCSTR1: 0x0000A354) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PWM1STR
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-1	-	-	-
0	PWM1STR	Reading the PWM1 binary counter's counting status	0: Counting down 1: Counting up

10.2.11 PWM Pin Protection Control Registers

This register is used to automatically bring the PWM output pins into high impedance state by the specified interrupt generation. The output pins can return from high impedance state by clearing the interrupt request flag (IR).

This register needs to be set only when single-buffer mode is selected.

■ PWM Pin Protection Control Register (PWMOFF: 0x0000A360) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	IRQSEL12	IRQSEL11	IRQSEL10	IRQSEL02	IRQSEL01	IRQSEL00	-	CLRHZ1	CLRHZ0	-	USEHZ1	USEHZ0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	-	-	-
14-12	-	Reserved	Set to “000”.
11-9	IRQSEL12 IRQSEL11 IRQSEL10	PWM1 protection interrupt selection (which interrupt the pin is to be protected)	000: IRQ0 001: IRQ1 010: IRQ2 011: IRQ3 100: IRQ4 101: IRQ5 11X: Setting prohibited
8-6	IRQSEL02 IRQSEL01 IRQSEL00	PWM0 protection interrupt selection (which interrupt the pin is to be protected)	000: IRQ0 001: IRQ1 010: IRQ2 011: IRQ3 100: IRQ4 101: IRQ5 11X: Setting prohibited
5	-	Reserved	Set to “0”.
4	CLRHZ1	PWM1 output protection function	0: Disabled 1: Enabled
3	CLRHZ0	PWM0 output protection function	0: Disabled 1: Enabled
2	-	Reserved	Set to “0”.
1	USEHZ1	PWM1 output setting	0: PWM output in high impedance state 1: PWM output
0	USEHZ0	PWM0 output setting	0: PWM output in high impedance state 1: PWM output

The TM11 output protection can be put into the high impedance state by setting the port 7 I/O control register (P7DIR) to input mode.

10.3 Operation

10.3.1 Motor Control PWM Operation

■ Waveform Mode

Waveform mode can be set by the WAVEMDn flag of the PWM mode control register (PWMMDn). When “0” is set, triangular waves are specified and “1” is set, saw-tooth waves are specified.

Table: 10.3.1 shows the output waveform logic operation formula and output level.

Table:10.3.1 Logic Operation Formula and Output Level

Logic operation formula	PWMn0 to 2	NPWMn0 to 2
Value to be compared≤Counter value	H	L
Value to be compared>Counter value	L	H

When triangular waves are set, the counter counts up and down. It counts the period setting and “0” twice each at the end of counting up and down. When saw-tooth waves are set, the counter counts up. After the counter counts up until the period setting value, it becomes “0” at the next counting . Triangular and saw-tooth wave output figures are shown below.

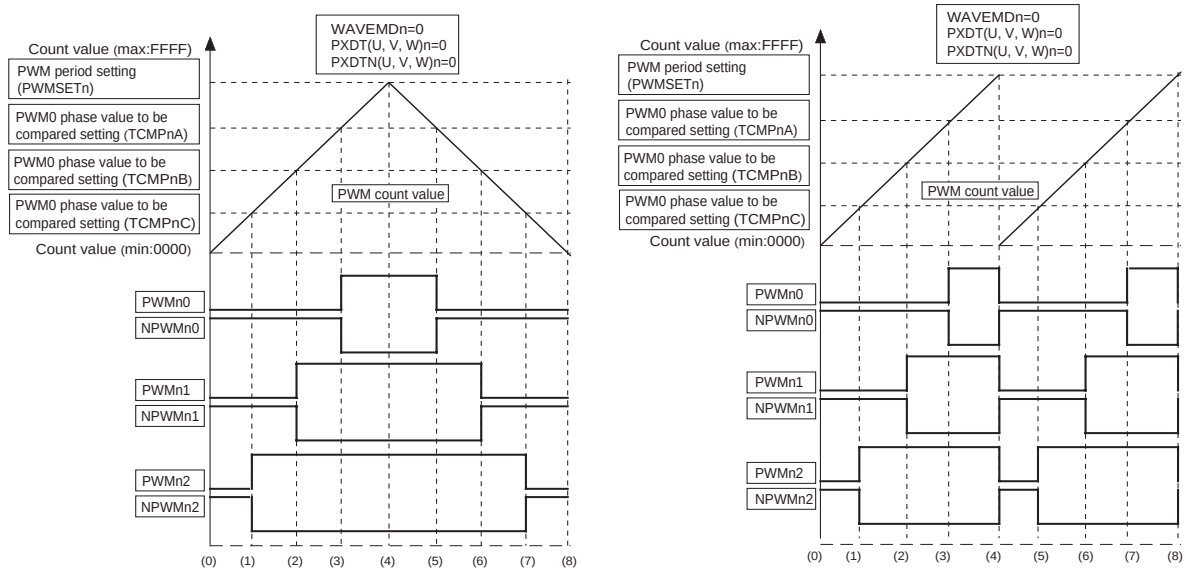


Figure:10.3.1 Triangular and Saw-tooth Waves

■ Setting PWM Period

The 3-phase period for PWMn is set by the PWM period setting register (PWMSETn). PWM counting is operated by the PWMn binary counter (PWMBCn). The formula of the PWM period is as follows. The count clock of the PWMBCn counter is IOCLK.

Waveform mode	PWM period
Triangular wave	Count clock period × (PWMSETn set value +1) × 2
Saw-tooth wave	Count clock period × (PWMSETn set value +1)

■ Starting and Stopping PWM Output

When the TCENn flag of the PWMMD0 register is set to “1”, PWM output starts and when set to “0”, it stops. Table: 10.3.2 shows the PWM block status stopped.

Table:10.3.2 PWM Block Status When Counting Operation is Disabled

PWM block			Status
Phase output	When positive polarity is selected as output polarity	PWMn0 to 2	L
		NPWMn0 to 2	H
	When negative polarity is selected as output polarity	PWMn0 to 2	H
		NPWMn0 to 2	L
PWM binary counter (16-bit counter)			Undefined
Dead Time counter			Reset status
PWM control register (double-buffer)			Double-buffer data loaded
PWM control register (single-buffer)			Retained

■ Output Waveform Polarity

The PWM output polarity control register (OUTMDn) can be used to control polarity of PWM output waveform.

Table:10.3.3 shows the flags and set values. When the PXDTn0 flag is set to “1”, PWMn0 and NPWMn0 outputs are switched.

Table:10.3.3 Flags and Settings

	Flag	Setting value	
		"0"	"1"
PWMn0	PXDTUn	Positive phase	Negative phase
NPWMn0	PXDTNUn	Negative phase	Positive phase
PWMn1	PXDTVn	Positive phase	Negative phase
NPWMn1	PXDTNVn	Negative phase	Positive phase
PWMn2	PXDTWn	Positive phase	Negative phase
NPWMn2	PXDTNWn	Negative phase	Positive phase

Figure:10.3.2 shows the flag value and the output waveform.

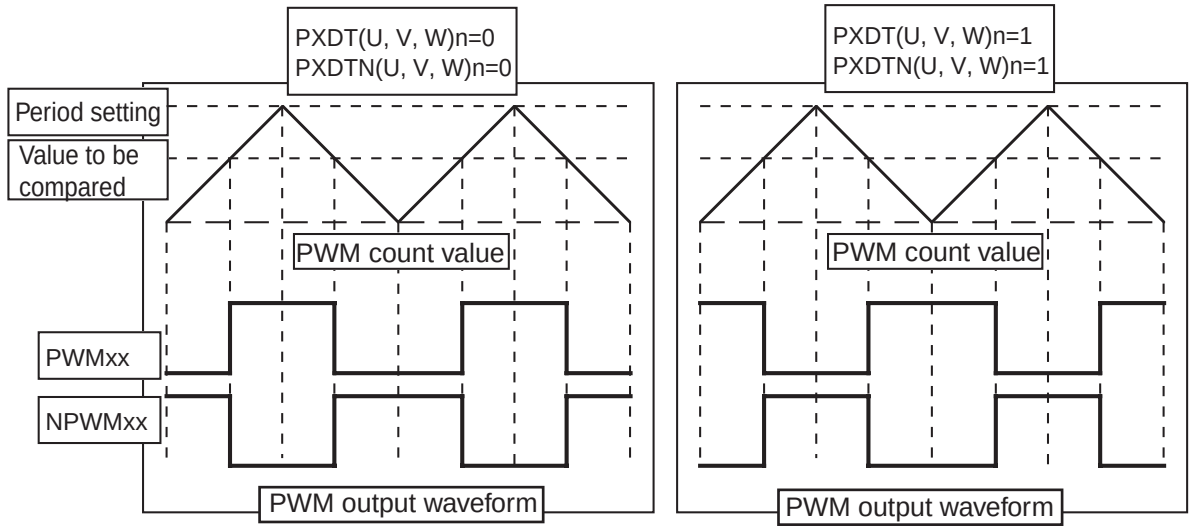


Figure:10.3.2 Flag Value and Output Waveform

■ Double Buffer

Each of the PWM registers is double-buffered to allow data changes during PWM operation. Registers read from and written to by the microcontroller are independent of registers referenced by the PWM. This makes it possible for microcontroller's register values to be loaded into PWM's registers in synchronization with PWM period. The PWM mode register (PWMMDn) is single-buffered as it is a basic register that controls PWM operation mode. However, double buffer and single buffer are selectable with all other PWM control registers. Therefore, the configuration that best suits the application can be selected. Check the PWM control register list for buffer configuration. Double buffer load timing can be set by overflow and underflow of PWM period.The PWMMDn register can be used to enable or disable either of these timings. Data in all double buffers for control registers is loaded into a PWM at the same timing. However, this timing can be specified separately for each PWM. If the PWMn binary counter is stopped with counting operation disabled, the double buffer values are directly loaded into PWM registers.

Table:10.3.4 Buffer Configuration Available with PWM Control Registers

Register	Double-buffered	Single-buffered	Remarks
PWMMDn	-	O	
OUTMDn	O	O	Switching by the SDSLAn flag in the PWMMDn register
PWMSELn	O	O	Switching by the SDSLBn flag in the PWMMDn register
PWMSETn	O	-	
TCMPnA	O	-	
TCMPnB	O	-	
TCMPnC	O	-	
DTMSETn	O	-	
PWMDCNTn	O	-	
PWMOFF	-	O	

■ Double Buffer Load Timing

Double buffer load can be enabled by the PCRAEN flag and PCRBEN flag of the PWMMDn register. Table: 10.3.5 shows the relationship between the double buffer load timing and enable setting flag.

Table:10.3.5 Double Buffer Load Timing and Enable Setting Flag

Load timing	Flag (Register)		
At PWM binary counter underflow	PCRAEN(PWMMDn)	0	Disabled
		1	Enabled
At PWM binary counter overflow	PCRBEN(PWMMDn)	0	Disabled
		1	Enabled

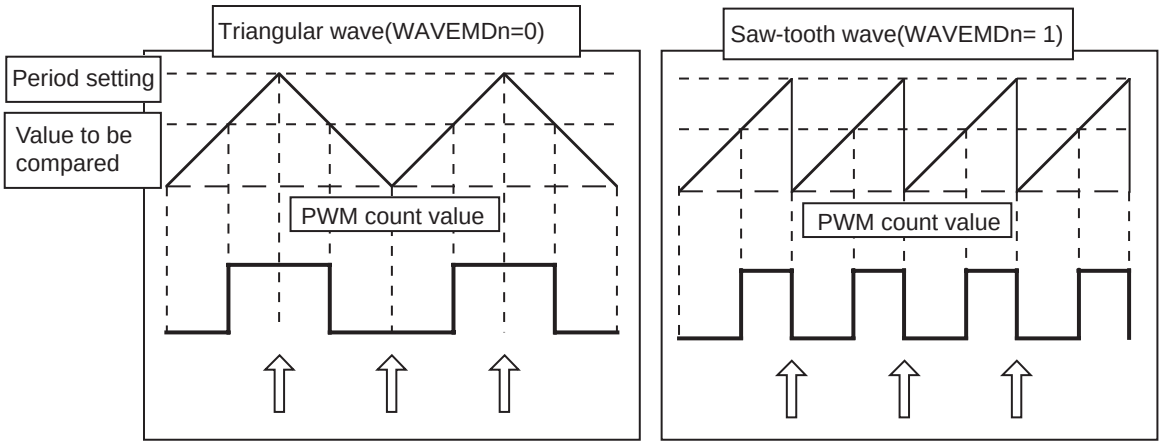


Figure:10.3.3 Double Buffer Load TIming

■ Setting Interrupt Timing

Interrupt signal can be generated in synchronization with the PWM period. Interrupt signal generation timing is at the PWM period underflow and overflow. Table: 10.3.6 shows the relationship between the interrupt timing and the enable setting flag.

Table:10.3.6 Interrupt Timing and Enable Setting Flag

Load timing	Flag (Register)		
At PWM binary counter underflow	INTAEN (PWMMDn)	0	Disabled
		1	Enabled
At PWM binary counter overflow	INTBEN (PWMMDn)	0	Disabled
		1	Enabled

■ Dead Time

Dead Time is designed to insert on time delay into each of the upper and lower phases when the signal is inverted at each PWM output phase. The DTEN flag of the PWMMDn register is used to select whether to enable or disable dead time. The ORMDn flag of the PWMMDn register is used to select output logic at the time of dead time insertion. The dead time setting register (DTMSETn) is used to specify delay time inserted as dead time. Any of "00" to "FF" can be selected as dead time with 8-bit data. The dead time counter functions in synchronization with MCLK when the CLKSELn flag of the PWMMDn register is "1" and with IOCLK when it is "0", and counts by 1 every 2 clock cycles. Calculate the dead time or delay time based on "set value × 2+1". Thus, when "00" is specified, 1 clock cycle of dead time is inserted if dead time is enabled.

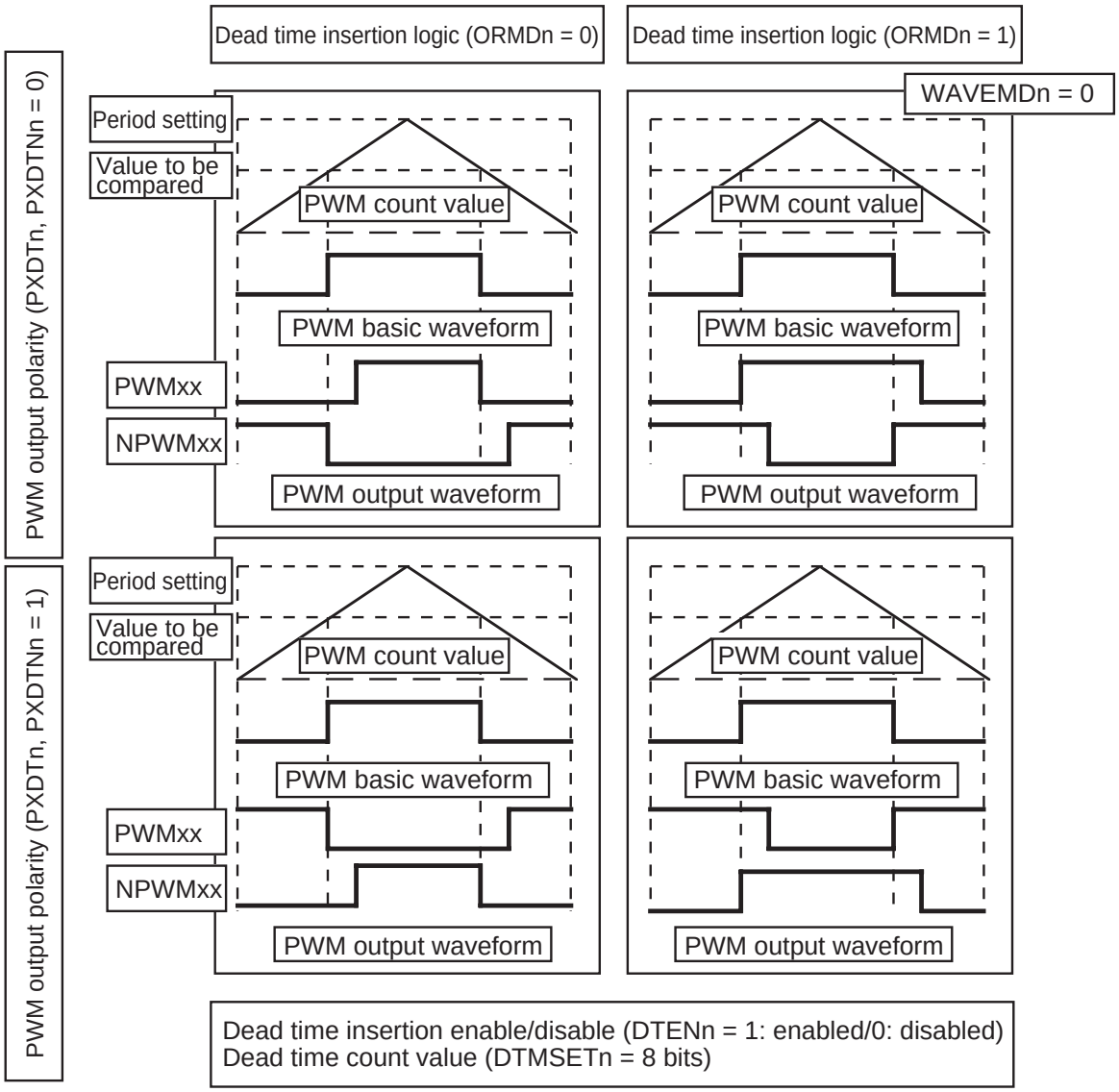


Figure:10.3.4 Dead Time

■ Setting H/L Level Output

PWM output or H/L level output can be selected for each of the 6 PWM pins by the PSELNn2-0 flags and the PSELn2-0 flags of the PWM output control register (PWMSELn). L level output or H level output can be selected by the OUTVNn2-0 and OUTVn2- 0 when setting H/L level output. The following shows the output timing of H/L level output.

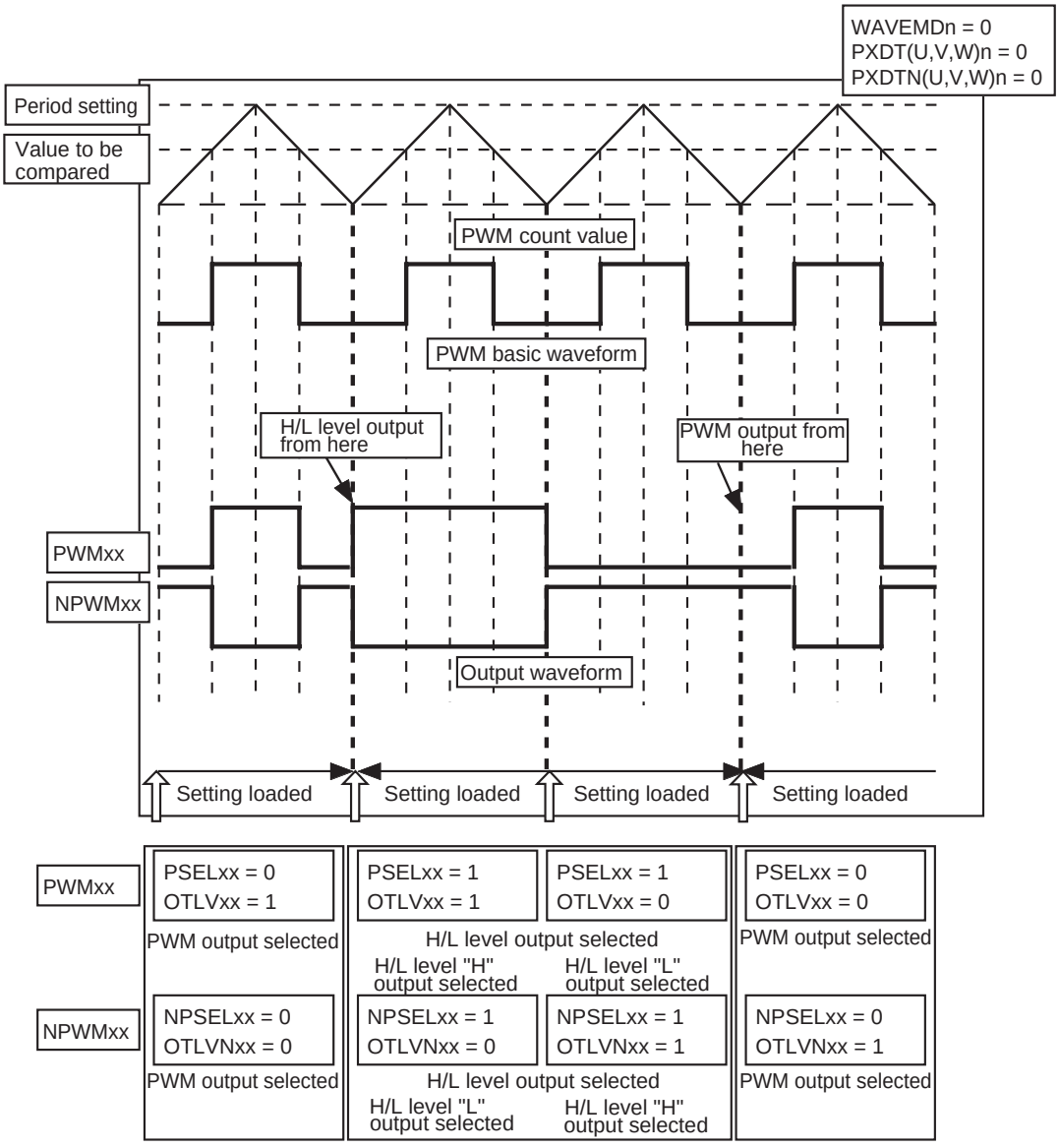


Figure:10.3.5 H/L Level Output Timing

■ Inserting Dead Time at H/L Level Output

Dead Time is inserted as delay time when signals are switched. Therefore, dead time is inserted even when PWM output is switched over to H/L level output. The timing of dead time insertion is shown below.

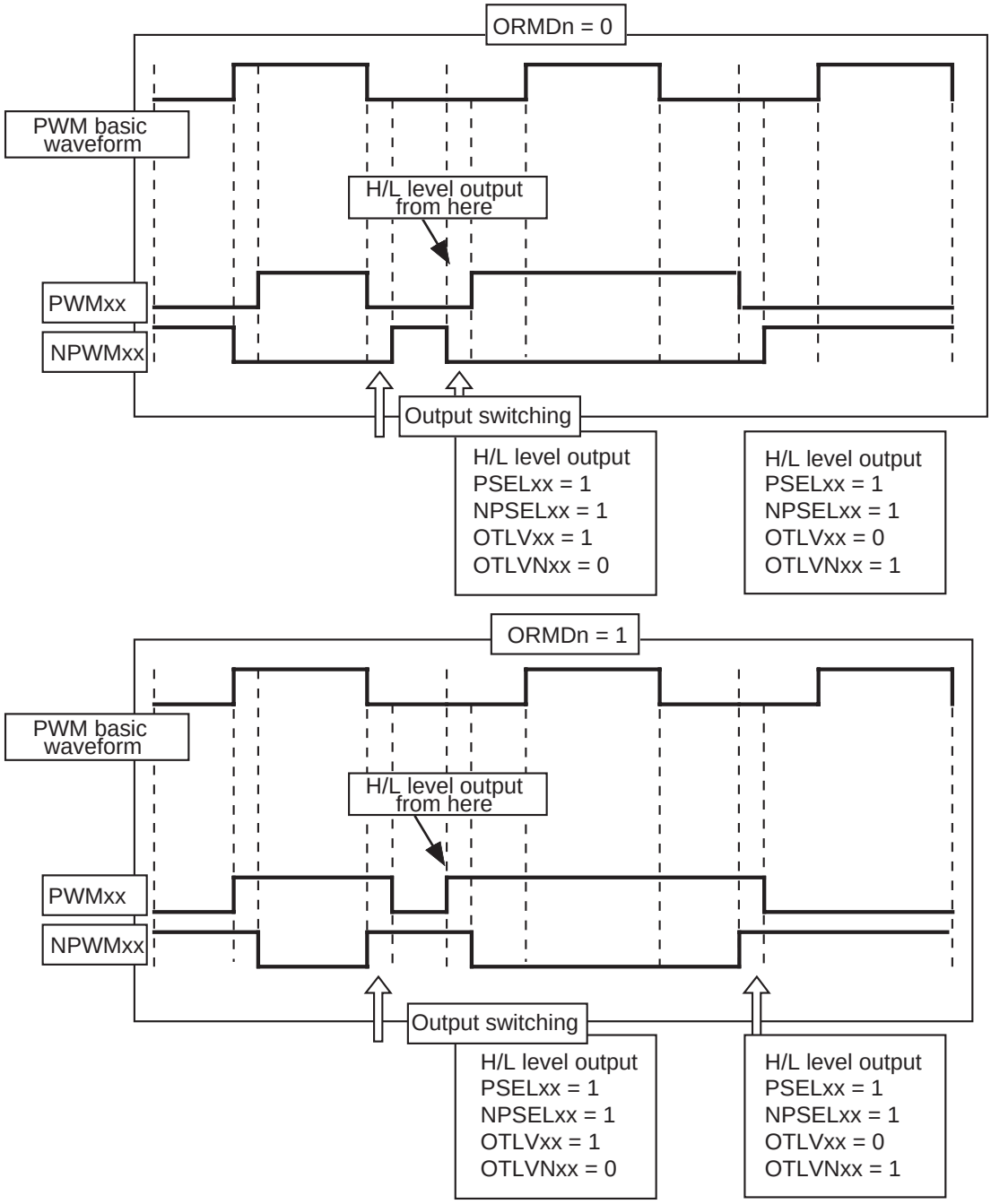


Figure:10.3.6 Dead Time Insertion Timing at H/L Level Output

■ Setting PWM Output Timing

PWM output timing can be shifted by the PWM output timing control register (PWMDCNT) within PWM period. Set the SETENn flag of the PWMMDn register to “1” to valid shift function of PWM output timing.

The relationship between the register value and PWM output timing is shown below.

When the SDIRn flag is set to “0”, PWM output timing shifts and to “1”, it shifts back.

When PWM output timing shifts beyond PWM period, the exceeding period comes out in the opposite side of the shift direction in the same period. (when shifting back, it comes out forward and when shifting ahead, it comes out backward).

In using saw-tooth wave, PWM output timing can shift only ahead.

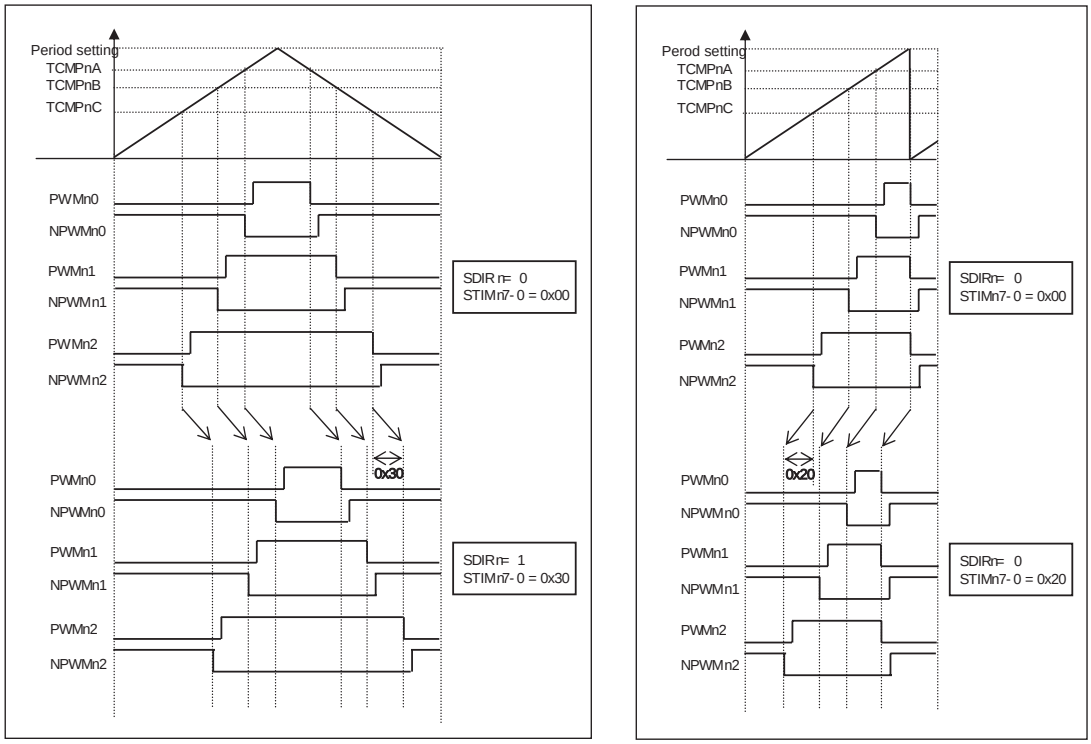


Figure:10.3.7 PWM Output Timing Control

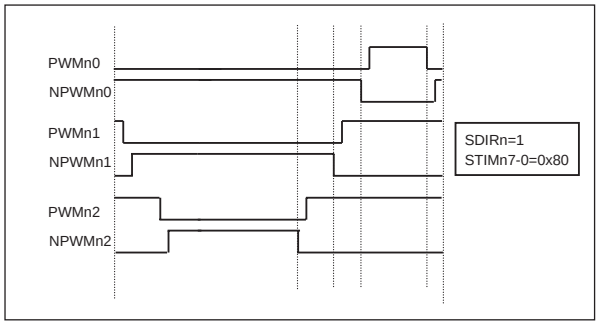


Figure:10.3.8 Output Timing at exceeding PWM period

Chapter 11 Watchdog Timer

11

11.1 Overview

This LSI has an internal 24-bit binary counter that can be used as a 16- to 24-bit watchdog timer. A watchdog timer overflow can generate a non-maskable interrupt. And if an overflow occurs for the second time in a row without clearing the binary counter of the watchdog timer, it is judged unable to return by software. Then, forced hard reset will be executed.
The watchdog timer is also used as an oscillation stabilization wait timer.

11.1.1 Functions

Table: 11.1.1 shows watchdog timer functions.

Table:11.1.1 Watchdog Timer Functions

	Watchdog timer
Interrupt source	WDOVFIRQ
Bit count for the binary counter	16, 18, 20, 22, and 24 bits
Overflow period	6.65 ms to 1677.72 (when the oscillation frequency is 10 MHz)
Oscillation stabilization wait time	26.21 ms (when reset is released; when the oscillation frequency is 10 MHz)
Self-reset function	The chip can be self-reset internally by writing to the RSTCTR register.
Forced-reset function	Forced hard reset in case of an overflow generation for the second time in a row

11.1.2 Block Diagram

■ Watchdog Timer Block Diagram

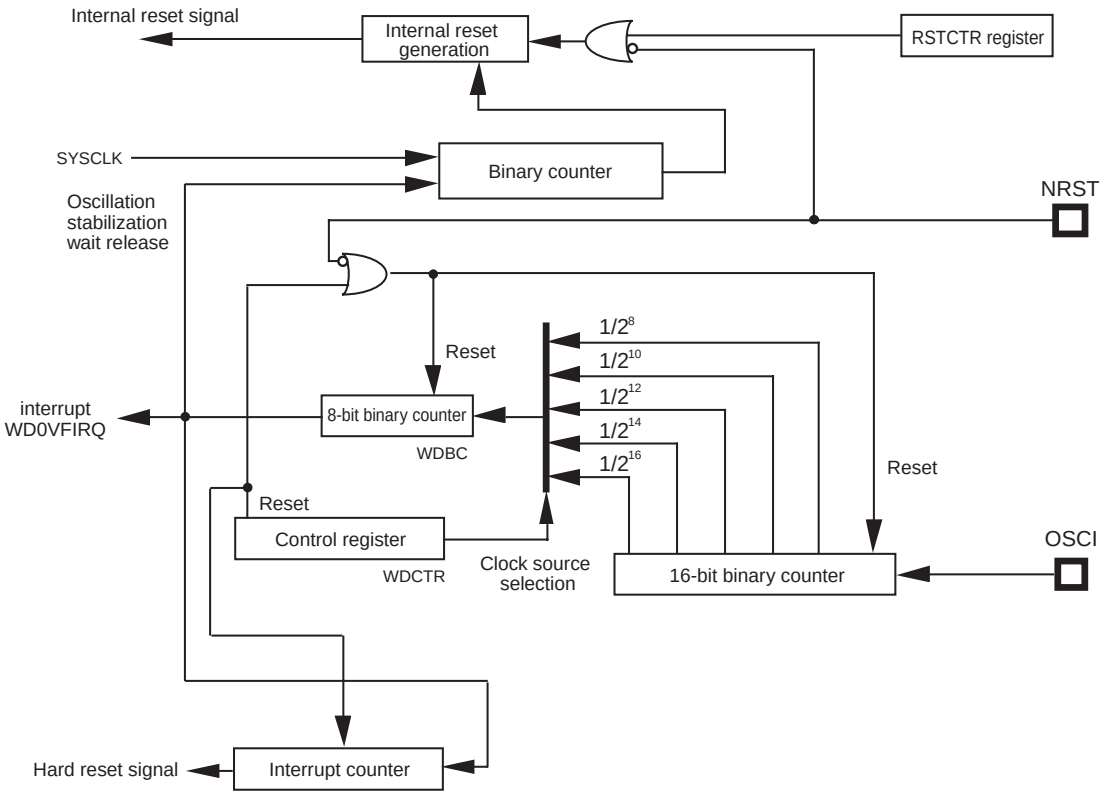


Figure:11.1.1 Watchdog Timer Block Diagram

11.2 Control Registers

Watchdog Timer is composed of the watchdog binary counter (WDBC), watchdog timer control register (WDCTR) and reset control register (RSTCTR).

11.2.1 Watchdog Timer Control Registers

Table: 11.2.1 shows registers which control watchdog timers.

Table:11.2.1 Watchdog Timer Control Registers

Register	Address	R/W	Access size	Description	Page
WDBC	0x00008200	R	8,16	Watchdog binary counter	XI-4
WDCTR	0x00008202	R/W	8,16	Watchdog timer control register	XI-5
RSTCTR	0x00008204	R/W	8,16	Reset control register	XI-6

R/W Readable / Writable
R Readable only
W Writable only

11.2.2 Watchdog Binary Counter

Watchdog binary counter is used to read the upper 8-bits of a 24-bit binary counter. If the counter value changes during read, the returned value is not guaranteed.

■ Watchdog Binary Counter (WDBC: 0x00008200) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	WD BC7	WD BC6	WD BC5	WD BC4	WD BC3	WD BC2	WD BC1	WD BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

11.2.3 Watchdog Timer Control Register

The watchdog timer control register (WDCTR) is used to control the watchdog timer.

■ Watchdog Timer Control Register (WDCTR: 0x00008202) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	WD CNE	WD RST	-	-	-	WD CK2	WD CK1	WD CK0
At reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7	WDCNE	Watchdog timer operation enable	0: Operation disabled (The oscillation stabilization wait operation is possible) 1: Operation enabled
6	WDRST	Watchdog binary counter reset	0: No reset 1: Reset
5-3	-	-	-
2-0	WDCK2 WDCK1 WDCK0	Count clock source for Binary counter selection	000: 1/2^8 of the oscillation frequency 001: 1/2^10 of the oscillation frequency 010: 1/2^12 of the oscillation frequency 011: 1/2^14 of the oscillation frequency 100: 1/2^16 of the oscillation frequency 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

Before changing the values of WDCK2 to 0, stop the watchdog timer and reset the counter.

When “1” is written to the WDRST flag, this flag generates 1 clock wide reset pulse and then changes back to “0”. “0” is always returned when this flag is read.

11.2.4 Reset Control Register

Reset control register is used to generate a self-reset (internal reset).

■ Reset Control Register (RSTCTR: 0x00008204) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	CHIP RST
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W

bp	Flag	Description	Setting condition
7-1	-	-	-
0	CHIPRST	Self-reset (internal reset)	A self-reset is generated when this flag is overwritten from “0” to “1”. A self-reset is not generated if this flag is set to “1” when it contains “1”. This flag value is retained even after the self-reset. The CHIPRST flag is cleared either by an external reset signal or when “0” is written to this flag by the program.

11.3 Operation

11.3.1 Oscillation Stabilization Wait Operation

■ Oscillation Stabilization Wait Operation

The oscillation stabilization wait operation is for the oscillation circuit recovering from stop mode.

The oscillation stabilization wait time is automatically inserted when the reset state is released.

The oscillation stabilization wait is not operated with the self-reset by the reset control register (RSTCTR).

The oscillation stabilization wait is operated even if the WDCNE flag of the watchdog timer control register (WDCTR) is “0”.

■ Oscillation Stabilization Wait Time

The oscillation stabilization wait time is 26.21 ms (when the oscillation frequency is 10 MHz). The timer to count the oscillation stabilization wait time is used as watchdog timer. It also is used as a incorrect code execution watchdog timer except at reset releasing. The watchdog timer is initialized at reset state and starts to count the oscillation frequency as a clock source. It continues to count as a watchdog timer after the oscillation stabilization wait stops.

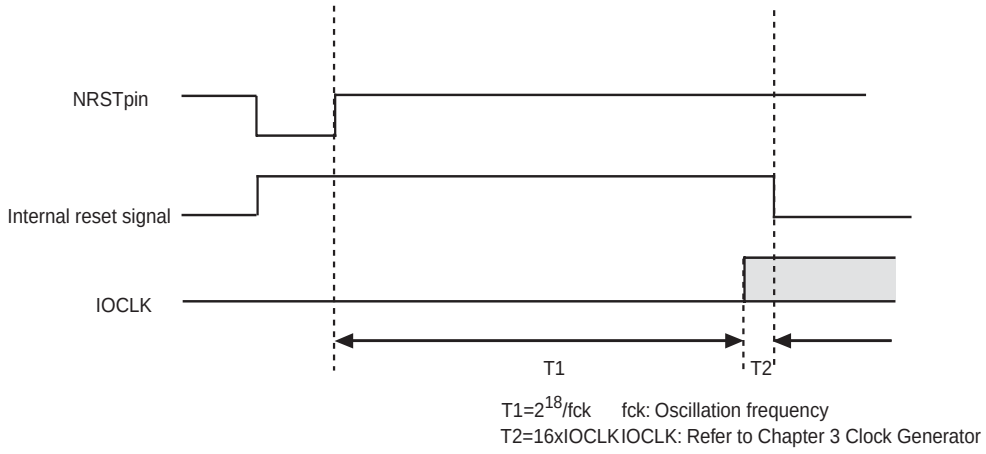


Figure:11.3.1 Oscillation Stabilization Wait Operation (When Reset is Released)

11.3.2 Watchdog Operation

The watchdog timer counts the oscillation frequency as a clock source. If the watchdog timer is overflowed, the watchdog interrupt (WD0VFIRQ) is generated as a non-maskable interrupt (NMI). The watchdog timer control register (WDCTR) sets when the watchdog timer is released and how long the time-out period should be.

■ Watchdog Timer Operation

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. As a result of the software failure, the software cannot execute in the intended sequence; so, the watchdog timer is cleared in the certain cycle. The watchdog timer overflows to detect errors.

■ Starting Watchdog Timer Operation and Watchdog Time-out Period

The watchdog binary counter is reset by setting the WDRST flag of the WDCTR register to “1”. The clock source is selected by the WDCK2-0 flags of the WDCTR register. Table: 11.3.1 shows the set up values and types. The watchdog time-out period is decided by the clock source.

The overflow period of the watchdog timer is calculated by the formula as follows.

Overflow period = $2^{(16+WDCK\times2)}$ / fck [sec]

fck: Oscillation clock frequency
WDCK: WDCK[2:0]

The watchdog time-out period is generally decided from the execution time for main routine of program. The watchdog timer operation is started by setting the WDCNE flag of the WDCTR register to “1”.

Table:11.3.1 Clock Source for Watchdog Timer and Overflow Period

WDCK2	WDCK1	WDCK0	Clock source	Overflow period (at 10 MHz oscillation)
0	0	0	$1/2^8$ of the oscillation frequency	6.55ms
0	0	1	$1/2^{10}$ of the oscillation frequency	26.21ms
0	1	0	$1/2^{12}$ of the oscillation frequency	104.86ms
0	1	1	$1/2^{14}$ of the oscillation frequency	419.43ms
1	0	0	$1/2^{16}$of the oscillation frequency	1677.72ms
1	0	1	Setting prohibited	-
1	1	0	Setting prohibited	-
1	1	1	Setting prohibited	-

■ Detecting Incorrect Code Execution

The watchdog timer detects error when it overflows. When the watchdog timer detects any error, the watchdog interrupt (WD0VFIRQ) is generated as a non maskable interrupt (NMI).

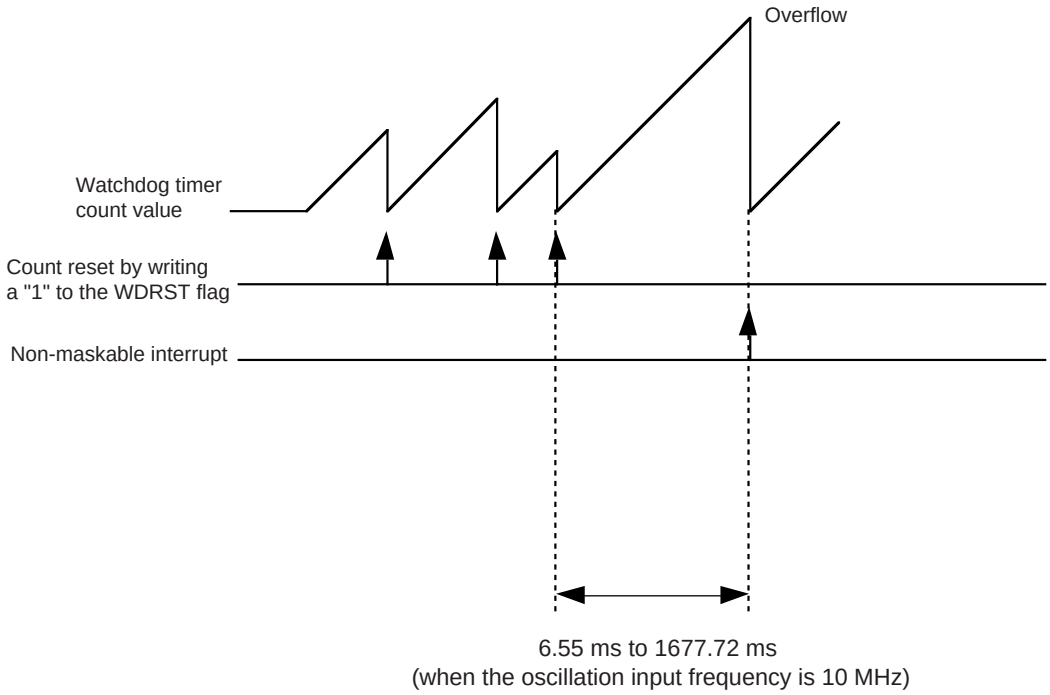


Figure:11.3.2 Watchdog Operation

■ Stopping and Clearing Watchdog Timer Operation

Set the WDCNE flag of the WDCTR register to “0” to stop the watchdog timer operation.

Stop the watchdog timer operation for sure in the following case.

- Before changing the WDCK2-0 flags of the WDCTR register

Set the WDRST flag of the WDCTR register to “1” to clear the watchdog timer . Be sure to clear the watchdog timer in the following cases.

- Before starting the watchdog timer operation
- Before changing the WDCK2-0 flags of the WDCTR register

11.3.3 Self-reset Operation

Self-reset operation is to reset the internal chip software.

■ Self-reset Operation

A self-reset is generated by setting the CHIPRST flag of the reset control register (RSTCTR) from “0” to “1”. A s elf-reset is not operated if the CHIPRST flag set to “1” when it contains “1”. The CHIPRST flag retains the value after the self-reset. The reset generated by the self-reset is an internal reset signal within the chip and does not appear on the external reset pin. The oscillation stabilization wait is not operated.

11.3.4 Forced-reset Operation

■ Forced-reset Operation

If an overflow occurs for the second time in a row without clearing the binary counter of watchdog timer, it is judged unable to return by software. And forced hard reset will be executed. After reset, the hard reset execute oscillation stabilization wait operation again. However, it does not appear on the external reset pin.

Chapter 12 Serial interface 0 and 1

12

12.1 Overview

Serial interface 0 and 1 can be used for both communication types of clock synchronous and UART (Universal Asynchronous Receiver).

12.1.1 Functions

Table: 12.1.1 shows functions for serial interface 0 and 1.

Table:12.1.1 Functions for Serial Interface 0 and 1

	Serial0		Serial1	
Communication style	Clock synchronous	UART(duplex)	Clock synchronous	UART(duplex)
Interrupt	SC0TIRQ(at transmission) SC0RIRQ(at reception)	SC0TIRQ(at transmission) SC0RIRQ(at reception)	SC1TIRQ(at transmission) SC1RIRQ(at reception)	SC1TIRQ(at transmission) SC1RIRQ(at reception)
Pin	SBO0,SBI0,SBT0	SBO0,SBI0	SBO1,SBI1,SBT1	SBO1,SBI1
3-channel communication	O	-	O	-
2-channel communication	-	O	-	O
1-channel communication	-	-	-	-
Transfer bit count specification/frame selection	7 to 8 bits	7 bits+1STOP 7 bits+2STOP 8 bits+1STOP 8 bits+2STOP	7 to 8 bits	7 bits+1STOP 7 bits+2STOP 8 bits+1STOP 8 bits+2STOP
Parity bit selection	O	O	O	O
Parity bit control	0 parity 1 parity odd parity even parity	0 parity 1 parity odd parity even parity	0 parity 1 parity odd parity even parity	0 parity 1 parity odd parity even parity
Start condition selection	-	“With” only	-	“With” only
First transfer bit specification	O	O	O	O
Input edge/output edge	-	-	-	-
SBO2 output control after last data transmission	-	-	-	-
Clock source	1/2,1/16 of timer 14 underflow 1/2,1/16 of timer 15 underflow 1/2,1/16 of timer 16 underflow SBT0 pin	1/16 of timer 14 underflow 1/16 of timer 15 underflow 1/16 of timer 16 underflow	1/2,1/16 of timer 14 underflow 1/2,1/16 of timer 15 underflow 1/2,1/16 of timer 16 underflow SBT1 pin	1/16 of timer 14 underflow 1/16 of timer 15 underflow 1/16 of timer 16 underflow
Error detection	Parity error Overrun error	Parity error Overrun error Framing error	Parity error Overrun error	Parity error Overrun error Framing error
Maximum transfer rate	3.0Mbps	375Kbps	3.0Mbps	375Kbps

12.1.2 Block Diagram

■ Serial Interface 0 and 1 Block Diagram

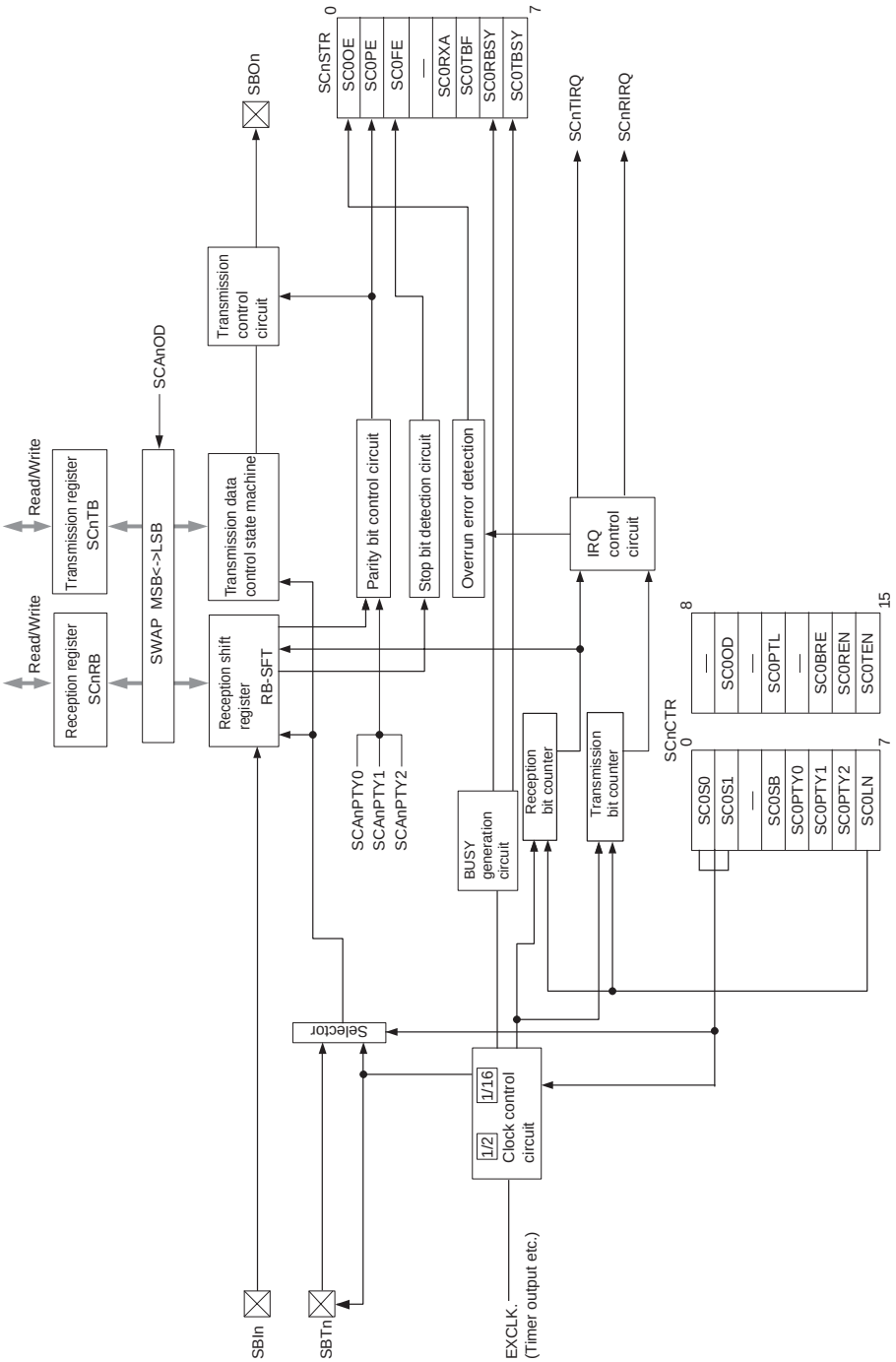


Figure:12.1.1 Serial Interface 0 and 1 Block Diagram

12.2 Control Registers

12.2.1 Registers

Table: 12.2.1 shows registers used to control serial interface 0 and 1.

Table:12.2.1 Control Registers for Serial Interface 0 and 1

	Register	Address	R/W	Access size	Function	Page
Serial 0	SC0RB	0x0000A104	R	8,16	Serial 0 reception register	XII-5
	SC0TB	0x0000A10C	R/W	8,16	Serial 0 transmission register	XII-5
	SC0CTR	0x0000A100	R/W	8,16	Serial 0 control register	XII-6
	SC0STR	0x0000A109	R	8,16	Serial 0 status register	XII-8
	G13ICR	0x00008934	R/W	8,16	Group 13 interrupt control register	V-23
	P2MD	0x0000A032	R/W	8	Port 2 output mode register	VII-14
	P2DIR	0x0000A022	R/W	8	Port 2 I /O control register	VII-13
Serial inter-face 1	SC1RB	0x0000A114	R	8,16	Serial 1 reception register	XII-5
	SC1TB	0x0000A11C	R/W	8,16	Serial 1 transmission register	XII-5
	SC1CTR	0x0000A110	R/W	8,16	Serial 1 control register	XII-7
	SC1STR	0x0000A119	R	8,16	Serial 1 status register	XII-9
	G14ICR	0x00008938	R/W	8,16	Group 14 interrupt control register	V-23
	P2MD	0x0000A032	R/W	8	Port 2 output mode register	VII-14
	P2DIR	0x0000A022	R/W	8	Port 2 I /O control register	VII-13
Serial 0 to 2	SIFCLK	0x0000A10E	R/W	8,16	Serial clock selection register	XII-10

R/W Readable / Writable
R Readable only
W Writable only

12.2.2 Serial Interface Reception and Transmission Registers

Serial interface 0 and 1 each 8-bit data buffer register for transmission/reception.

Data is loaded by reading data from the SCnRB register during serial reception.

Reception data can be loaded when an interrupt occurs or when the SCnRXA flag of the SCnSTR register is “1”. In the case of 7-bit transmission, the MSB (bit 7) is “0”. Proper operation of this register is not guaranteed if data is written. If the register is read through 16-bit access, the reception flag in the status register is cleared.

Data transmission is initiated by writing data to the SCnTB register during serial transmission.

Data transmission starts during 4 transmit clock cycles from write. In the case of 7-bit transmission, the MSB (bit 7) is ignored.

■ Serial 0 Reception Register (SC0RB: 0x0000A104) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA0 RB7	SCA0 RB6	SCA0 RB5	SCA0 RB4	SCA0 RB3	SCA0 RB2	SCA0 RB1	SCA0 RB0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Serial 1 Reception Register (SC1RB: 0x0000A114) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA1 RB7	SCA1 RB6	SCA1 RB5	SCA1 RB4	SCA1 RB3	SCA1 RB2	SCA1 RB1	SCA1 RB0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Serial 0 Transmission Register (SC0TB: 0x0000A10C) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA 0TB 7	SCA 0TB 6	SCA 0TB 5	SCA 0TB 4	SCA 0TB 3	SCA 0TB 2	SCA 0TB 1	SCA 0TB 0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Serial 1 Transmission Register (SC1TB: 0x0000A11C) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA 1TB 7	SCA 1TB 6	SCA 1TB 5	SCA 1TB 4	SCA 1TB 3	SCA 1TB 2	SCA 1TB 1	SCA 1TB 0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2.3 Serial Interface Control Registers

The serial control register is used to set the operation conditions for the corresponding serial interface. This register controls parameters including clock source selection, parity bit selection, protocol selection and enabling of transmission and reception.

■ Serial 0 Control Register (SC0CTR: 0x0000A100) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	SCA0 TEN	SCA0 REN	SCA0 BRE	Rese rved	SCA 0PTL	Rese rved	SCA 0OD	Rese rved	SCA 0LN	SCA 0PT Y2	SCA 0PT Y1	SCA 0PT Y0	SCA 0SB	-	SCA 0S1	SCA 0S0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

bp	Flag	Description	Setting condition
15	SCA0TEN	Transmission enable	0: Transmission disabled 1: Transmission enabled
14	SCA0REN	Reception enable	0: Reception disabled 1: Reception enabled
13	SCA0BRE	Break transmission	0: No break 1: Break
12	Reserved	Reserved	Always set this bit to “0”
11	SCA0PTL	Protocol	0: Start-stop (UART) 1: Synchronous
10	Reserved	Reserved	Always set this bit to 0”
9	SCA0OD	Transmission/reception bit sequence	0: LSB first 1: MSB first
8	Reserved	Reserved	Always set this bit to “0”
7	SCA0LN	Character length	0: 7 bits 1: 8 bits
6-4	SCA0PTY2 SCA0PTY1 SCA0PTY0	Parity bit	000: No parity 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: Fixed at 0 (“L” output) 101: Fixed at 1(“H” output) 110: Even (even number of 1s) 111: Odd (odd number of 1s)
3	SCA0SB	Stop bit	0: 1 bit 1: 2 bits Stop bit selection is valid only in start-stop mode 1 bit judgement at reception
2	-	-	-
1-0	SCA0S1 SCA0S0	Clock source	00: SBT0 01: 1/2 of timer n underflow frequency 10: Setting prohibited 11: 1/16 of timer n underflow frequency 1/2 of timer n underflow is not available in start-stop mode.

■ Serial 1 Control Register (SC1CTR: 0x0000A110) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	SCA 1TEN	SCA1 REN	SCA1 BRE	Rese rved	SCA 1PTL	Rese rved	SCA 1OD	Rese rved	SCA 1LN	SCA 1PT Y2	SCA 1PT Y1	SCA 1PT Y0	SCA 1SB	-	SCA 1S1	SCA 1S0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

bp	Flag	Description	Setting condition
15	SCA1TEN	Transmission enable	0: Transmission disabled 1: Transmission enabled
14	SCA1REN	Reception enable	0: Reception disabled 1: Reception enabled
13	SCA1BRE	Break transmission	0: No break 1: Break
12	Reserved	Reserved	Always set this bit to “0”
11	SCA1PTL	Protocol	0: Start-stop (UART) 1: Synchronous
10	Reserved	Reserved	Always set this bit to 0”
9	SCA1OD	Transmission/reception bit sequence	0: LSB first 1: MSB first
8	Reserved	Reserved	Always set this bit to “0”
7	SCA1LN	Character length	0: 7 bits 1: 8 bits
6-4	SCA1PTY2 SCA1PTY1 SCA1PTY0	Parity bit	000: No parity 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: Fixed at 0 (“L” output) 101: Fixed at 1(“H” output) 110: Even (even number of 1s) 111: Odd (odd number of 1s)
3	SCA1SB	Stop bit	0: 1 bit 1: 2 bits Stop bit selection is valid only in start-stop mode 1 bit judgement at reception
2	-	-	-
1-0	SCA1S1 SCA1S0	Clock source	00: SBT1 01: 1/2 of timer n underflow frequency 10: Setting prohibited 11: 1/16 of timer n underflow frequency 1/2 of timer n underflow is not available in start-stop mode.

12.2.4 Serial Status Registers

The serial status register indicates operation status for serial interface.

Table: 12.2.2 shows generation cause and flag update timing for SCAnFE, SCAnPE, an SCAnOE flags.

Table:12.2.2 Generation Cause and Update Timing of Flags Related with Error

Error	Generation cause	Flag update timing
Framing error	When “0” is received at stop bit reception	At stop bit reception
Parity error	When “1” is received at parity bit fixed to 0, when “0” is received at parity bit fixed to 1, when “odd number” is received at even parity and when “even number” is received at odd parity.	At parity bit reception
Overrun error	When reception of the next data is completed before reception data is read by SCnRB register	At reception of the last bit data

■ Serial 0 Status Register (SC0STR: 0x0000A109) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA0 TBSY	SCA0 RBSY	-	SCA0 RXA	-	SCA0 FE	SCA0 PE	SCA0 OE
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	SCA0TBSY	Transmission status flag	0: Can transmit 1: On transmitting
6	SCA0RBSY	Reception status flag	0: Can receive 1: On receiving
5	-	-	-
4	SCA0RXA	Reception data flag	0: No available 1: Available
3	-	-	-
2	SCA0FE	Framing error	0: No error detected 1: Error detected
1	SCA0PE	Parity error	0: No error detected 1: Error detected
0	SCA0OE	Overrun error	0: No error detected 1: Error detected

■ Serial 1 Status Register (SC1STR: 0x0000A119) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SCA1 TBSY	SCA1 RBSY	-	SCA1 RXA	-	SCA1 FE	SCA1 PE	SCA1 OE
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	SCA1TBSY	Transmission status flag	0: Can transmit 1: On transmitting
6	SCA1RBSY	Reception status flag	0: Can receive 1: On receiving
5	-	-	-
4	SCA1RXA	Reception data flag	0: No available 1: Available
3	-	-	-
2	SCA1FE	Framing error	0: No error detected 1: Error detected
1	SCA1PE	Parity error	0: No error detected 1: Error detected
0	SCA1OE	Overrun error	0: No error detected 1: Error detected

Do not to write data to any of the serial interface status registers.

12.2.5 Serial Clock Selection Registers

Serial clock selection register is used to set a clock for serial interface.

■ Serial Clock Selection Register (SIFCLK: 0x0000A10E) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	-	SC2 CKS1	SC2 CKS0	SC1 CKS1	SC1 CKS0	SC0 CKS1	SC0 CKS0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-6	-	-	-
5-4	SC2CKS1 SC2CKS0	Serial 2 clock source	00: Timer 14 underflow 01: Timer 15 underflow 10: Timer 16 underflow 11: Setting prohibited
3-2	SC1CKS1 SC1CKS0	Serial 1 clock source	00: Timer 14 underflow 01: Timer 15 underflow 10: Timer 16 underflow 11: Setting prohibited
1-0	SC0CKS1 SC0CKS0	Serial 0 clock source	00: Timer 14 underflow 01: Timer 15 underflow 10: Timer 16 underflow 11: Setting prohibited

12.3 Operation

12.3.1 Operation

Serial interface 0 and 1 can be used for both clock synchronous and duplex UART serial interfaces.

12.3.2 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table: 12.3.1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the serial transmission register SCnTB.

Table:12.3.1 Synchronous Serial Interface Activation Factor

	Activation factor		
	Transmission	Reception	Transmission/Reception
Master communication	Set transmission data	Set dummy data	Set transmission data
Slave communication	Input clock after transmission data is set	Input clock	Input clock after transmission data is set

■ Transmission Data Buffer

The transmission data buffer, SCnTB is a buffer of reserve that stores data to load to the internal shift register. Data to be transferred should be set to the transmission data buffer, SCnTB, to be loaded to the internal shift register automatically.

■ Reception Data Buffer

The reception data buffer, SCnRB is a buffer of reserve that pushes the received data in the internal shift register. After the communication complete interrupt SCnTIRQ is generated, all data stored in the internal shift register are stored to the reception data buffer SCnRB automatically. SCnRB can store data up to 1 byte. SCnRB is rewritten in every time when communication is completed, so read out data of SCnRB till the next reception is completed. The reception data flag SCAnRXA is set to “1” after SCnTIRQ is generated. SCAnEXA flag is cleared to “0” after SCnRB is read out.

If a start condition is fed and activation restarts during communication, the transmission data is invalid. Set the transmission data to SCnTB again to retransmit data.

SCnRB is rewritten every time when communication is completed. Data of SCnRB should be read out until the next reception is completed for continuous communication.

■ Setting Transfer Bit

7 to 8 bits can be set as transfer bit count. Set the bit count by the SCAnLN flag of the SCnCTR register. The SCAnLN flag holds the former set value until it is set again.

■ Setting First Transfer Bit

The SCAnOD flag of the SCnCTR register can set the first transfer bit. Whether MSB first or LSB first can be selected. When the transfer bit is set to 7 bits, LSB is first.

■ Transmit Bit Count and First Transfer Bit

In transmission, when the transfer bit count is 7, data is stored in bp0 to 6 as shown in Figure: 12.3.1, store data in bp0 to 6. When the transfer bit is set to 7 bits, LSB is first and data is transferred “A” to “G” in order.

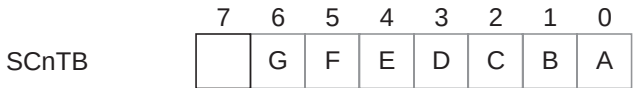


Figure:12.3.1 Transmission Bit Count and First Transfer Bit

■ Receive Bit Count and First Transfer BIt

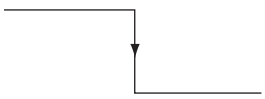
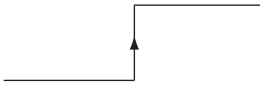
In reception, when the transfer bit count is 7, data is stored in bp0 to 6 as shown in Figure: 12.3.2. When the transfer bit is set to 7 bits, LSB is first, and data is transferred from “A” to “G” in order.

Figure:12.3.2 Reception Bit Count and First Transfer BIt

■ Edge for Output/ Input

Transmission data is output in synchronization with the falling edge of the clock. Reception data is fed in synchronization with the rising edge of the clock.

Table:12.3.2 Edge for Transmission Data Output/Reception Data Input

Edge for transmission data output	Edge for reception output
	

■ Setting Clock

The SCnCKS1 to 0 of the SIFCLK register selects a clock source from the internal clock (clock master), or the SBTn pins selects it from the external clock (clock slave) by .

Table:12.3.3 Synchronous Serial Interface Clock Source

Clock source	Serial interfaces 0 and 1
Internal clock	1/2 of timer 14 underflow
	1/16 of timer 14 underflow
	1/2 of timer 15 underflow
	1/16 of timer 15 underflow
	1/2 of timer 16 underflow
	1/16 of timer 16 underflow
External clock	SBTn pin

■ Setting Data Input/Output Pins

3-channel type (clock pin (SBTn pin), data output pin (SBOn pin), and data input pin (SBIn pin)) is used for communication.

The transfer rate should be up to 3.0 Mbps. If the transfer rate is over 3.0 Mbps, the transmission data may not be sent correctly.

■ Reception Data Flag Operation

After reception is completed (communication complete interrupt SCnTIRQ), data is automatically stored to SCnRB from the internal shift register and the reception data flag SCAnRXA of the SCnSTR register is set to “1”.

The SCAnRXA flag is cleared to “0” by reading data from SCnRB.

■ Reception BUSY Flag Operation

If data is set to the SCnTB or a start condition is recognized with setting SCAnREN flag of the SCnCTR register to “enable”, the reception status flag SCAnRBSY of the SCnSTR register is set to “1”. The SCAnRBSY flag is cleared when the communication complete interrupt SCnTIRQ is generated.

■ Transmission BUSY Flag Operation

If data is set to SCnTB or a start condition is recognized with setting the SCAnTEN flag of the SCnCTR register to “enable”, the reception status flag SCAnTBSY of the SCnSTR register is set to “1”. The SCAnTBSY flag is cleared when the communication complete interrupt SCnTIRQ is generated.

■ Overrun Error Operation

After reception is completed, if the next data has been already received before reading out of the data of the reception data buffer SCnRB, overrun error is generated and the SCAnOE flag of the SCnSTR register is set to “1”. The SCAnOE flag is not cleared till the next communication interrupt SCnTIRQ is generated after loading data of the SCnRB. These error flags have no effects on communication operation.

■ Continuous Commutation

This serial has no continuous transfer function. Do not set data in the transmission data buffer SCnTB during communication.

■ Transmission Timing

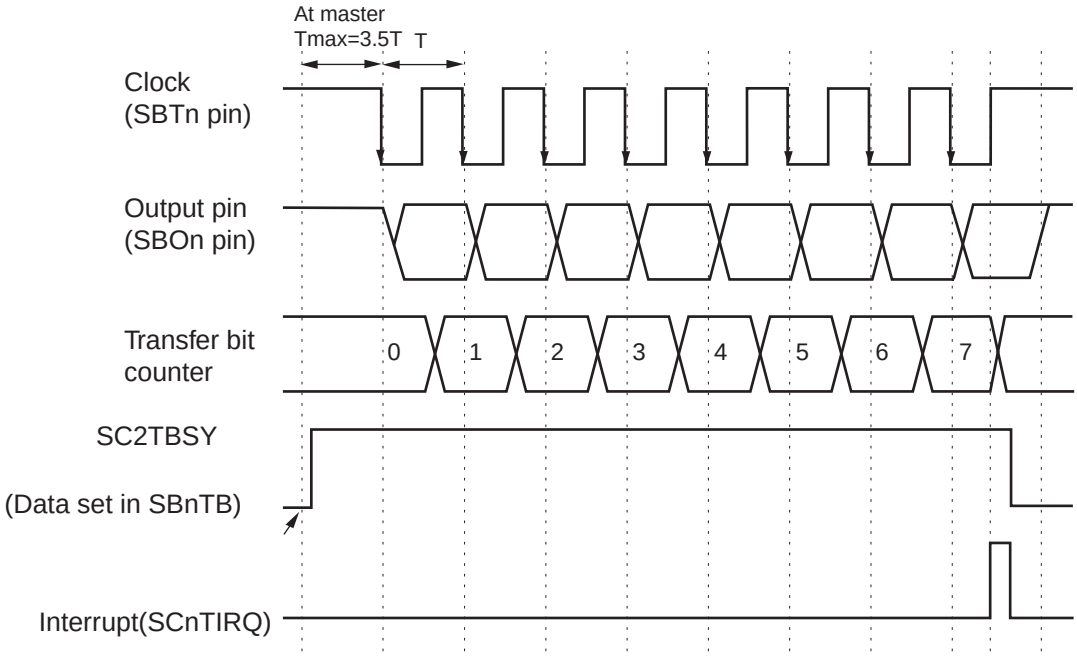


Figure:12.3.3 Transmission Timing (At Falling Edge)

■ Reception Timing

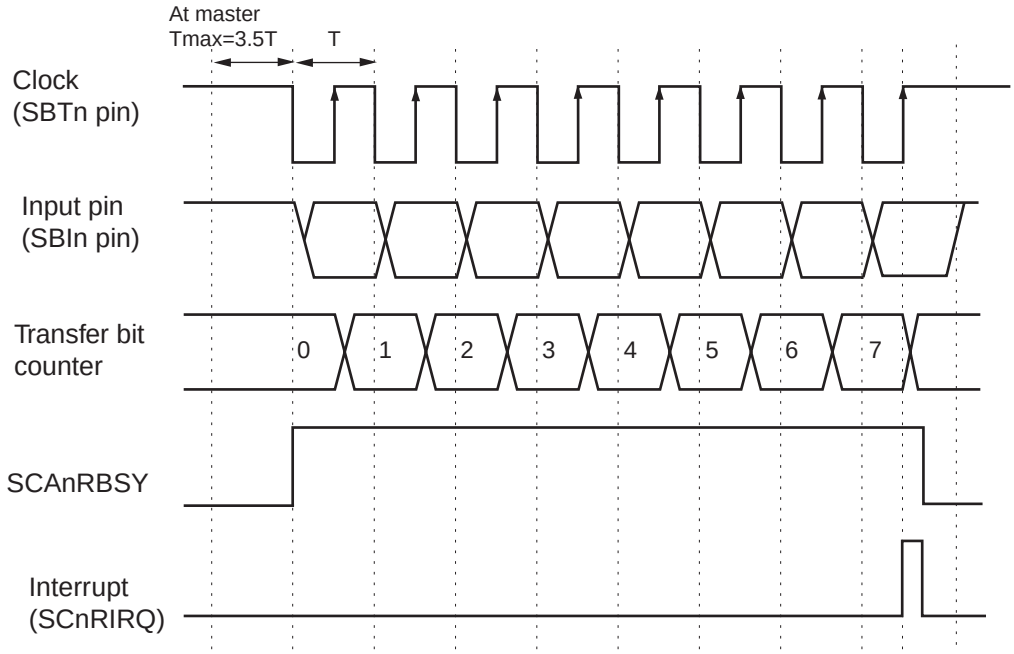


Figure:12.3.4 Reception Timing (At Rising Edge)

■ Transmission/Reception Timing

As data is received at the opposite edge timing (rising edge) of the falling output edge of transmission data, output transmission data at the falling edge and input reception data at the rising edge for the equipment with which the microcontroller is exchanging data.

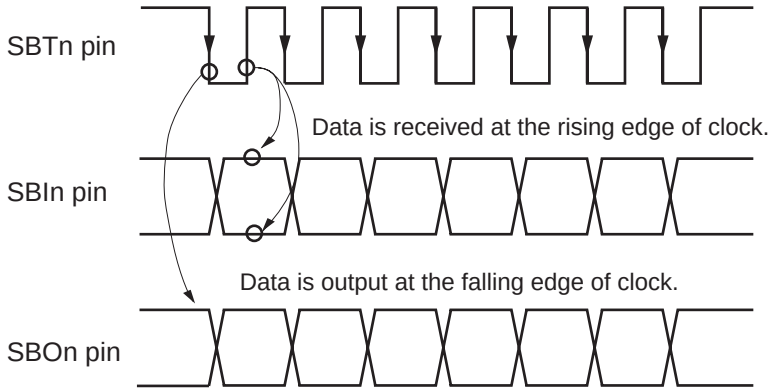


Figure:12.3.5 Transmission/Reception Timing (Reception: Rising Edge, Transmission: Falling Edge)

12.3.3 Setup Example

■ Transmission/Reception Setup Example

The setup example for clock synchronous serial communication with serial 0 is shown. Table: 12.3.4 shows the conditions at transmission/reception.

Table:12.3.4 Setup Example for Synchronous Serial Interface Transmission/Reception

Setup item	Description
SBI2/SBO2 pin setting	Independent (3 channels)
Transfer bit count	8 bits
Parity bit	Even parity
First transfer bit	MSB
Clock	Clock master
Timer for clock	Timer 14
Clock source	1/2 of timer 14 underflow
SBI0sbt0 pin pull-up resistor	Added
Serial 0 communication complete interrupt	Enable

Setup Procedure	Description
(1) Start the timer for the clock	(1) Set the baud rate by the TM14MD and TM14BR registers and the TM14CNE flag to “1” to operate the timer 14.
(2) Select the timer for the clock SIFCLK(0x0000A10E) bp1-0: SC0CKS1-0=00	(2) Set the SC0CKS1-0 flag of the SIFCLK register to “00” to select the timer 14 underflow.
(3) Control the pin style P2PLU(0x0000A042) bp7: P27R=1	(3) Set the P27R flag of the P2PLU register to “1” to enable the pull-up resistor.
(4) Control the pin direction P2DIR(0x0000A022) bp7-5: P27D-P25D=011	(4) Set the P25D flag of the P2DIR register to “1” to set P25 (SBO0 pin) to the output pin, the P26D flag to “1” to set P26 (SBT0 pin) to the output pin and the P27D flag to “0” to set P27(SBI0 pin) to the input pin.
(5) Set the pin function P2MD(0x0000A032) bp6-5: P26M-P25M=11	(5) Set the P26M flag of the P2MD register to “1” to set it to SBT0 pin function, and set the P25M flag to “1” to set it to SBO0 pin function.

Setup Procedure	Description
(6) Set the SC0CTR register Set the protocol SC0CTR(0x0000A100) bp11: SCA0PTL=1 Set the first bit to be transferred SC0CTR(0x0000A100) bp9: SCA0OD=1 Set the transfer bit count SC0CTR(0x0000A100) bp7: SCA0LN=1 Set the parity SC0CTR(0x0000A100) bp6-4: SCA0PTY2-0=110 Set the clock source SC0CTR(0x0000A100) bp1-0: SCA0S1-0=0	(6) Set the SCA0PTL flag of the SC0CTR register to “1” to select synchronous communication. Set the SCA0OD flag of the SC0CTR register to “1” to set the first transfer bit to MSB. Set the SCA0LN flag of the SC0CTR register to “1” to set the transfer bit count to 8 bits. Set the SCA0PTY2-0 flags of the SC0CTR register to “110” to set the parity bit to even parity. Set the SCA0S1-0 flags of the SC0CTR register to “01” to set the clock source to 1/2 cycle of the timer 14 underflow.
(7) Enable the transmission / reception SC0CTR(0x0000A100) bp14: SCA0REN=1 bp15: SCA0TEN=1	(7) Set the SCA0REN flag of the SC0CTR register to “1” to enable reception, and set the SCA0TEN flag to “1” to enable transmission.
(8) Set the interrupt level G13ICR(0x00008934) bp14-12: G13LV2-0=100	(8) Set the interrupt by the G13LV2-0 flags of the GI131CR register.
(9) Enable the interrupt G13ICR(0x00008934) bp9: G13IE1=1	(9) Set the G13IE1 flag of the G13ICR register to “1” to enable the interrupt. If any interrupt request flag (the G13IR1 of the G13ICR register) has been already set, clear the G13IR1 flag to enable the interrupt.
(10) Start the serial transmission Transmission data→SC0TB(0x0000A10C) Reception data→Input to the SBI0sbi0 pin	(10) Set transmission data to the serial 0 transmission register (SC0TB). The transfer clock is generated and transmission or reception is started. When the transmission is finished, the serial 0 interrupt SC0TIRQ is generated.

Note: Each in (6) can be set at the same time.

12.3.4 UART Serial Interface

■ Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer SCnTB, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. In reception, if the data length of “L” for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■ Transmission

Data transfer is automatically started by setting data to the transmission data buffer SCnTB. When the transmission is completed, the serial transmission interrupt SCnTIRQ is generated.

■ Reception

Once a start condition is received, the reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial reception interrupt SCnRIRQ is generated.

■ Duplex Communication

On duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■ Transmission Data Buffer

Refer to: XII-11

■ Reception Data Buffer

Refer to: XII-11

■ First Transfer Bit Setup

Refer to: XII-12

■ Transmission Bit Count and First Transfer Bit

Refer to: XII-12

■ Reception Bit Count and First Transfer Bit

Refer to: XII-12

■ Clock Setup

Transfer clock is not necessary for UART communication itself but necessary for setup of data transmission/ reception timing in the serial interface. Select the timer to be used as a baud rate timer by the SISFCLK register.

■ Break Status Transmission Control Setup

The SCAnBRE flag of the SCnCTR register generates the break status. If SCAnBRE is set to “1” to select the break transmission, all bits from start bits to stop bits transfer “0”.

■ Frame Setup

Figure: 12.3.6 shows the data format at UART communication.

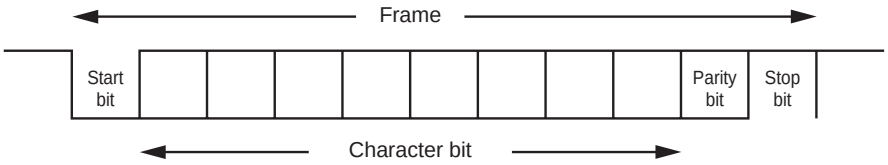


Figure:12.3.6 UART Serial Interface Transmission/Reception Data Format

Transmission/reception data consists of start bit, character bit, parity bit and stop bit. Table: 12.3.5 shows its kinds to be set.

Table:12.3.5 UART Serial Interface Transmission/Reception Data

Start bit	1 bit
Character bit	7,8 bits
Parity bit	Fixed to 0, fixed to 1, odd, even, none
stop bit	1,2 bits

The SCAnLN flag of the SCnCTR register is used to set character bit to 7 or 8 bits.

The SCAnS1-0 flags of the SCnCTR register are used to set stop bit to 1 or 2 bits.

1 bit judgement is set at reception regardless of setting.

Parity bit is used to detect wrong bits of transmission/reception data. Table: 12.3.6 shows kinds of parity bit. The SCAnPTY2-0 flags of the SCnCTR register set parity bit.

Table:12.3.6 UART Serial Interface Parity Bit

SCnCTR			Parity bit	Description
SCAnPTY2	SCAnPTY1	SCAnPTY0		
0	0	0	None	Do not add parity bit
0	0	1	Setting prohibited	
0	1	0		
0	1	1		
1	0	0	Fixed at 0	Set parity bit to “0”
1	0	1	Fixed at 1	Set parity bit to “1”
1	1	0	Even parity	Control that the total of “1” of parity bit and character bit should be even
1	1	1	Odd parity	Control that the total of “1” of parity bit and character bit should be odd

■ Setting Data I/O Pin

2 channels (data output pin (SBO pin), data input pin (SBIn pin)) are used for communication.

■ Reception Data Flag Operation

Data is automatically stored to SCnRB from the internal shift register when the reception complete interrupt SCnRIRQ is generated. If data is stored in the shift register SCnRB, the reception data flag SCAnRXA of the SCnSTR register is set to “1”. This indicates that reception data is ready to be read out. SCAnRXA is cleared to “0” by reading out SCnRB data.

■ Reception BUSY Flag Operation

When a start condition is recognized, the SCAnRBSY flag of the SCnSTR register is set to “1”. It is cleared to “0” after the reception complete interrupt SCnRIRQ is generated.

■ Transmission BUSY Flag Operation

When SCnTB data is set, the SCAnTBSY flag of the SCnSTR register is set to “1”. Is is cleared to “0” after the transmission complete interrupt SCnTIRQ is generated.

■ Reception Error

Errors at reception have 3 types, overrun error, parity error, and framing error. Reception error can be determined by the SCAnOE, SCAnPE and SCAnFE flags of the SCnSTR register. The SCAnPE and SCAnFE flags of the reception error flags are renewed at generation of the communication complete interrupt SCnRIRQ. After reading data of SCnRB, The SCAnOE flag is cleared at the same time when the next communication complete interrupt SCnRIRQ is generated. The judgement of the reception error flag should be operated until the next communication is completed. These error flags have no effects on communication operation. The reception error source is shown in the following table.

Table:12.3.7 Reception Error Source of UART Serial InterfaceS

Flag	Reception error		
SCAnOE	Overrun error	The next data is received before the reception buffer is read.	
SCAnPE	Parity error	Fixed to 0	When parity bit is “1”
		Fixed to 1	When parity bit is “0”
		Odd parity	When the total of “1” of parity bit and character bit is even
		Even parity	When the total of “1” of parity bit and character bit is odd
SCAnFE	Framing error	Stop bit is not detected.	

■ Continuous Communication

This serial has no continuous transfer function. Do not set data in the transmission data buffer SCnTB during transmission.

■ Transmission Timing

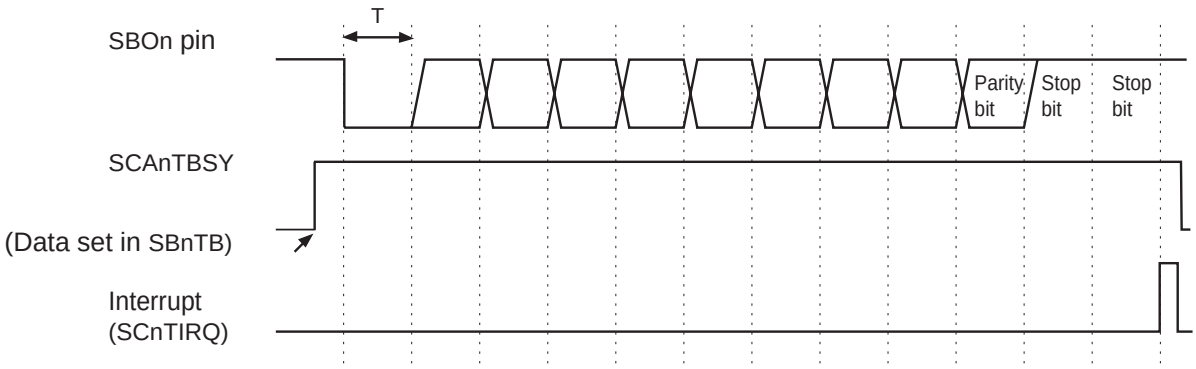


Figure:12.3.7 Transmission Timing (With Parity bit)

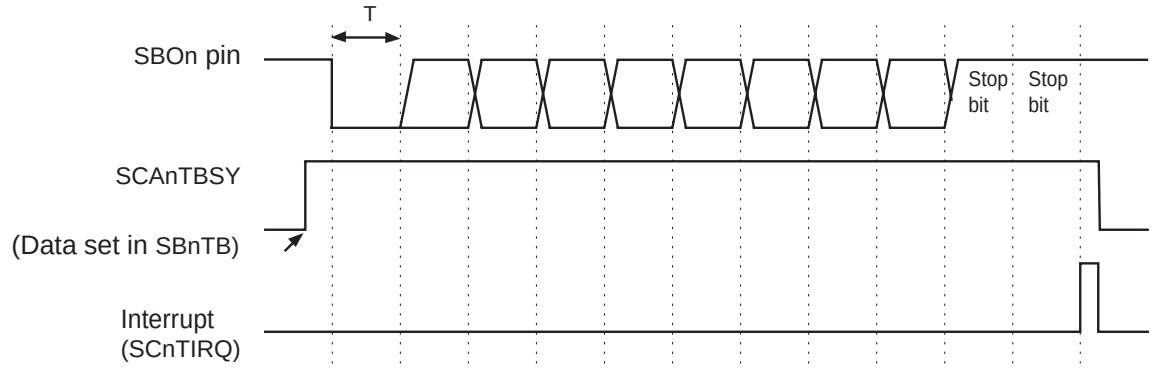


Figure:12.3.8 Transmission Timing (Without Parity bit)

■ Reception Timing

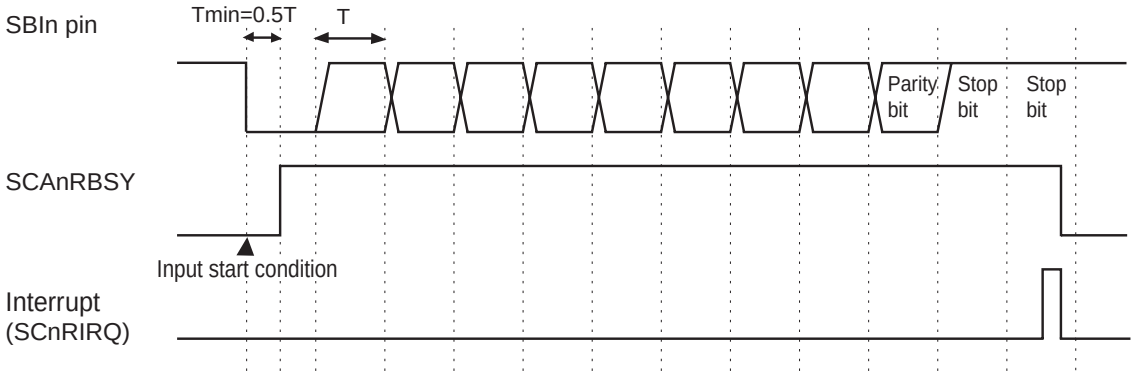


Figure:12.3.9 Reception Timing (With Parity bit)

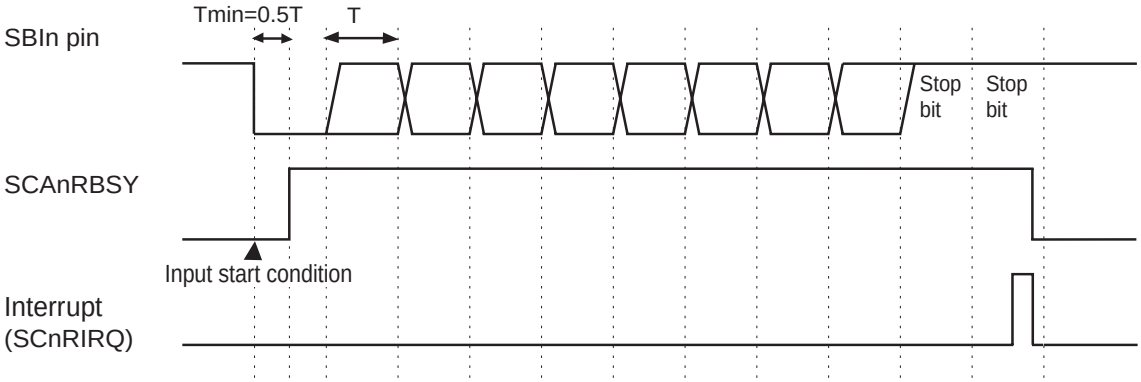


Figure:12.3.10 Reception Timing (Without Parity bit)

■ Transfer Speed Setup

Any transfer rate can be set by using baud rate timer (timer 14, timer 15 and timer 16). Table: 12.3.8 shows the setup example of the transfer speed.

Table:12.3.8 UART Serial Interface Transfer Speed Setting Register

Setup	Register	Page
Serial clock source setting (setting 1/16 of timer underflow)	SCnCTR	XII-6, XII-7
Timer selection	SIFCLK	XII-10

The value of timer base register is set as follows:

Underflow cycle = (Base register set value + 1) × Timer clock cycle

Baud rate = 1/(Underflow cycle × 16) (“16” represents 1/16 of a clock source)

therefore,

Base register set value = Timer clock frequency/(Baud rate × 16) - 1

For example, if the baud rate is 300 bps at timer clock source IOCLK/32 (Input frequency = 10 MHz, 6 multiplication and IOCLK = MCLK/2), the set value is as follows:

Base register setting value = $(30 \times 10^6 /32) (300 \times 16) - 1$
=194
=x’C2

The table 12.3.9 shows the clock source with the standard rate and the set value of the base register at MCLK=60 and MHz (IOCLK=MCLK/2).

Transfer rate should be selected under 375 kbps.

Table:12.3.9 The Set Value of Transfer Speed (Register Set Value: Hexadecimal)

Timer clock source IOCLK/n		1	8	32	128
Transfer Speed (bps)	300	1869	30C	C2	30
	960	7A0	F3	3C	E
	1200	61A	C2	30	B
	2400	30C	61	17	5
	4800	186	30	B	2
	9600	C2	17	5	-
	19200	61	B	2	-
	28800	40	7	-	-
	38400	30	5	-	-
	76800	17	2	-	-

12.3.5 UART Serial Interface Setup

■ UART Serial Interface Setup

The setup example for UART transmission/reception with serial 0 is shown. Table: 12.3.10 shows the condition for transmission/reception.

Table:12.3.10 UART Interface Transmission/Reception Condition

Setup item	Description
SBI0/SBO0 pin setting	Independent (2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 14
Parity bit add / check	"0" added / check
Serial 0 transmission complete interrupt	Enable
Serial0 reception complete interrupt	Enable

An setup procedure, with a description of each steps is shown below.

Setup Procedure	Description
(1) Set the baud rate timer	(1) Set the baud rate by the TM14MD and TM14BR registers, and set the TM14CNE flag to 1 to operate the timer 14.
(2) Select the baud rate timer SIFCLK(0x0000A10E) bp5-4: SC0CKS2-1=00	(2) Set the SC0CKS2-1 flags of the SIFCLK register to “00” to set the timer 14 underflow to the baud rate timer.
(3) Set the pin function P2MD(0x0000A032) bp5: P25M=1	(3) Set the P25M flag of the P2MD register to “1” to set it to SB0 pin function .
(4) Control the pin direction P2DIR(0x0000A022) bp27: P27D=0 bp25: P25D=1	(4) Set the P25D flag of the P2DIR register to “1” to set P25 to output mode , and set the P27D flag to “0” to set P27 to input mode.

Setup Procedure	Description
(5) Set the SC0CTR register Set the protocol SC0CTR(0x0000A100) bp11: SCA0PTL=0 Set the first transfer bit SC0CTR(0x0000A100) bp9: SCA0OD=1 Set the transfer bit count SC0CTR(0x0000A100) bp7: SCA0LN=1 Set the parity bit SC0CTR(0x0000A100) bp6-4: SCA0PTY2-0=100 Set the stop bit SC0CTR(0x0000A100) bp3: SCA0SB=1 Set the clock source SC0CTR(0x0000A100) bp1-0: SCA0S1-0=11	(5) Set the SCA0PTL flag of the SC0CTR register to “0” to select the UART (start-stop) communication. Set the SCA0OD flag of the SC0CTR register to “1” to set the first transfer bit to MSB. Set the SCA0LN flag of the SC0CTR register to “1” to set the transfer bit count to 8 bits. Set the SCA0PTY2-0 flags of the SC0CTR register to “100” to select “ fixed at 0”. Set the SCA0SB flag of the SC0CTR register to “1” to set the stop bit to 2 bits. Set the SCA0S1-0 flags of the SC0CTR register to “11” to set the clock source to 1/16 of the timer 14 underflow.
(6) Enable the transmission/reception SC0CTR(0x0000A100) bp14: SCA0REN=1 bp15: SCA0TEN=1	(6) Set the SCA0REN flag of the SC0CTR register to “1” to enable reception, and set the SCA0TEN flag to “1” to enable transmission.
(7) Set the interrupt level G13ICR(0x00008934) bp14-12: G13LV2-0=100	(7) Set the interrupt level by the G13LV2-0 flags of the G13ICR register.
(8) Enable the interrupt G13ICR(0x00008934) bp8: G13IE0=1 bp9: G13IE1=1	(8) Set the G13IE0 flag of the G13ICR register to “1” and the G13IE1 flag to “1” to enable the interrupt. If an interrupt request flags has been set already, clear the request flag.
(9) Start the serial transmission Transmission data → SC0TB (0x0000A10C) Reception data → Input to the SBI0 pin	(9) Transmission is started by setting transmission data to the serial 0 transmission register (SC0TB). When transmission is completed, the serial 0 transmission interrupt (SC0TIRQ) is generated. Also, reception data is stored in the SBI0sbi0 pin and the serial 0 reception interrupt (SC0RIRQ) is generated.

Note: Each setting in (5) can be set at the same time.

Chapter 13 Serial Interface 2

13

13.1 Overview

Serial interface 2 can be used for both communication types of clock synchronous and UART (Universal Asynchronous Receiver).

13.1.1 Functions

Table: 13.1.1 shows functions with serial interface 2.

Table:13.1.1 Serial Interface 2 Functions

Communication type	Clock synchronous	UART (full duplex)
Interrupt	SC2TIRQ (at completion of transmission)	SC2TIRQ (at completion of transmission) SC2RIRQ (at completion of reception)
Pin	SBO2,SBI2,SBT2	SBO2,SBI2
3-channel communication	O	-
2-channel communication	O SBO2,SBT2	O
1-channel communication	-	O SBO2
Transfer bit count specification/frame selection	1 to 8 bits	7 bits +1STOP 7 bits +2STOP 8 bits +1STOP 8 bits +2STOP
Parity bit selection	-	O
Parity bit control	-	0 parity 1 parity Even parity Odd parity
Start condition selection	O	“With” only
First transfer bit specification	O	O
Input edge/output edge	O	-
SBO2 output control after last data transmission	H/L last data retained	-
Clock source	1/2, 1/4, 1/16, 1/64 of timer 14 underflow 1/2, 1/4, 1/16, 1/64 of timer 15 underflow 1/2, 1/4, 1/16, 1/64 of timer 16 underflow IOCLK/2 IOCLK/4 SBT2 pin	1/32, 1/64, 1/256, 1/1024 of timer 14 underflow 1/32, 1/64, 1/256 , 1/1024 of timer 15 underflow, 1/32, 1/64, 1/256, 1/1024 of timer 16 underflow IOCLK/32 IOCLK/64
Error detection	Overrun error	Parity error Overrun error Frame error
Max. transfer rate	5.0Mbps	300Kbps

13.1.2 Block Diagram

■ Serial Interface 2 Block Diagram

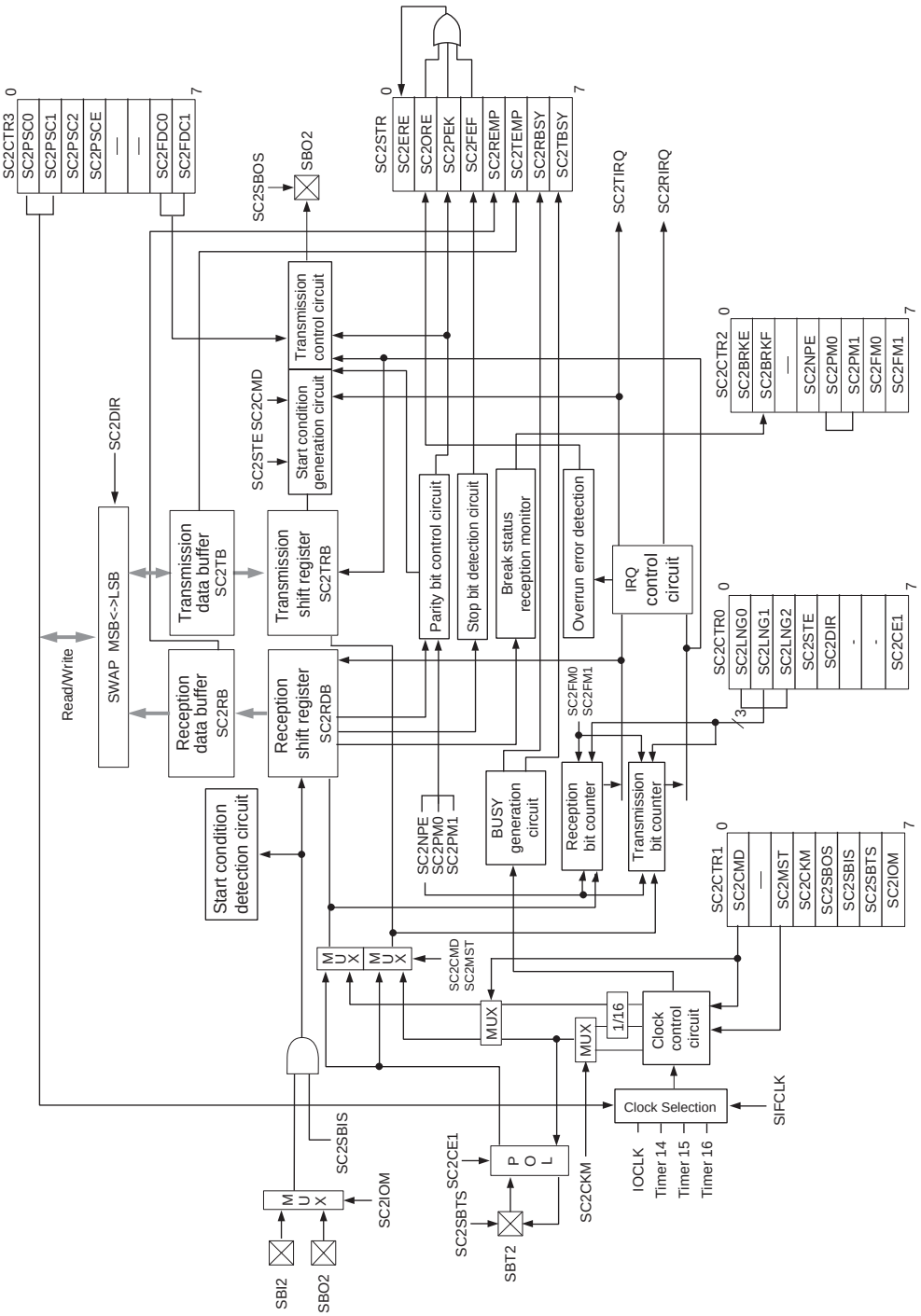


Figure:13.1.1 Serial Interface 2 Block Diagram

13.2 Control Registers

13.2.1 Registers

Table: 13.2.1 shows registers that control serial interface 2.

Table:13.2.1 Serial Interface 2 Control Registers

	Register	Address	R/W	Access size	Function	Page
Serial 2	SC2RB	0x0000A12C	R	8,16	Serial interface 2 reception data buffer	XIII-5
	SC2TB	0x0000A130	R/W	8,16	Serial interface 2 transmission data buffer	XIII-5
	SC2CTR0	0x0000A120	R/W	8	Serial interface 2 mode register 0	XIII-6
	SC2CTR1	0x0000A121	R/W	8	Serial interface 2 mode register 1	XIII-7
	SC2CTR2	0x0000A124	R/W	8	Serial interface 2 mode register 2	XIII-8
	SC2CTR3	0x0000A125	R/W	8	Serial interface 2 mode register 3	XIII-9
	SC2STR	0x0000A128	R	8,16	Serial interface 2 status register	XIII-10
	G15ICR	0x0000893C	R/W	8,16	Group 15 interrupt control register	V-24
	P1MD	0x0000A031	R/W	8	Port 1 output model register	VII-11
	P1DIR	0x0000A021	R/W	8	Port 1 I/O control register	VII-11
	P2MD	0x0000A032	R/W	8	Port 2 output mode register	VII-14
	P2DIR	0x0000A022	R/W	8	Port 2 I/O control register	VII-13
Serial 0 to 2	SIFCLK	0x0000A10E	R/W	8,16	Serial clock selection register	XII-10

R/W Readable / Writable
R Readable only
W Writable only

When changing the setting value of the mode register, rewrite it after setting the serial forced reset.
(Both the SC2BIS flag and the SC2BOS flag of the SC2CTR1 registers are set to "0".)

13.2.2 Serial Interface 2 Data Buffer Register

Serial interface 2 has each 8-bit data buffer register for transmission and reception.

■ Serial Interface 2 Reception Data Buffer (SC2RB: 0x0000A12C)
[8,16-Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 RB7	SC2 RB6	SC2 RB5	SC2 RB4	SC2 RB3	SC2 RB2	SC2 RB1	SC2 RB0
At reset	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R

■ Serial Interface 2 Transmission Data Buffer (SC2TB: 0x0000A130)
[8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 TB7	SC2 TB6	SC2 TB5	SC2 TB4	SC2 TB3	SC2 TB2	SC2 TB1	SC2 TB0
At reset	×	×	×	×	×	×	×	×
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.2.3 Serial Interface 2 Mode Register

These registers are readable/writable 8-bit registers that control serial interface 2

■ Serial Interface 2 Mode Register 0 (SC2CTR0: 0x0000A120) [8-bit Access Register]

Table:13.2.2 Serial Interface 2 Mode Register 0

bp	7	6	5	4	3	2	1	0
Flag	SC2 CE1	-	-	SC2 DIR	SC2 STE	SC2 LNG2	SC2 LNG1	SC2 LNG0
At reset	0	0	0	0	0	1	1	1
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7	SC2CE1	Transmission data output edge Reception data input edge	Transmission data output edge 0: Falling 1: Rising Reception data input edge 0: Rising 1: Falling
6-5	-	-	-
4	SC2DIR	Transfer bit specification	0: MSB first 1: LSB first
3	SC2STE	Start condition selection	0: Without 1: With
2-0	SC2LNG2 SC2LNG1 SC2LNG0	Synchronous serial transfer bit count	000: 1bit 001: 2bit 010: 3bit 011: 4bit 100: 5bit 101: 6bit 110: 7bit 111: 8bit

■ Serial Interface 2 Mode Register 1 (SC2CTR1: 0x0000A121) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 IOM	SC2 SBTS	SC2 SBIS	SC2 SBOS	SC2 CKM	SC2 MST	-	SC2 CMD
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

bp	Flag	Description	Setting condition
7	SC2IOM	Serial data input pin selection	0: Data input from SB12 1: Data input from SB02
6	SC2SBTS	SBT2 pin function selection	0: Port 1: Transfer clock I/O
5	SC2SBIS	Serial input control selection	0: “1” input fix 1: Serial data input
4	SC2SBOS	SBO2 pin function selection	0: Port 1: Serial data output
3	SC2CKM	1/16 dividing of transfer clock selection	0: No 1: Yes 1/16 dividing is set regardless of setting at UART communication.
2	SC2MST	Clock master/slave selection	0: Clock slave 1: Clock master
1	-	-	-
0	SC2CMD	Synchronous serial/full duplex UART selection	0: Synchronous serial 1: Full duplex UART

When changing the setting value of the mode register, rewrite it after setting the serial forced reset.
(Both the SC2BIS flag and the SC2BOS flag of the SC2CTR1 registers are set to "0".)

■ Serial Interface 2 Mode Register 2 (SC2CTR2: 0x0000A124) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 FM1	SC2 FM0	SC2 PM1	SC2 PM0	SC2 NPE	-	SC2 BRKF	SC2 BRKE
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

bp	Flag	Description	Setting Condition
7-6	SC2FM1 SC2FM0	Frame mode specification	00: 7 data bits + 1 stop bit 01: 7 data bits + 2 stop bits 10: 8 data bits + 1 stop bit 11: 8 data bits + 2 stop bits
5-4	SC2PM1 SC2PM0	Additional bit specification (at transmission)	00: “0” added 01: “1” added 10: Odd parity added 11: Even parity added
		Additional bit specification (at reception)	00: "0" checked 01: "1" checked 10: Odd parity checked 11: Even parity checked
3	SC2NPE	Parity enable	0: Parity enabled 1: Parity disabled
2	-	-	-
1	SC2BRKF	Break status reception monitor	0: Data reception 1: Break reception
0	SC2BRKE	Break status transmission control	0: Data transmission 1: Break transmission

■ Serial Interface 2 Mode Register 3 (SC2CTR3: 0x0000A125) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 FDC1	SC2 FDC0	-	-	SC2 PSCE	SC2 PSC2	SC2 PSC1	SC2 PSC0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition	
7-6	SC2FDC 1 SC2FDC 0	Output selection after SB0 last data transmission	00: Fixed at "1"(High) output 10: Fixed at "0"(Low) output X1: Last data retained	
5-4	-	-	-	
3	SC2PSCE	Prescaler count control	0: Count disabled 1: Count enabled	
2-0	SC2PSC2 SC2PSC1 SC2PSC0	Clock selection	Clock synchronous	UART
			000: 1/2 of timer underflow 001: 1/4 of timer underflow 010: 1/16 of timer underflow 011: 1/64 of timer underflow 100: IOCLK/2 101: IOCLK/4 110: Setting prohibited 111: Setting prohibited	000: 1/32 of timer underflow 001: 1/64 of timer underflow 010: 1/256 of timer underflow 011: 1/1024 of timer underflow 100: IOCLK/32 101: IOCLK/64 110: Setting prohibited 111: Setting prohibited
			Timer is selected by the serial interface clock selection register (SIFCLK).	

■ Serial Interface 2 Status Register (SC2STR: 0x0000A128) [8,16-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	SC2 TBSY	SC2 RBSY	SC2 TEMP	SC2 REMP	SC2 FEF	SC2 PEK	SC2 ORE	SC2 ERE
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
7	SC2TBSY	Serial bus busy status	0: Other than serial transmission 1: Serial transmission
6	SC2RBSY	Serial bus busy status	0: Other than serial reception 1: Serial reception
5	SC2TEMP	Transmission buffer empty flag	0: Empty 1: Full
4	SC2REMP	Reception buffer empty flag	0: Empty 1: Full
3	SC2FEF	Frame error detection	0: No error detected 1: Error detected
2	SC2PEK	Parity error detection	0: No error detected 1: Error detected
1	SC2ORE	Overrun error detection	0: No error detected 1: Error detected
0	SC2ERE	Error monitor flag	0: No error detected 1: Error detected

13.3 Operation

13.3.1 Serial Interface 2 Operation

Serial interface 2 is used as clock synchronous and full duplex UART serial interface.

13.3.2 Clock Synchronous Serial Interface

■ Activation Factors for Communication

Table: 13.3.1 shows activation factors for communication. In the case of master communication, a transfer clock is generated by setting data to the transfer data buffer SC2TB or by receiving a start condition. Signal input from the SBT2 pin is masked inside serial interface to prevent operating errors by noise, except during communication.This mask is automatically released by setting data to SC2TB (access to the SC2TB register) or feeding a start condition to the data input pin. Therefore, in the case of slave communication, set data to SC2TB or input a start condition before feeding external clock.

However, the external clock should be fed after more than 3.5 transfer clock intervals since data is set in SC2TB. This wait time is necessary to load data from SC2TB into the internal shift register.

Table:13.3.1 Activation Factor for Synchronous Serial Interface

	Activation factor	
	Transmission	Reception
Master communication	Set transmission data	Set dummy data
		Input start condition
Slave communication	Input clock after transmission data is set.	Input clock after dummy data is set.
		Input clock after start condition is input.

■ Transmission Data Buffer

The transmission data buffer SC2TB is a spare buffer that stores data to be loaded into the transmission shift register. Set the data to be transmitted in the transmission data buffer SC2TB; then, data is automatically loaded into the internal shift register. 3.5 transfer clock cycles are required for loading data. If data is set in SC2TB again during data loading, data may not be properly set. Whether data is under loading or not can be determined by monitoring the transmission buffer empty flag SC2TEMP of SC2STR.

When data is set in SC2TB, the SC2TEMP flag is set to “1”, and when data loading is completed, the flag is automatically cleared to “0”.

■ Reception Data Buffer

The reception data buffer SC2RB is a spare buffer that pushes the received data by the reception shift register. After the communication complete interrupt SC2TIRQ is generated, data stored in the reception shift register is automatically stored in the reception data buffer SC2RB. SC2RB can store data up to 1 byte. SC2RB is rewritten in every time when communication is completed; so, read out data of SC2RB until the next reception is completed. The reception data buffer empty flag SC2RB is set to “1” after SC2RB is generated. SC2RB is cleared to “0” when SC2RB is read out.

If a start condition is fed and activation restarts during communication, the transmission data is invalid. Set the transmission data to SC2TB again to retransmit data.

SC2RB is rewritten every time when communication is completed. Data of SC2RB should be read out until the next reception is completed for continuous communication.

■ Setting Transfer Bit

The transfer bit count can be set from 1 bit to 8 bits. Set the SC2LNG2 to 0 flag of the SC2CTR0 register (at reset: 111) . The SC2LNG2 to 0 flags retain the previous value until a new value is set.

The SBT2 pin is masked inside serial interface to prevent operating errors by noise, except during communication. At slave communication, set data to SC2TB or input a start condition before feeding a clock to the SBT2 pin.

Wait more than 3.5 transfer clocks for feeding the external clock after the data set to SC2TB. Otherwise, normal communication is not guaranteed.

■ Setting Start Condition

Enable or disable of start condition can be selected with the SC2STE flag of the SC2CTR0 register.

Start condition is detected when the SC2CE1 flag of the SC2CTR0 register is set to “0” and data line SBI2 pin (3 channels) or SBO2 pin (2 channels) changes from “H” to “L” while the clock line (SBT2 pin) is “H”. It is also detected when the SC2CE1 flag of the SC2CTR0 register is set to “1”, and data line SBI2 pin (3 channels) or SBO2 pin (2 channels) changes from “H” to “L” while the clock line (SBT2 pin) is “L”.

Set the SC2SBOS flag and SC2SBIS flag of the SC2CTR1 register to “0” before change the start condition edge. Then, select “without start condition” when performing transmission and reception at the same time.
It may not be operated properly.

■ Setting First Transfer Bit

The SC2DIR flag of the SC2CTR0 register sets the first bit at transfer. LSB or MSB first can be selected.

■ Transmission Bit Count and First Transfer Bit

In transmission, when the transfer bit count is from 1 to 7 bits, the method for data storage to the transmission data buffer differs depending on the first transfer bit. When MSB is the first bit, store data to use the upper bits of SC2TB. As in Figure: 13.3.1, if data “A” to “F” is stored in bp2 to bp7of SC2RB when transfer bit count is 6, data is transferred from “F” to “A” in order. When LSB is the first bit , store data to use the lower bits of SC2TB. As in Figure: 13.3.2, if data “A to “F” are stored in bp0 to bp5 of SC2TB when the transfer bit is 6, data is transferred from “A” to “F” in order.

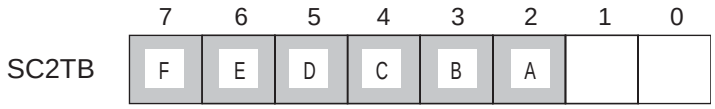


Figure:13.3.1 Transmission Bit Count and First Transfer Bit (MSB First)

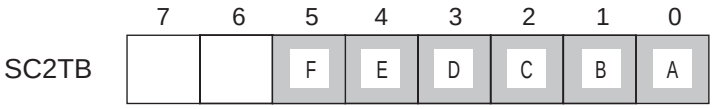


Figure:13.3.2 Transmission Bit Count and First Transfer Bit (LSB First)

■ Reception Bit Count and First Transfer Bit

In reception, when the transfer bit is from 1 to 7 bits, the method for data storage to the reception data buffer SC2RB differs depending on the first transfer bit. At MSB first, data is stored in the lower bits of SC2RB. When transfer bit count is 6, data “A” to “F” is stored in bp0 to bp5 of SC2RB, data is transferred from “F” to “A” in order as shown in Figure: 13.3.3. At LSB first, data is stored in the upper bits of SC2RB. When transfer bit count is 6, , if data “A” to “F” is stored in bp2 to bp7 of SC2RB, data is transferred from “A” to “F” in order as shown in Figure: 13.3.4.

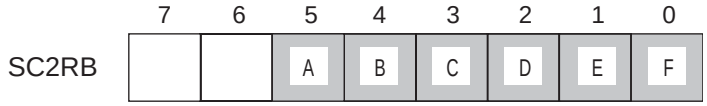


Figure:13.3.3 Reception Bit Count and First Transfer Bit (MSB First)

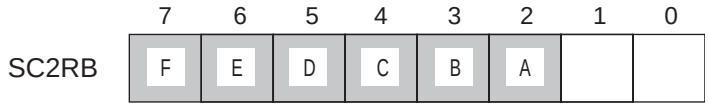
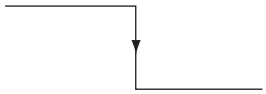
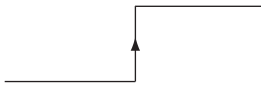
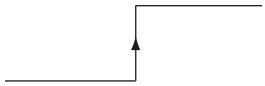
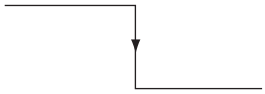


Figure:13.3.4 Reception Bit Count and First Transfer Bit (LSB First)

■ Setting Edge for Output/Input

The SC2CE1 flag of the SC2CTR0 register sets the edge of transmission data output and the edge of reception data input. Transmission data is output in synchronization with the falling edge of the clock when the SC2CE1 flag = “0” and with the rising edge of the clock when the SC2CE1=”1”. Reception data is fed in synchronization with the rising edge of the clock when the SC2CE1 flag =”0” and with the falling edge of the clock when the SC2CE1=”1”.

Table:13.3.2 Edge for Transmission Data Output/Reception Data Input

SC2CE1	Edge for transmission data output	Edge for reception data input
0		
1		

■ Setting Clock

A clock source is selected by the SC2PSC2 to 0 of the SC2CTR3 register and the SC2CKS1 to 0 of the SIFCLK register. The dedicated prescaler is started to operate with selecting “prescaler operation” by the SC2PSCE flag of the SC2CTR3 register. The SC2MST flag of the SC2CTR1 register selects an internal clock (clock master) or external clock (clock slave). When selecting an external clock, set an internal clock whose clock cycle does not exceed and is similar to an external clock’ by the SC2CKS register. The reason for this is that the interrupt flag SC2TIRQ is generated by the internal clock. Table: 13.3.3 shows the internal clock source which can be set with the SC2CKS register. Also, the internal clock can be set to 16 dividing further by the SC2CKM flag of the SC2CTR1 register.

Table:13.3.3 Synchronous Serial Interface Internal Clock Source

Clock source	Serial 2
Internal clock	1/2 of timer underflow
	1/4 of timer underflow
	1/16 of timer underflow
	1/64 of timer underflow
	IOCLK/2
	IOCLK/4

Set the SC2SBIS and SC2SBOS flags of the SC2CTR1 register to “0” before switching clock settings.

■ Setting Parity Check

No need for setting parity bit because it is not added.

■ Last Bit of Transmission Data

Table: 13.3.4 shows the last bit data output holding period at transmission and minimum data input period of the last bit at reception. At slave, an internal clock should be set to secure data holding time at data transmission.

Table:13.3.4 Last Bit Data Length of Data Transfer

	Last bit data holding period at transmission	Last bit data input period at reception
At master	1-bit data length	1 bit data length (min.)
At slave	[1-bit data length of external clock × 1/2] +[Internal clock cycle × (1/2 to 3/2)]	

When no start condition is specified (SC2STE flag = 0), the SBO2 output after the last bit data output holding period can be set with the SC2FDC1-0 flags of the SC2CTR3 register as shown in Table: 13.3.5.

After reset is released, the output prior to serial transfer is “H” regardless of the setting value of the SC2FDC1-0 flags. When a start condition is specified (SC2STE), “H” is output regardless of the setting value of the SC2FDC1 to 0.

Table:13.3.5 SBO2 Output After Last Bit Data Output Holding Period (without start condition)

SC2FDC1 flag	SC2FDC0 flag	SBO2 output after last bit data output holding period
0	0	Fixed to "1"(High) output
1	0	Fixed to "0"(Low) output
X	1	Last data retained

■ Setting Other Control Flags

The following flags need not be set or monitored because they are not used for clock synchronous communication.

Table:13.3.6 Other Control Flags

Register	Flag	Description
0SC2CTR2	SC2BRKE	Break status transmission control
	SC2BRKF	Break status reception monitor
	SC2NPE	Parity enable
	SC2PM1 to 0	Additional bit specification
	SC2FM1 to 0	Frame mode specification
SC2STR	SC2PEK	Parity error detection
	SC2FEF	Frame error detection

■ Setting Data I/O Pin

Communication modes have 2 types: 3 channels (clock pin (SBT2 pin), data output pin (SBO2 pin) and data input pin (SBI2 pin)) and 2 channels (clock pin SBT2 pin) and data I/O pin (SBO2 pin)). The SBO2 pin can be used only for serial data input. The SBI2 pin can be used for serial data input and output. The SC2IOM flag of the SC2CTR1 register can select whether serial data is fed from the SBI2 pin or SBO2 pin. When “data input from the SBO2 pin” is selected, 2-channel communication is used. In this case, the P17D flag of the P1DIR register controls the SBO2 pin direction and switches between transmission and reception. The SBI2 pin can be used as a general-purpose port because it not used at this time, .

In using synchornous serial interface, only GI5IR1 of the interrupt request flag becomes "1" whether the completion of the transmission or reception. GI5IR0 is not generated.

Maximum transfer speed should be under 5.0 MHz. If transfer clock exceeds 5.0 MHz, data may not be transferred properly.

In reception, the SBI2 pin can be used as a general-purpose port when the SC2IOM of the SC2CTR1 register is set to “1” and “serial data input from the SBO2 pin” is selected.

■ Reception Buffer Empty Flag Operation

After reception is completed, (communication complete interrupt SC2TIRQ), data is automatically stored from the reception shift register into SC2RB. If data is stored in the shift register SC2RB while the SC2SBIS flag of the SC2CTR1 register is set to “serial input” , the reception buffer empty flag SC2REMP of the SC2STR register is set to “1”. This indicates that reception data is ready to be read out. SC2REMP is cleared to “0” when data is read from SC2RB.

■ Transmission Buffer Empty Flag Operation

If data is set in SC2TB during communication (till the communication complete interrupt SC2TIRQ is generated after data is load into the transmission shift register), the transmission buffer empty flag SC2TEMP of the SC2TB register is set to “1”. This indicates that the next transmission data is ready to be loaded. When data is loaded into the internal shift register from SC2TB after SC2TIRQ is generated and when SC2TEMP is cleared to “0”, the next transfer is automatically started.

■ Reception BUSY Flag Operation

The BUSY flag SC2RBSY of the SC2STR register is set to “1” when data is set in SC2TB or when a start condition is recognized while “serial data input” is selected with the SC2SBIS flag of the SC2CTR1 register. The BUSY flag is cleared to “0” after generation of the communication end interrupt SC2TIRQ. The SC2RBSY flag setting is maintained during continuous communication. If the transmission buffer empty flag SC2TEMP is cleared to “0” when the communication complete interrupt SC2TIRQ is generated, SC2RBSY is cleared to “0”. The SC2RBSY flag is reset to “0” when the SC2SBIS flag is set to “0” during communication.

■ Transmission BUSY Flag Operation

The SC2TBSY flag of the SC2STR register is set if the SC2SBOS flag of the SC2CTR1 register is set to “1” when data is set in SC2TB or a when a start condition is recognized while “serial data output” is selected with the SC2SBOS flag of the SC2CTR1 register. The SC2TBSY flag is cleared to “0” after generation of the communication end interrupt SC2TIRQ. The SC2TBSY flag setting is maintained during continuous communication. If transmission buffer empty flag SC2TEMP is set to”0” when the communication complete interrupt SC2TIRQ is generated, SC2RBSY is cleared to “0”. The SC2TBSY flag is reset to “0” when the SC2SBOS flag is cleared to “0” during communication.

■ Overrun Error and Error Monitor Flag Operation

After reception is completed, if reception of the next data is completed before data is read from the reception data buffer SC2RB, overrun error occurs and the SC2ORE flag of the SC2STR register is set to “1”. At the same time, the error monitor flag SC2ERE is set, indicating that the reception has an error. The SC2ERE flag is cleared after the next communication complete interrupt SC2TIRQ is generated since data is read from SC2RB. The SC2ERE flag is cleared along with the SC2ORE flag . These error flags have no effects on communication.

■ Continuous Transmission

This serial is equipped with a continuous transmission function. If data is set in the transmission data buffer SC2TB during communication, the transmission buffer empty flag SC2TEMP is set; thus, allowing automatic, continuous communication. Set data to SC2TB the period that after data is loaded to the transmission shift register and before the communication end interrupt SC2IRQ is generated. In master communication, communication blank from SC2TIRQ generation to next transfer clock output is 4 transfer clock.

■ Forced Reset

This serial interface is equipped with a forced reset function to address abnormal operation. Communication can be shut down by setting both the SC2SBOS and SC2SBIS flags of the SC2CTR1 register to “0” (SBO2 pin function: port, input data: “1” input). When a force reset is done, the status registers (the SC2BRKF flag of the SC2CTR2 register, all flags of the SC2STR register) are initialized, but other control registers hold their set values.

■ Transmission Timing

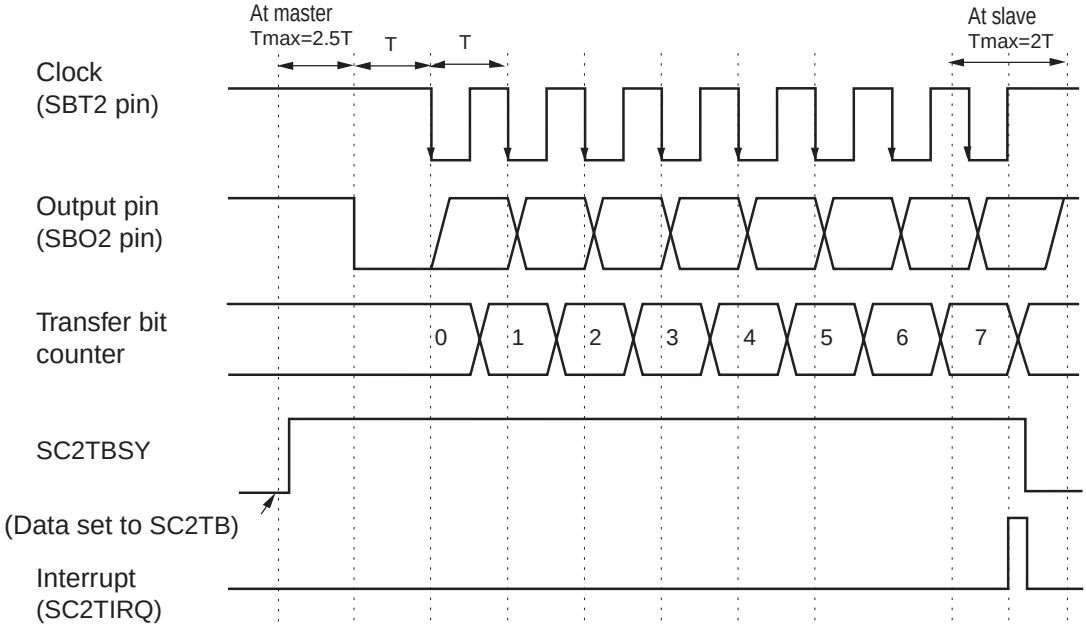


Figure:13.3.5 Transmission Timing (Falling Edge, With Start Condition)

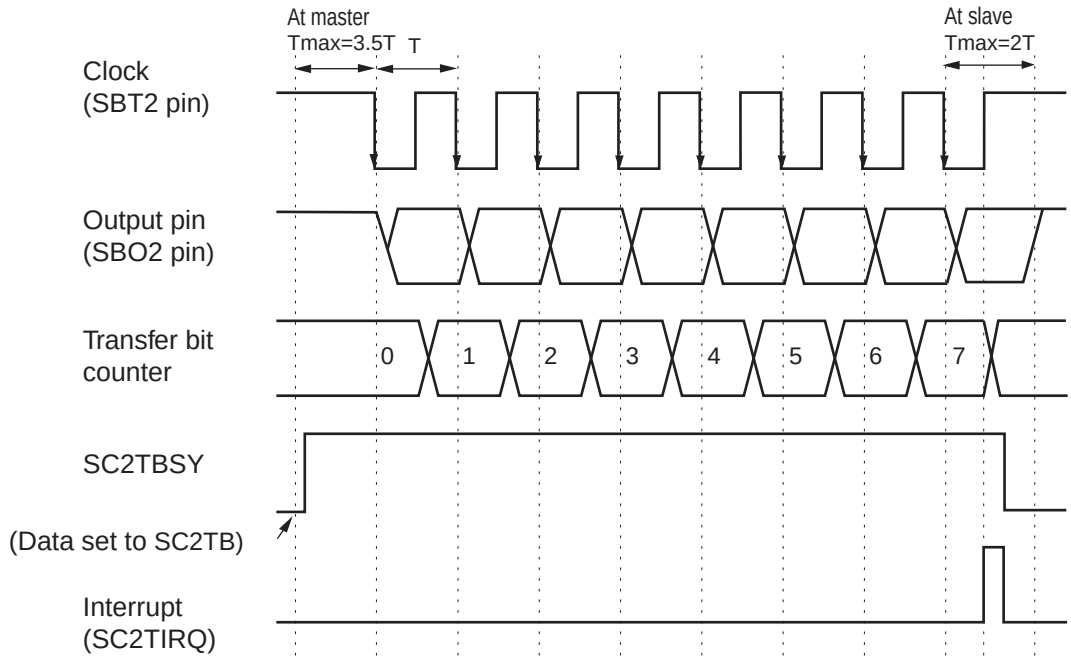


Figure:13.3.6 Transmission Timing (Falling Edge, Without Start Condition)

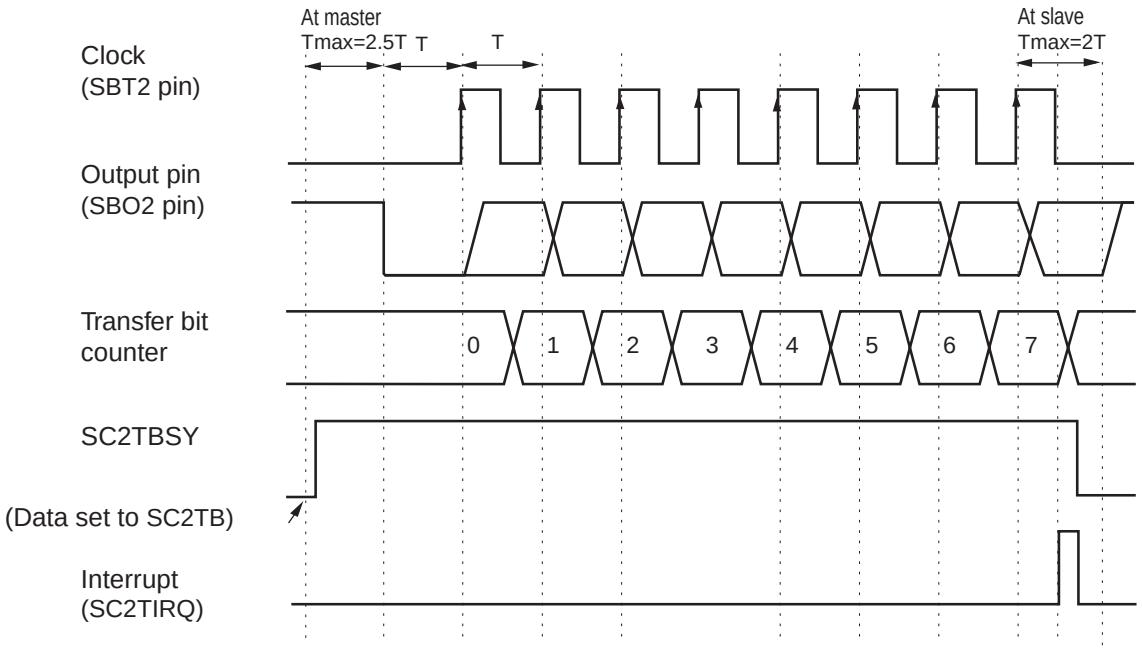


Figure:13.3.7 Transmission Timing (Rising Edge, With Start Condition)

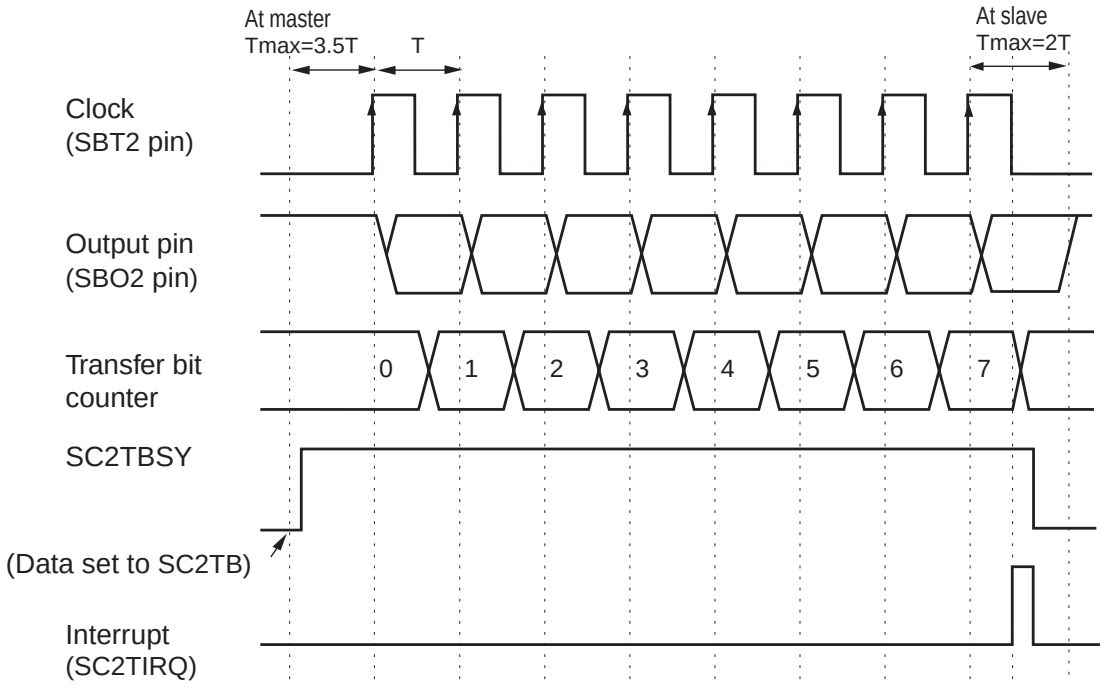


Figure:13.3.8 Transmission Timing (Rising Edge, Without Start Condition)

■ Reception Timing

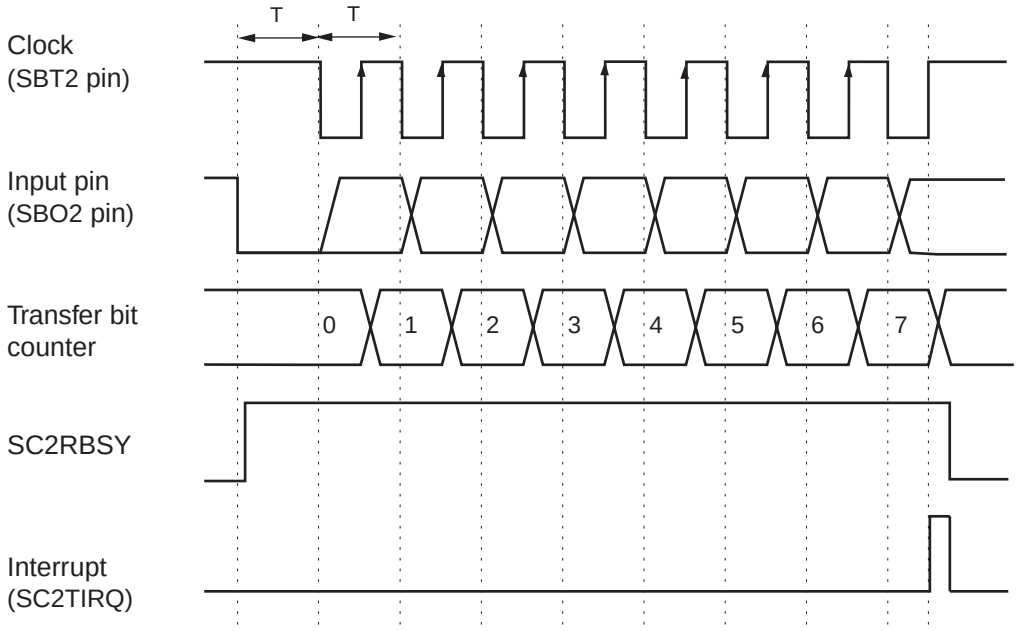


Figure:13.3.9 Reception Timing (Rising Edge, With Start Condition)

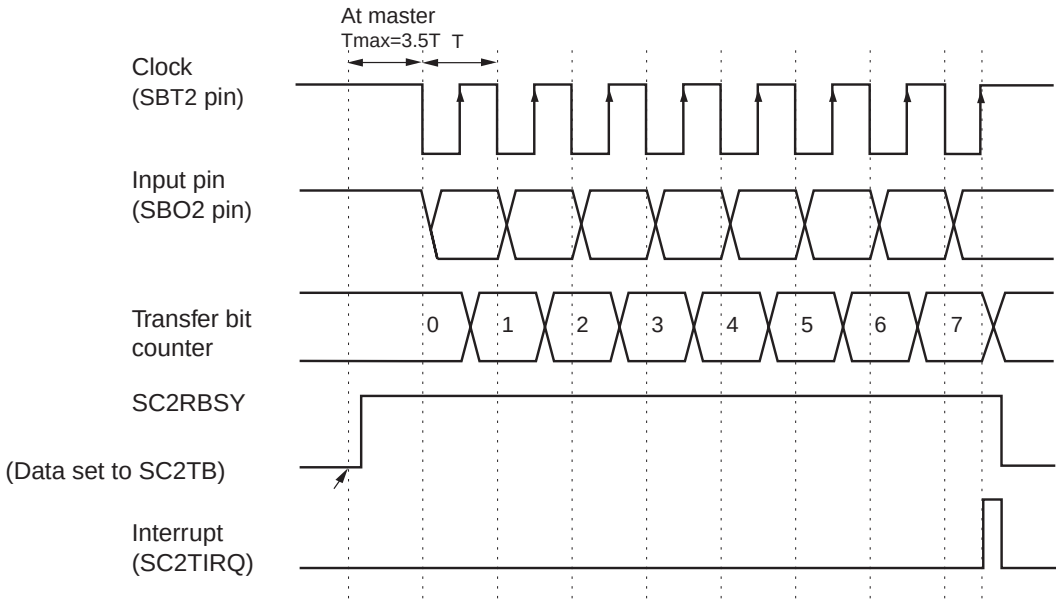


Figure:13.3.10 Reception Timing (Rising Edge, Without Start Condition)

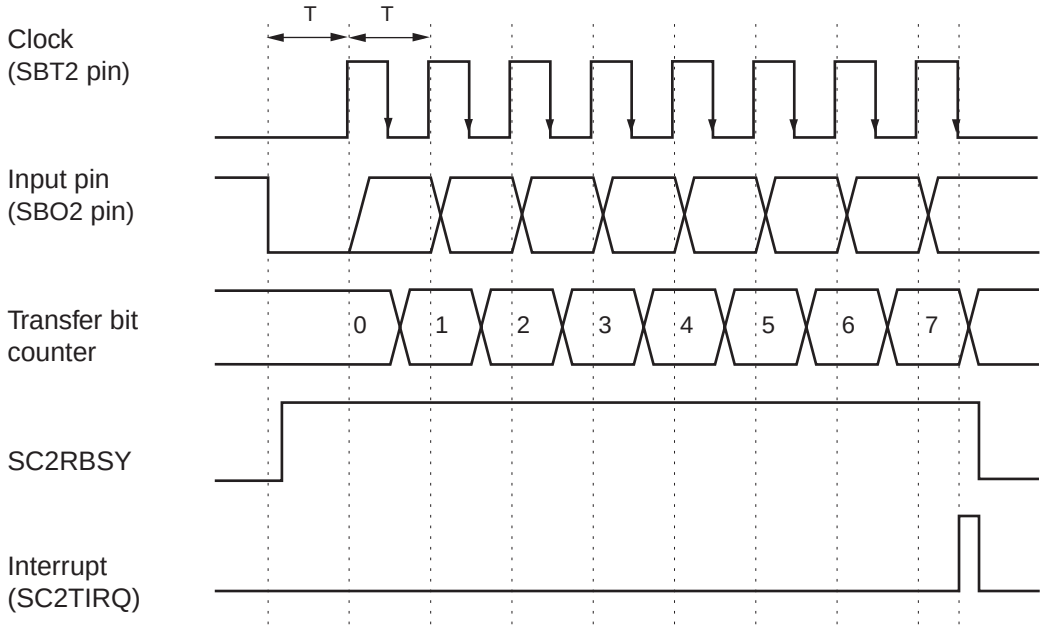


Figure:13.3.11 Reception Timing (Falling Edge, With Start Condition)

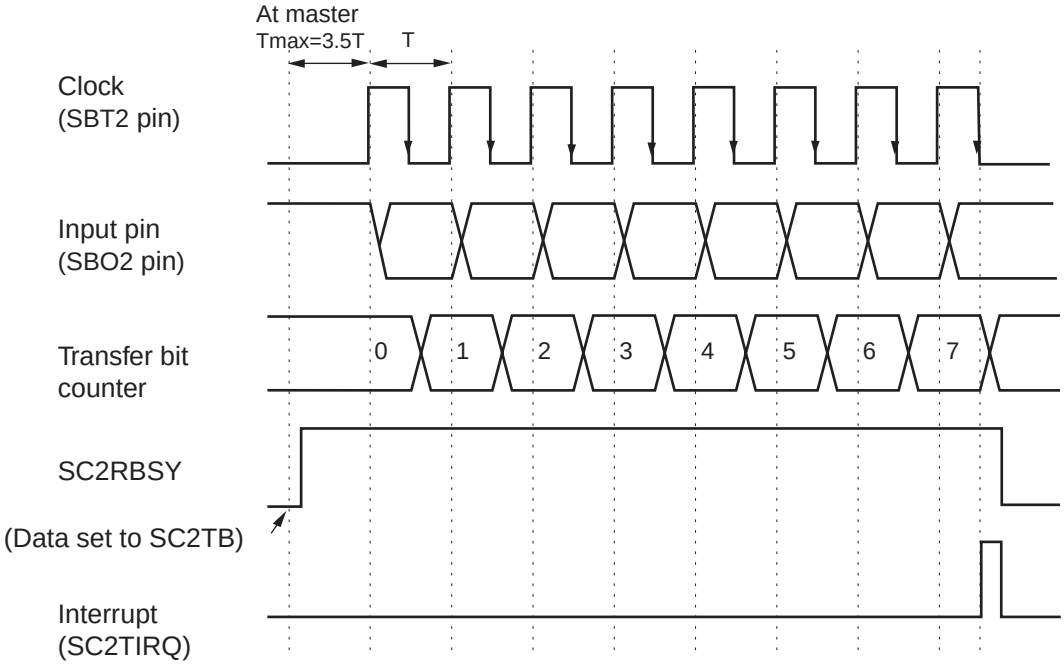


Figure:13.3.12 Reception Timing (Falling Edge, Without Start Condition)

■ Transmission and Reception

As data is received at the opposite edge of transmission data, set the polarity of the reception data input edge to the opposite of the transmission data output edge. Then, set to “without start condition” when performing transmission and reception at the same time. Failure to do so may cause improper communication.

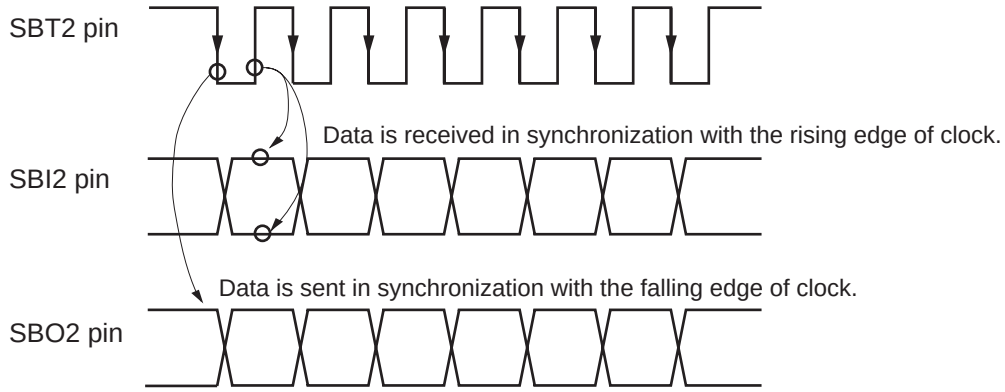


Figure:13.3.13 Transmission/Reception Timing (Reception: Rising Edge, Transmission: Falling Edge)

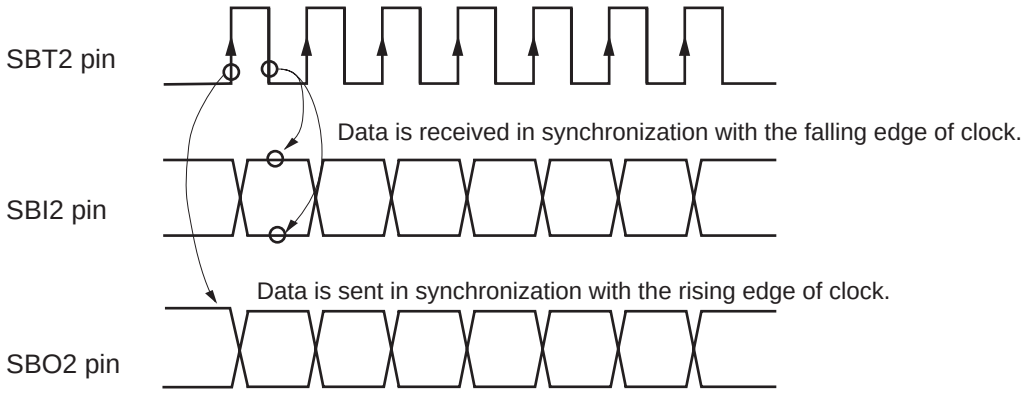


Figure:13.3.14 Transmission/Reception Timing (Reception: Falling Edge, Transmission: Rising Edge)

13.3.3 Setup Example

■ Transmission/Reception Setup Example

Here is the setup example for transmission/reception of clock synchronous communication with serial interface 2. Table: 13.3.7 shows the conditions for transmission/reception.

Table:13.3.7 Conditions of Synchronous Serial Interface Transmission/Reception

Setting item	Description
SBI2/SBO2 pin setting	Independent (3 channels)
Transfer bit count	8 bits
Start condition	Without start condition
First transfer bit	MSB
Input edge	Rising
Output edge	Falling
Clock	Clock master
Clock source	IOCLK/2
1/16 dividing of clock source	No 16 dividing
SBT2 pin pull-up resistor	Added
Serial interface 2 communication complete interrupt	Enabled
SBO2 output after last data output	Fixed to "1"(H)

Setup Procedure	Description
(1) Select the prescaler operation SC2CTR3(0x0000A125) bp3: SC2PSCE=1	(1) Set the SC2PSCE flag of the SC2CTR3 register to “1” to select the prescaler operation.
(2) Select the clock source SC2CTR3(0x0000A125) bp2-0: SC2PSC2-0=100	(2) Set the SC2PSC2-0 flags of the SC2CTR3 register to “100” to select IOCLK/2 to the clock source.
(3) SBO2 output control after last data output SC2CTR3(0x0000A125) bp7-6: SC2FDC1-0=00	(3) Set the SC2FDC1-0 flags of the SC2CTR3 register to “00” to select the “Fixed to “1” (High)” after the SBO last data output.
(4) Control the pin style P2PLU(0x0000A042) bp0: P20R=1	(4) Set the P20R flag of the P2PLU register and the P20R flag of the P2PLU register to “1” to select the pull-up resistor enabled.
(5) Control the pin direction P1DIR(0x0000A021) bp7: P17D=1 P2DIR(0x0000A022) bp1-0: P21D-P20D=01	(5) Set the P17D flag of the P1DIR register to “1” to set P17 (SBO2 pin) to the output pin. Set the P21D flag of the P2DIR register to “1” to set P21 (SBI2 pin) to the input pin, and set the P21D flag to “0” to set P20 (SBT2 pin) to the output pin,

Setup Procedure	Description
(6) Set the pin function P1MD(0x0000A031) bp7: P17M=1 P2MD(0x0000A032) bp0: P20M=1	(6) Set the P17M flag of the P1MD register to “1” to set the SBO2 pin function, the P20M flag of the P2MD register to “1” to set the SBT2 pin function.
(7) Set the SC2CTR0 register Set the transfer bit count SC2CTR0(0x0000A120) bp2-0: SC2LNG2-0=111 Select the start condition SC2CTR0(0x0000A120) bp3: SC2STE=0 Select the first transfer bit SC2CTR0(0x0000A120) bp4: SC2DIR=0 Select the transfer edge SC2CTR0(0x0000A120) bp7: SC2CE1=0	(7) Set the SC2LNG2-0 flag of the SC2CTR0 register to “111” to set the transfer bit count to 8 bits. Set the SC2STE flag of the SC2CTR0 register to “0” and select “Without start condition”. Set the SC2DIR flag of the SC2CTR0 register to “0” to set the first transfer bit to MSB. Set the SC2CE1 flag of the SC2CTR0 register to “0” to set the transmission data output edge to “falling” and the reception data input edge to “rising”.
(8) Set the SC2CTR1 register Select the communication style SC2CTR1(0x0000A121) bp0: SC2CMD=0 Select the transfer clock SC2CTR1(0x0000A121) bp2: SC2MST=1 bp3: SC2CKM=0 Control the pin function SC2CTR1(0x0000A121) bp4: SC2SBOS=1 bp5: SC2SBIS=1 bp6: SC2SBTS=1 bp7: SC2IOM=0	(8) Set the SC2CMD flag of the SC2CTR1 register to “0” and select the synchronous serial. Set the SC2MST flag of the SC2CTR1 register to “1” and select the clock master (internal clock). Set the SC2CKM flag to “0” and select “ no 1/16 dividing of the clock source. Set the SC2SBOS, SC2SBIS, and SC2SBTS flags of the SC2CTR1 register to “1” to set the SBO2 pin to the serial data output and the SBT2 pin to the serial I/O pin. Set the SBI2 pin to the serial data input by setting the SC2IOM flag to “0”.
(9) Set the interrupt level G15ICR(0x0000893C) bp14-12: G15LV2-0=100	(9) Set the interrupt level by the G15LV2-0 flags of the G15ICR register.
(10) Enable the interrupt G15ICR(0x0000893C) bp9: G15IE1=1	(10) Set the G15IE1 flag of the G15ICR register to “1” to enable the interrupt. If the interrupt request flag (G15IR1 of the G15ICR register) is already set, clear the G15IR1 flag to enable the interrupt.
(11) Start the serial transmission Transmission data→SC2TB(0x0000A130) Reception data→input to the SBI2 pin	(11) set the transmission data to the serial interface 2 transmission data buffer (SC2TB). The transfer clock is generated and transmission and reception are started. When transmission is completed, the serial interface 2 interrupt SC2TIRQ is generated.

Note: Each in (1) to (3), (7), and (8) can be set at the same time.

13.3.4 UART Serial Interface

Serial interface 2 is capable of duplex UART communication. Table: 13.3.8 shows UART serial interface functions.

Table:13.3.8 UART Serial Interface Functions

Communication style	UART (duplex)
Interrupt	SC2TIRQ (transmission), SC2RIRQ (reception)
Pin	SBO2 (I/O) SBI2 (input)
First transfer bit specification	MSB/LSB first
Parity bit selection	O
Parity bit control	0 parity 1 parity Even parity Odd parity
Frame selection	7 data bits +1STOP 7 data bits +2STOP 8 data bits +1STOP 8 data bits+2STOP
Continuous operation	O
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

■ Activation Factor for Communication

At transmission, if data is set in the transmission data buffer SC2TB, a start condition is generated to start transfer. At reception, reception is started by receiving a start bit. In reception, when the data length of "L" for input data is equal to or longer than 0.5 bit, that is recognized as a start bit.

■ Transmission

Data transmission is automatically started when data is set in the transmission data buffer SC2TB. When transmission is completed, the serial 1 transmission interrupt SC2TIRQ is generated.

■ Reception

When a start bit is recognized, reception is started after the transfer bit counter that counts transfer bit is cleared. The serial interface 2 interrupt SC2RIRQ is generated when the reception is completed.

■ Duplex Communication

In duplex communication, transmission and reception can be performed independently at the same time. In this case, the frame mode and parity bit polarity of data on transmission/reception must be the same.

■ Transmission Data Buffer

Refer to: XIII-11

■ Reception Data Buffer

Refer to: XIII-12

■ Setting Transfer Bit Count

Transfer bit count is set automatically when a frame mode is specified with the SC2FM1-0 flags of the SC2CTR2 register. When the SC2CMD flag of the SC2CTR1 register is set to “1” and UART communication is selected , the setting in the synchronous serial transfer bit count selection flag SC2LNG2-0 f the SC2CTR0 register becomes invalid.

■ Setting First Transfer Bit

Refer to :XIII-12

■ Transmission Bit Count and First Transfer BIt

Refer to : XIII-13

■ Reception Bit Count and First Transfer BIt

In reception, when transfer bit count is 7, the data storing method to the reception data buffer SC2RB is different depending on start transfer bit specification . When “MSB first” is selected, data is stored in lower bits of SC2RB. When transfer bit count is 7, data “A” to “G” are stored in bp 7 to 1 of SC2RB from “A” to “G” in order as shown in Figure: 13.3.15. When “LSB first” is selected, data is stored in upper bits of SC2RB. When transfer bit count is 7, data “A” to ”G” are stored in bp 6 to 0 of SC2RB from “A” to “G” in order as shown in Figure: 13.3.16.

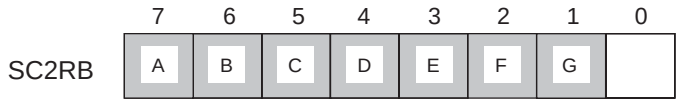


Figure:13.3.15 Reception Bit Count and First Transfer BIt (MSB first)

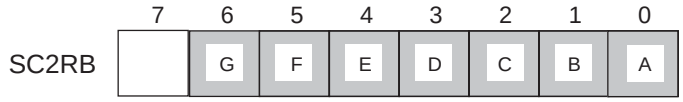


Figure:13.3.16 Reception Bit Count and First Transfer BIt (LSB first)

■ Setting Frame Mode and Parity Check

Figure: 13.3.17 shows the data format at UART communication.

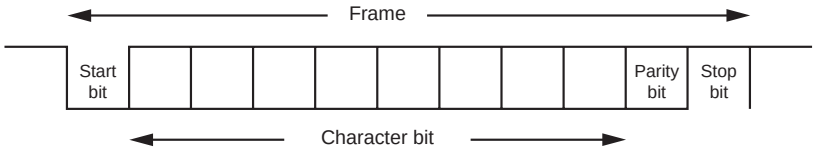


Figure:13.3.17 UART Serial Interface Transmission/Reception Data Format

Transmission/reception data contain start bit, character bit, parity bit, and stop bit. Table: 13.3.9 shows the types to be set.

Table:13.3.9 Types of UART Serial Interface Transmission/Reception Data

Start bit	1 bit
Character bit	7,8 bits
Parity bit	Fixed to 0, fixed to 1, even, odd, none
Stop bit	1,2 bits

The SC2FM1-0 flags of the SC2CTR2 register is used to specify a frame mode. Table: 13.3.10 shows available frame mode types. When the SC2CMD flag of the SC2CTR1 register is set to “1” and UART communication is selected. the transfer bit count in the SC2LMG2-0 flags of the SC2CTR0 register becomes invalid.

Table:13.3.10 Types of UART Serial Interface Transmission/Reception Data

SC2CTR2 register		Frame mode type
SC2FM1	SC2FM0	
0	0	7 character bits + 1 stop bit
0	1	7 character bits + 2 stop bit
1	0	8 character bits + 1 stop bit
1	1	8 character bits + 2 stop bit

Parity bit is used to detect bit errors in transmission/reception data. Table: 13.3.11 shows parity bit types. The SC2NPE and the SC2PM1-0 flags of the SC2CTR2 register are used to specify parity bit.

Table:13.3.11 Parity Bit Types of UART Serial Interface

SC2CTR2			Parity bit type	Description
SC2NPE	SC2PM1	SC2PM0		
0	0	0	Fixed to 0	Parity bit is set to “0”.
0	0	1	Fixed to 1	Parity bit is set to “1”.
0	1	0	Odd parity	Control that the total of “1” of character bit and parity bit should be odd
0	1	1	Even parity	Control that the total of “1” of character bit and parity bit should be even
1	-	-	None	No parity bit is added.

■ Setting Data I/O PIn

Communication modes can be selected from 2 channels (data output pin (SBO2 pin) and data input pin (SBI2 pin)), or 1 channel (data I/O pin (SBO2 pin)). The SBI2 pin can be used only for serial data input. The SBI2 pin can be used for both serial data input and output. The SC2IOM flag of the SC2CTR1 register can select whether serial data is fed from the SBI2 pin or SBO2 pin. When “data input from the SBO2 pin” is selected, 1-channel communication mode is used; so, the P17D flag of the P1DIR register controls the SBO2 pin direction for switching between transmission and reception. At this time, the SBI2 pin can be used as a general-purpose port since it is not used.

■ Reception Buffer Empty Flag Operation

When the reception complete interrupt SC2RIRQ is generated, data is automatically stored from the reception shift register to SC2RB. If data is stored in the shift register SC2RB, the reception buffer empty flag SC2REMP of the SC2STR register is set to “1”. This indicates that reception data is ready to be read out. SC2REMP is cleared to “0” when data is read from SC2RB.

■ Transmission Buffer Empty Flag Operation

If data is set in SC2TB during communication (till the communication complete interrupt SC2TIRQ is generated after data is load into the transmission shift register), the transmission buffer empty flag SC2TEMP of the SC2TB register is set to “1”. This indicates that the next transmission data is ready to be loaded. When data is loaded into the internal shift register from SC2TB after SC2TIRQ is generated and when SC2TEMP is cleared to “0”, the next transfer is automatically started.

■ Reception BUSY Flag Operation

The SC2RBSY flag of the SC2STR register is set to “1” when a start bit is recognized. The flag is cleared to “0” after generation of the reception complete interrupt SC2RIRQ. The SC2RBSY flag is reset to “0” when the SC2SBIS flag is set to “0” during reception.

■ Transmission BUSY Flag Operation

The SC2TBSY flag of the SC2STR register is set to “1” when data is set in SC2TB. The flag is cleared to “0” after generation of the transmission complete interrupt SC2TIRQ. SC2TBSY flag setup is maintained during continuous communication. If the transmission buffer empty flag SC2TEMP is set to”0” when the transmission complete interrupt SC2TIRQ is generated, SC2TBSY is cleared to “0”. The SC2TBSY flag is reset to “0” when the SC2SBIS flag is set to “0” during transmission.

■ Setting Break Status Transmission Control

Break status can be transmitted by the SC2BRKE flag of the SC2CTR2 register. When SC2BRKE is set to “1” to select break transmission, all from the start to stop bits transmit “0” .

■ Break Status Reception Judgement

Reception at bread status can be judged. If all received data from the start bit to stop bit are “0”, the SC2BRKF flag of the SC2CTR2 register is set and regards the break status. The SC2BRKF flag is set when the reception complete interrupt SC2RIRQ is generated.

■ Reception Error

Reception errors can be classified under 3 types, overrun error, parity error and framing error. Reception error can be determined by checking the SC2ORE, SC2PEK and SC2FEF flags of the SC2STR register. If an error is found from any of these flags, the SC2ERE flag of the SC2STR register is set to “1”. The SC2PEK and SC2FEF flags of the reception error flags are updated when the communication complete interrupt SC2RIRQ is generated. The SC2ORE flag is cleared upon generation of the next communication complete interrupt SC2RIRQ after data is read from SC2RB. Check the reception error flags before the next communication is completed. These error flags do not affect communication. Table: 13.3.12 shows reception errors causes.

Table:13.3.12 Cause of UART Serial Interface Reception Errors

Flag	Reception error type		
SC2ORE	Overrun error	Next data is received before reception buffer is read.	
SC2PEK	Parity error	Fixed to 0	When parity bit is “1”
		Fixed to 1	When parity bit is “0”
		Odd parity	When the total of “1” of character bit and parity bit is even
		Even parity	When the total of “1” of character bit and parity bit is odd
SC2FEF	Framing error	Stop bit is not detected.	

■ Continuous Communication

This serial interface has a continuous communication function. If data is set in the transmission data buffer SC2TB during transmission, the transmission buffer empty flag SC2TEMP is set, thus allowing automatic, continuous communication. In this case, there is no communication blank. Set the next data to SC2TB until the transmission complete interrupt SC2TIRQ is generated since previous data is set.

■ Force Reset

Refer to: XIII-17

■ Transmission Timing

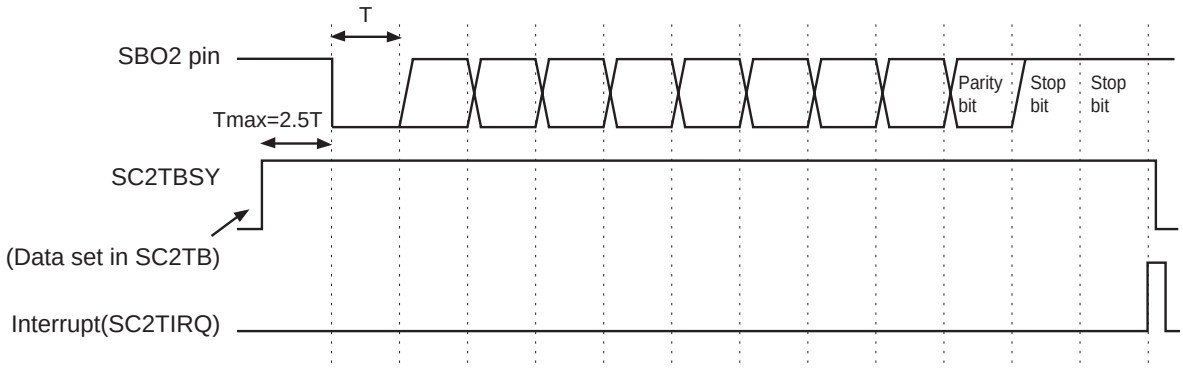


Figure:13.3.18 Transmission Timing (With Parity bit)

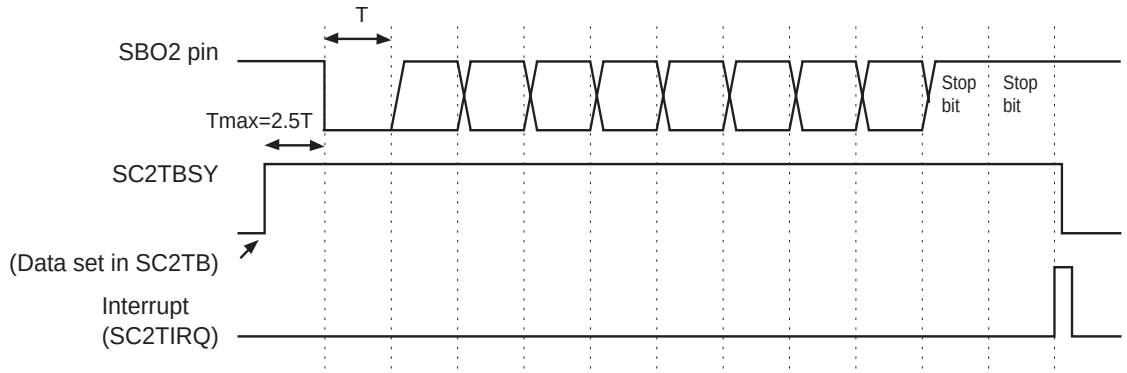


Figure:13.3.19 Transmission Timing (Without Parity bit)

■ Reception Timing

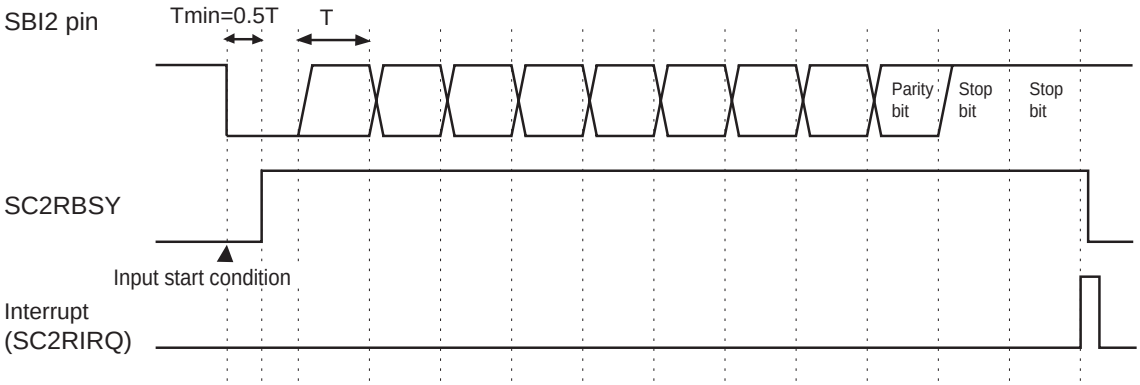


Figure:13.3.20 Reception Timing (With Parity bit)

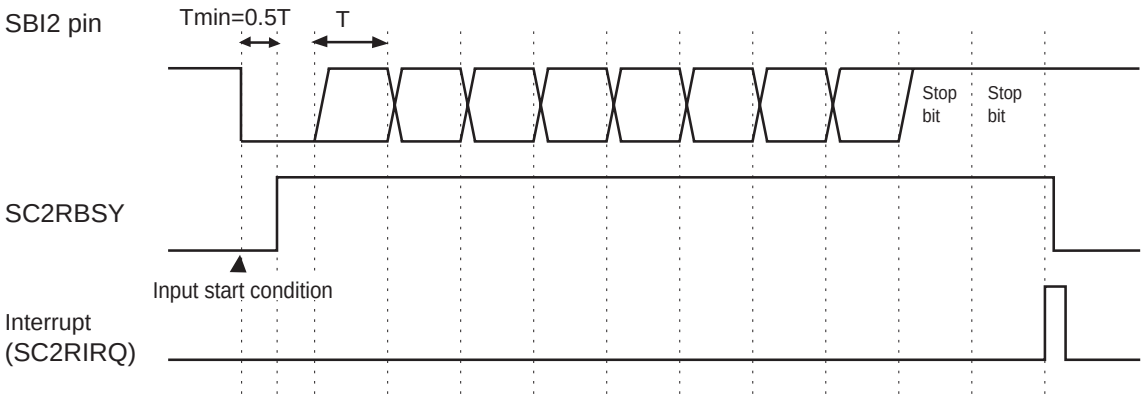


Figure:13.3.21 Reception Timing (Without Parity bit)

■ Setting Transfer Speed

Baud rate timers (timer 14, timer 15 and timer 16) can set any transfer rate. Table: 13.3.13 shows an example of setting transfer speed.

Table:13.3.13 Register for Setting UART Serial Interface Transfer Speed

Description	Register	Page
Serial clock source setting (Division ratio setting)	SC2CTR3	XIII-9
Timer selection	SIFCLK	XII-10

The value of the timer base register can be set as follows:

Underflow cycle = (Base register set value + 1) × timer clock cycle

Baud rate = 1/ (Underflow cycle × Dividing ratio of serial clock source)

From the above,

Base register set value = Timer clock frequency/(Baud rate × Dividing ratio of serial clock source) - 1

For example, if the desired baud rate is 300 bps at 64 dividing of serial clock source when the timer clock source is IOCLK/32 (input frequency = 10 MHz, 6 multiplication and IOCLK = MCLK/2) the set value can be determined as follows:

Base register set value = $(10 \times 10^6/32) / (300 \times 64) -1$

=48

=x’30

The following table shows the clock source at standard transfer rate and the set value of the compare register at MCLK=60 MHz (IOCLK=MCLK/2).

Transfer rate should be selected under 300 kbps.

Table:13.3.14 Set value of Transfer Speed (Base Register value: hexadecimal)

Serial clock source timer underflow/n		32				64				256				1024			
Timer clock source IOCLK/n		1	8	32	128	1	8	32	128	1	8	32	128	1	8	32	128
Transfer speed (bps)	300	C34	186	61	17	61A	C2	30	B	186	30	B	2	61	B	2	-
	960	3D0	79	1E	7	1E7	3C	E	3	79	E	3	-	1E	3	-	-
	1200	30C	61	17	5	186	30	B	2	61	B	2	-	17	2	-	-
	2400	186	30	B	2	C2	17	5	-	30	5	-	-	B	-	-	-
	4800	C2	17	5	-	61	B	2	-	17	2	-	-	5	-	-	-
	9600	61	B	2	-	30	5	-	-	B	-	-	-	2	-	-	-
	19200	30	5	-	-	17	2	-	-	5	-	-	-	-	-	-	-
	28800	20	3	-	-	F	-	-	-	3	-	-	-	-	-	-	-
	38400	17	2	-	-	B	-	-	-	2	-	-	-	-	-	-	-
	76800	B	-	-	-	5	-	-	-	-	-	-	-	-	-	-	-

13.3.5 Setup Example

■ UART Serial Interface Setup Example

The setup example of UART transmission/reception with serial interface 2 is shown. Table: 13.3.14 shows the conditions for transmission/reception.

Table:13.3.15 Condition of UART Interface Transmission/Reception

Setting item	Description
SBI2/SBO2 pin setting	Independent (2 channels)
Frame mode specification	8 bit + 2 stop bits
First transfer bit	MSB
Clock source	Timer 14
Parity bit add/check	"0" added/check
Serial 2 transmission complete interrupt	Enabled
Serial 2 reception complete interrupt	Enabled

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the baud rate timer	(1) Set the baud rate by the TM14MD and TM14BR registers and set the TM4EN flag to “1” to operate the timer 14.
(2) Select the baud rate timer SIFCLK(0x0000A10E) bp5-4: SC2CKS2-1=00	(2) Set the SC2CKS2-1 flags of the SIFCLK register to “00” to set the timer 14 underflow to the baud rate timer.
(3) Select the clock source SC2CTR3(0x0000A125) bp2-0: SC2PSC2-0=000	(3) Set the SC2PSC2-0 flags of the SC2CTR3 register to “000” to select 1/32 of timer underflow.
(4) Set the pin function P1MD(0x0000A031) bp7: P17M=1	(4) Set the P17M flag of the P1MD register to “1” to set it to the SBO2 pin function.
(5) Control the pin direction P1DIR(0x0000A021) bp7: P17D=1 P2DIR(0x0000A022) bp1: P21D=0	(5) Set the P17D flag of the P1DIR register to “1” to set P17(SBO2 pin) to the output pin; and set the P21D flag of the P2DIR register to “0” to set P21(SBI2) to the input pin.
(6) Set the SC2CTR0 register Select the start condition SC2CTR0(0x0000A120) bp3: SC2STE=1 Select the first transfer bit SC2CTR0(0x0000A120) bp4: SC2DIR=0	(6) Set the SC2STE flag of the SC2CTR0 register to “1” and select “With start condition”. Set the SC2DIR flag of the SC2CTR0 register to “0” to set the first transfer bit to MSB.

Setup Procedure	Description
(7) Set the SC2CTR2 register Control the output data SC2CTR2(0x0000A124) bp0: SC2BRKE=0 Select the added parity bit SC2CTR2(0x0000A124) bp3: SC2NPE=0 bp5-4: SC2PM1-0=00 Specify the frame mode SC2CTR2(0x0000A124) bp7-6: SC2FM1-0=11	(7) Set the SC2BRKE flag of the SC2CTR2 register to “0” to select the serial data transmission. Set the SC2PM1-0 flags of the SC2CTR2 register to “00” to select 0 parity and the SC2NPE flag to “0” to enable the parity bit added. Set the SC2FM1-0 flags of the SC2CTR2 register to “11” to select 8 bits + 2 stop bits to the frame mode.
(8) Set the SC2CTR1 register Set the communication style SC2CTR1(0x0000A121) bp0: SC2CMD=1 Select the clock dividing SC2CTR1(0x0000A121) bp3: SC2CKM=1 bp2: SC2MST=1 Control the pin function SC2CTR1(0x0000A121) bp4: SC2SBOS=1 bp5: SC2SBIS=1 bp7: SC2IOM=0	(8) Set the SC2CMD flag of the SC2CTR1 register to “1” to select duplex UART. Set the SC2CKM flag of the SC2CTR1 register to “1” to select 16 dividing of source clock. Be sure to set the SC2MST flag to “1” and select the clock timer. Set the SC2SBOS and SC2SBIS flags of the SC2CTR1 register to “1” to set the SBO2 pin to the serial data output and the SBI2 pin to the serial data input.
(9) Set the interrupt level G15ICR(0x0000893C) bp14-12: G15LV2-0=100	(9) Set the interrupt level by the G15LV2-0 flags of the G15ICR register.
(10) Enable the interrupt G15ICR(0x0000893C) bp8: G15IE0=1 bp9: G15IE1=1	(10) Set the G15IE0 flag of the G15ICR register to “1” and the G15IE1 flag to “1” to enable the interrupt. When the interrupt request flag is already set, clear the request flag.
(11) Start the serial transmission Transmission data→SC2TB(0x0000A130) Reception data→input to SBI2 pin	(11) If transmission data is set to the serial interface 2 transmission data buffer (SC2TB), transmission is started. When transmission is completed, the serial 2 transmission interrupt (SC2TIRQ) is generated. Also, reception data is fed to the SBI2 pin; and, the serial 2 reception interrupt (SC2RIRQ) is generated.

Note: Each in (6), (7), and (8) can be set at once.

Chapter 14 A/D Converter

14

14.1 Overview

This LSI has an A/D converter with 10 bit resolutions and up to 16-channel analog signals can be processed with 3 converters. It contains a built-in sample hold circuit. 6 types of conversion reference clocks can be switched by software.

14.1.1 Functions

Table: 14.1.1 shows the A/D converter functions.

Table:14.1.1 A/D Converter Functions

	AD0	AD1	AD2	Page
Interrupt cause	AD0IRQ, AD0IRQB	AD1IRQ, AD1IRQB	AD2IRQ	-
Numbers of analog input pins	Max. 6 pins	Max. 8 pins	Max. 10 pins	-
Resolution\	10 bits			-
A/D converter clock selection	IOCLK $\times$ 1 IOCLK $\times$ 2 IOCLK $\times$ 3 IOCLK $\times$ 4 IOCLK $\times$ 8 IOCLK $\times$ 16			-
Sampling/hold time	1 cycle 2 cycles 4 cycles 6 cycles			XIV-28
Conversion time	Set to over 1.0 μs			-
Input range	V_{SS} to V_{DD}			-
Operation mode	6 types	6 types	22 types	XIV-28
Conversion start trigger	Register set by instruction PWM0 underflow PWM0 overflow PWM1 underflow PWM1 overflow Timer 12 compare A Timer 12 compare B Timer 13 compare A Timer 13 compare B	Register set by instruction PWM0 underflow PWM0 overflow PWM1 underflow PWM1 overflow Timer 12 compare A Timer 12 compare B Timer 13 compare A Timer 13 compare B	Register set by instruction PWM0 underflow PWM0 overflow PWM1 underflow PWM1 overflow Timer 12 compare A Timer 12 compare B Timer 13 compare A Timer 13 compare B	XIV-28

14.1.2 Configuration

■ A/D Converter Configuration

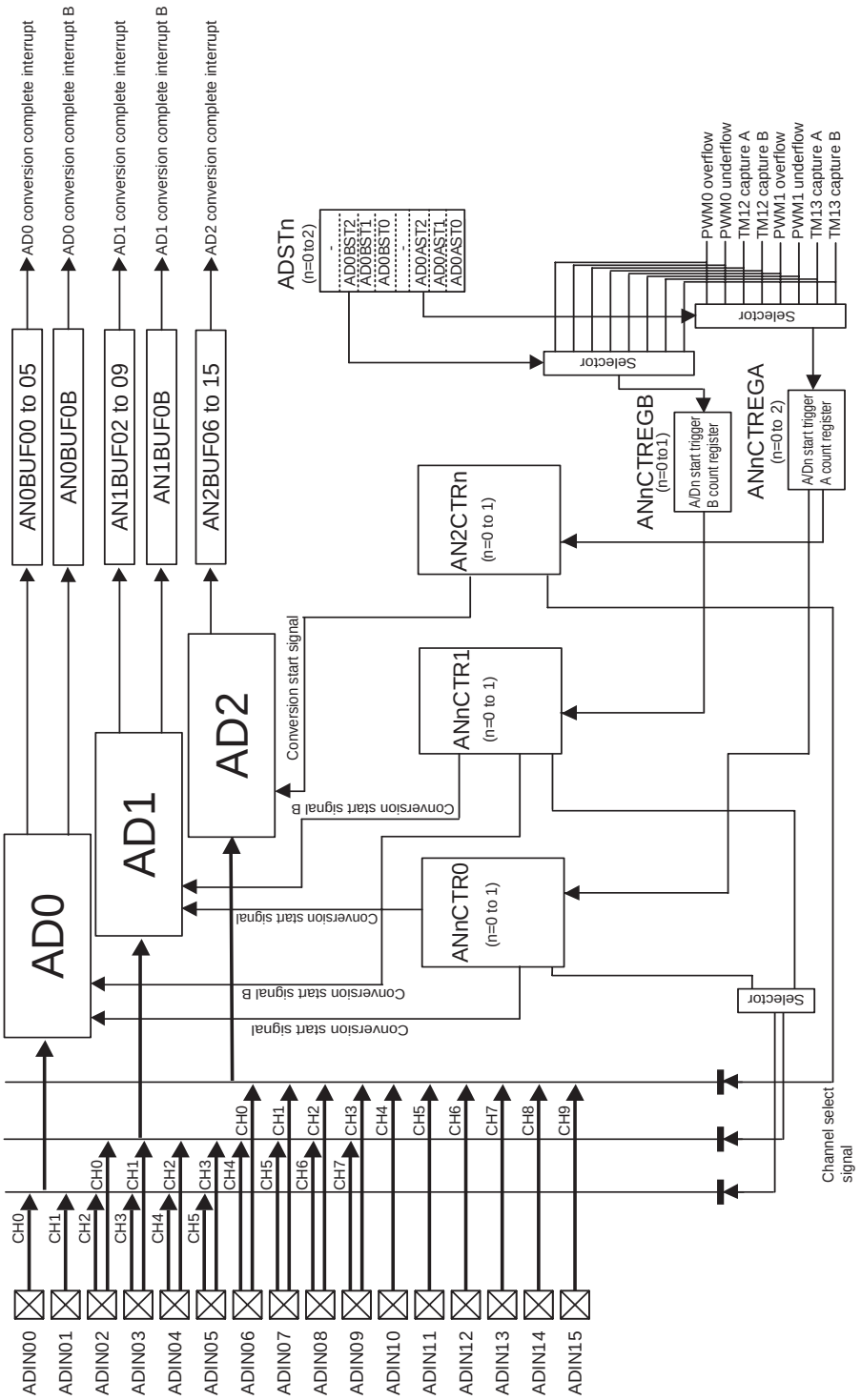


Figure:14.1.1 A/D Converter Configuration

14.2 Control Registers

A/D converter consists of the conversion control register, conversion data buffer and start selection register.

14.2.1 Registers

Table: 14.2.1 shows the registers used to control A/D converter.

Table:14.2.1 A/D Converter Control Registers

	Register	Address	R/W	Access size	Function	Page
AD0	AN0CTR0	0x0000A400	R/W	8,16	A/D0 conversion control register 0	XIV-6
	AN0CTR1	0x0000A404	R/W	8,16	A/D0 conversion control register 1	XIV-9
	ADST0	0x0000A408	R/W	8	A/D0 start trigger selection register	XIV-12
	AN0CTREGA	0x0000A40C	R/W	8	A/D0 start trigger A count register	XIV-14
	AN0CTREGB	0x0000A40D	R/W	8	A/D0 start trigger B count register	XIV-14
	AN0BUF00	0x0000A410	R	16	A/D0 conversion data buffer 00	XIV-17
	AN0BUF01	0x0000A414	R	16	A/D0 conversion data buffer 01	XIV-17
	AN0BUF02	0x0000A418	R	16	A/D0 conversion data buffer 02	XIV-17
	AN0BUF03	0x0000A41C	R	16	A/D0 conversion data buffer 03	XIV-18
	AN0BUF04	0x0000A420	R	16	A/D0 conversion data buffer 04	XIV-18
	AN0BUF05	0x0000A424	R	16	A/D0 conversion data buffer 05	XIV-18
	AN0BUF0B	0x0000A430	R	16	A/D0 conversion data buffer 0B	XIV-19
AD1	AN1CTR0	0x0000A440	R/W	8,16	A/D1 conversion control register 0	XIV-7
	AN1CTR1	0x0000A444	R/W	8,16	A/D1 conversion control register 1	XIV-10
	ADST1	0x0000A448	R/W	8	A/D1 start trigger selection register	XIV-13
	AN1CTREGA	0x0000A44C	R/W	8	A/D1 start trigger A count register	XIV-15
	AN1CTREGB	0x0000A44D	R/W	8	A/D1 start trigger B count register	XIV-15
	AN1BUF02	0x0000A450	R	16	A/D1 conversion data buffer 02	XIV-20
	AN1BUF03	0x0000A454	R	16	A/D1 conversion data buffer 03	XIV-20
	AN1BUF04	0x0000A458	R	16	A/D1 conversion data buffer 04	XIV-20
	AN1BUF05	0x0000A45C	R	16	A/D1 conversion data buffer 05	XIV-21
	AN1BUF06	0x0000A460	R	16	A/D1 conversion data buffer 06	XIV-21
	AN1BUF07	0x0000A464	R	16	A/D1 conversion data buffer 07	XIV-21
	AN1BUF08	0x0000A468	R	16	A/D1 conversion data buffer 08	XIV-22
	AN1BUF09	0x0000A46C	R	16	A/D1 conversion data buffer 09	XIV-22
	AN1BUF0B	0x0000A470	R	16	A/D1 conversion data buffer 0B	XIV-22

	Register	Address	R/W	Access size	Function	Page
AD2	AN2CTR0	0x0000A480	R/W	8,16	A/D2 conversion control register 0	XIV-8
	AN2CTR1	0x0000A484	R/W	8,16	A/D2 conversion control register1	XIV-11
	ADST2	0x0000A488	R/W	8	A/D2 start trigger selection register	XIV-13
	AN2CTREGA	0x0000A48C	R/W	8	A/D2 start trigger count register	XIV-16
	AN2BUF06	0x0000A490	R	16	A/D2 conversion data buffer 06	XIV-23
	AN2BUF07	0x0000A494	R	16	A/D2 conversion data buffer 07	XIV-23
	AN2BUF08	0x0000A498	R	16	A/D2 conversion data buffer 08	XIV-23
	AN2BUF09	0x0000A49C	R	16	A/D2 conversion data buffer 09	XIV-24
	AN2BUF10	0x0000A4A0	R	16	A/D2 conversion data buffer 10	XIV-24
	AN2BUF11	0x0000A4A4	R	16	A/D2 conversion data buffer 11	XIV-24
	AN2BUF12	0x0000A4A8	R	16	A/D2 conversion data buffer 12	XIV-25
	AN2BUF13	0x0000A4AC	R	16	A/D2 conversion data buffer 13	XIV-25
	AN2BUF14	0x0000A4B0	R	16	A/D2 conversion data buffer 14	XIV-25
	AN2BUF15	0x0000A4B4	R	16	A/D2 conversion data buffer 15	XIV-26

R/W Readable / Writable
R Readable only
W Writable only

14.2.2 Control Registers

These registers are 16-bit readable/writable registers which control an A/D converter.

■ A/D0 Conversion Control Register 0 (AN0CTR0: 0x0000A400) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	EX TRG0	-	AN0 CH2	AN0 CH1	AN0 CH0	AN0 EN	AN0 OFF	AN0 TRG	AN0 CK2	AN0 CK1	AN0 CK0	AN0 MD1	AN0 MD0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-13	-	-	-
12	EXTRG0	Edge detection at external trigger conversion	Reserved
11	-	-	-
10-8	AN0CH2 AN0CH1 AN0CH0	Channel number at any single channel conversion Start channel number at multiple channel conversion (When reading during A/D conversion, however, the channel number in conversion is read.)	000: ADIN00 001: ADIN01 010: ADIN02 011: ADIN03 100: ADIN04 101: ADIN05 110: Setting prohibited 111: Setting prohibited
7	AN0EN	Conversion start-execution flag	0: Disabled 1: Conversion start or in progress
6	AN0OFF	Power-down mode	0: Power-down mode 1: Operation mode
5	AN0TRG	External trigger A conversion start enable	0: Disabled 1: Enabled
4-2	AN0CK2 AN0CK1 AN0CK0	Conversion clock	000: IOCLK 001: 2 dividing of IOCLK 010: 3 dividing of IOCLK 011: 4 dividing of IOCLK 100: 8 dividing of IOCLK 101:16 dividing of IOCLK 110: setting prohibited 111: setting prohibited
1-0	AN0MD1 AN0MD0	Operation mode	00: Any single channel, one-time conversion 01: Multiple channels, one-time conversion for each 10: Any single channel, continuous conversion 11: Multiple channels, continuous conversion

Do not change the A/D0 conversion control register during A/D conversion.

■ A/D1 Conversion Control Register 0 (AN1CTR0: 0x0000A440) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	EX TRG1	-	AN1 CH2	AN1 CH1	AN1 CH0	AN1 EN	AN1 OFF	AN1 TRG	AN1 CK2	AN1 CK1	AN1 CK0	AN1 MD1	AN1 MD0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-13	-	-	-
12	EXTRG1	Edge detection at external trigger conversion	Reserved
11	-	-	-
10-8	AN1CH2 AN1CH1 AN1CH0	Channel number at any single channel conversion Start channel number at multiple channel conversion (When reading during A/D conversion, however, the channel number in conversion is read.)	000: ADIN02 001: ADIN03 010: ADIN04 011: ADIN05 100: ADIN06 101: ADIN07 110: ADIN08 111: ADIN09
7	AN1EN	Conversion start-execution flag	0: Disabled 1: Conversion start or in progress
6	AN1OFF	Power-down mode	0: Power-down mode 1: operation mode
5	AN1TRG	External trigger A conversion start enable	0: Disabled 1: Enabled
4-2	AN1CK2 AN1CK1 AN1CK0	Conversion clock	000: IOCLK 001: 2 dividing of IOCLK 010: 3 dividing of IOCLK 011: 4 dividing of IOCLK 100: 8 dividing of IOCLK 101:16 dividing of IOCLK 110: setting prohibited 111: setting prohibited
1-0	AN1MD1 AN1MD0	Operation mode	00: Any single channel, one-time conversion 01: Multiple channels, one-time conversion for each 10: Any single channel, continuous conversion 11: Multiple channels, continuous conversion

Do not change the A/D1 conversion control register during A/D conversion.

■ A/D2 Converter Control Register 0 (AN2CTR0: 0x0000A480) [8,16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	EX TRG 2	AN2 CH3	AN2 CH2	AN2 CH1	AN2 CH0	AN2 EN	AN2 OFF	AN2 TRG	AN2 CK2	AN2 CK1	AN2 CK0	AN2 MD1	AN2 MD0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-13	-	-	-
12	EX TRG2	Edge detection at external trigger conversion	Reserved
11	-	-	-
10-8	AN2CH3 AN2CH2 AN2CH1 AN2CH0	Channel number at any single channel conversion Start channel number at multiple channel conversion (When reading during A/D conversion, however, the channel number in conversion is read.)	0000: ADIN06 0001: ADIN07 0010: ADIN08 0011: ADIN09 0100: ADIN10 0101: ADIN11 0110: ADIN12 0111: ADIN13 1000: ADIN14 1001: ADIN15 1010: Setting prohibited 1011: Setting prohibited 1100: Setting prohibited 1101: Setting prohibited 1110: Setting prohibited 1111: Setting prohibited
7	AN2EN	Conversion start-execution flag	0: Disabled 1: Conversion start or in progress
6	AN2OFF	Power-down mode	0: Power-down mode 1: operation mode
5	AN2TRG	External trigger conversion start enable	0: Disabled 1: Enabled
4-2	AN2CK2 AN2CK1 AN2CK0	Conversion clock	000: IOCLK 001: 2 dividing of IOCLK 010: 3 dividing of IOCLK 011: 4 dividing of IOCLK 100: 8 dividing of IOCLK 101:16 dividing of IOCLK 110: setting prohibited 111: setting prohibited
1-0	AN2MD1 AN2MD0	Operation mode	00: Any single channel, one-time conversion 01: Multiple channels, one-time conversion for each 10: Any single channel, continuous conversion 11: Multiple channels, continuous conversion

Do not change the A/D2 conversion control register during A/D conversion.

■ A/D0 Conversion Control Register 1 (AN0CTR1: 0x0000A404) [8,16-bit Control Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	Reserved	Reserved	Reserved	Reserved	AN0CH0B2	AN0CH0B1	AN0CH0B0	AN0ENB	AN0TRGB	AN0SHC1	AN0SHC0	-	AN0NCH2	AN0NCH1	AN0NCH0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	-	-	-
14-11	Reserved	-	Write “0”
10-8	AN0CH0B2 AN0CH0B1 AN0CH0B0	Channel number at generation of trigger B. * The result of this channel conversion is stored in AN0BUF0B: x0000A430.	000: ADIN00 001: ADIN01 010: ADIN02 011: ADIN03 100: ADIN04 101: ADIN05 110: Setting prohibited 111: Setting prohibited
7	AN0ENB	Conversion start-execution flag B	0: Disabled 1: Conversion start or in progress
6	AN0TRGB	External trigger B conversion start enable	0: Disabled 1: Enabled
5-4	AN0SHC1 AN0SHC0	Sampling/hold cycle mode	00: 1 cycle 01: 2 cycles 10: 4 cycles 11: 6 cycles
3	-	-	-
2-0	AN0NCH2 AN0NCH1 AN0NCH0	Complete channel number at multiple channel conversion	000: ADIN00 001: ADIN01 010: ADIN02 011: ADIN03 100: ADIN04 101: ADIN05 110: Setting prohibited 111: Setting prohibited

■ A/D1 Conversion Control Register 1 (AN1CTR1: 0x0000A444) [8,16-bit Control Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	Reserved	Reserved	Reserved	Reserved	AN1CH0B2	AN1CH0B1	AN1CH0B0	AN1ENB	AN1TRGB	AN1SHC1	AN1SHC0	-	AN1NCH2	AN1NCH1	AN1NCH0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15	-	-	-
14-11	Reserved	-	Write “0”
10-8	AN1CH0B2 AN1CH0B1 AN1CH0B0	Channel number at generation of trigger B. * The result of this channel conversion is stored in AN1BUF0B: x0000A470.	000: ADIN02 001: ADIN03 010: ADIN04 011: ADIN05 100: ADIN06 101: ADIN07 110: ADIN08 111: ADIN09
7	AN1ENB	Conversion start-execution flag B	0: Disabled 1: Conversion start or in progress
6	AN1TRGB	External trigger B conversion start enable	0: Disabled 1: Enabled
5-4	AN1SHC1 AN1SHC0	Sampling/hold cycle mode	00: 1 cycle 01: 2 cycles 10: 4 cycles 11: 6 cycles
3	-	-	-
2-0	AN1NCH2 AN1NCH1 AN1NCH0	Complete channel number at multiple channel conversion	000: ADIN02 001: ADIN03 010: ADIN04 011: ADIN05 100: ADIN06 101: ADIN07 110: ADIN08 111: ADIN09

■ A/D2 Conversion Control Register 1 (AN2CTR1: 0x0000A484) [8,16-bit Control Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-	-	-	AN2SHC1	AN2SHC0	AN2NCH3	AN2NCH2	AN2NCH1	AN2NCH0
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
15-6	-	-	-
5-4	AN2SHC1 AN2SHC0	Sampling/hold cycle mode	00: 1 cycle 01: 2 cycles 10: 4 cycles 11: 6 cycles
3-0	AN2NCH3 AN2NCH2 AN2NCH1 AN2NCH0	Channel number at generation of trigger B.	0000: ADIN06 0001: ADIN07 0010: ADIN08 0011: ADIN09 0100: ADIN10 0101: ADIN11 0110: ADIN12 0111: ADIN13 1000: ADIN14 1001: ADIN15 1010: Setting prohibited 1011: Setting prohibited 1100: Setting prohibited 1101: Setting prohibited 1110: Setting prohibited 1111: Setting prohibited

14.2.3 A/D Start Trigger Selection Registers

A/D start trigger selection registers are used for selecting each A/D conversion start trigger.

■ A/D0 Start Trigger Selection Register (ADST0: 0x0000A408) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	AD0BST2	AD0BST1	AD0BST0	-	AD0AST2	AD0AST1	AD0AST0
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7	-	-	-
6-4	AD0BST2 AD0BST1 AD0BST0	AD0 start trigger selection B	000: PWM0 overflow 001: PWM0 underflow 010: Timer 12 compare A 011: Timer 12 compare B 100: PWM1 overflow 101: PWM1 overflow 110: Timer 13 compare A 111: Timer 13 compare B
3	-	-	-
2-0	AD0AST2 AD0AST1 AD0AST0	AD0 start trigger selection A	000: PWM0 overflow 001: PWM0 underflow 010: Timer 12 compare A 011: Timer 12 compare B 100: PWM1 overflow 101: PWM1 overflow 110: Timer 13 compare A 111: Timer 13 compare B

* If the A/D0 start trigger selection A of the ADST0 is accessed, the A/D0 start trigger count register and the AN0CTREGA register are cleared.

■ A/D1 Start Trigger Selection Register (ADST1: 0x0000A448) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	AD1BST2	AD1BST1	AD1BST0	-	AD1AST2	AD1AST1	AD1AST0
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7	-	-	-
6-4	AD1BST2 AD1BST1 AD1BST0	AD1 start trigger selection B	000: PWM0 overflow 001: PWM0 underflow 010: Timer 12 compare A 011: Timer 12 compare B 100: PWM1 overflow 101: PWM1 overflow 110: Timer 13 compare A 111: Timer 13 compare B
3	-	-	-
2-0	AD1AST2 AD1AST1 AD1AST0	AD1 start trigger selection A	000: PWM0 overflow 001: PWM0 underflow 010: Timer 12 compare A 011: Timer 12 compare B 100: PWM1 overflow 101: PWM1 overflow 110: Timer 13 compare A 111: Timer 13 compare B

■ A/D2 Start Trigger Selection Register (ADST2: 0x0000A488) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	AD2ST2	AD2ST1	AD2ST0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-3	-	-	-
2-0	AD2ST2 AD2ST1 AD2ST0	AD2 start trigger selection	000: PWM0 overflow 001: PWM0 underflow 010: Timer 12 compare A 011: Timer 12 compare B 100: PWM1 overflow 101: PWM1 overflow 110: Timer 13 compare A 111: Timer 13 compare B

14.2.4 A/D Start Trigger Count Registers

A/D start trigger count registers are used for counting each A/D conversion start trigger. AD starts after the set number is counted.

■ A/D0 Start Trigger A Count Register (AN0CTREGA: 0x0000A40C) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	AN0A CNT3I	AN0A CNT2I	AN0A CNT1I	AN0A CNT0I	AN0A CNT3	AN0A CNT2	AN0A CNT1	AN0A CNT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-4	AN0ACNT3I AN0ACNT2I AN0ACNT1I AN0ACNT0I	Setting the number of AD0 external trigger A counting (at the first AD conversion)	0000~1111: 0 to 15 times AD starts after the set number of trigger factor A is counted.
3-0	AN0ACNT3 AN0ACNT2 AN0ACNT1 AN0ACNT0	Setting the number of AD0 external trigger A counting (at AD conversion after the second time)	0000~1111: 0 to 15 times AD starts after the set number of trigger factor A is counted.

■ A/D0 Start Trigger B Count Register (AN0CTREGB: 0x0000A40D) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	AN0B CNT3I	AN0B CNT2I	AN0B CNT1I	AN0B CNT0I	AN0B CNT3	AN0B CNT2	AN0B CNT1	AN0B CNT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-4	AN0BCNT3I AN0BCNT2I AN0BCNT1I AN0BCNT0I	Setting the number of AD0 external trigger B counting (at the first AD conversion)	0000~1111: 0 to 15 times AD starts after the set number of trigger factor B is counted.
3-0	AN0BCNT3 AN0BCNT2 AN0BCNT1 AN0BCNT0	Setting the number of AD0 external trigger B counting (at AD conversion after the second time)	0000~1111: 0 to 15 times AD starts after the set number of trigger factor B is counted.

■ A/D1Start Trigger A Count Register (AN1CTREGA: 0x0000A44C) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	AN1A CNT3I	AN1A CNT2I	AN1A CNT1I	AN1A CNT0I	AN1A CNT3	AN1A CNT2	AN1A CNT1	AN1A CNT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-4	AN1ACNT3I AN1ACNT2I AN1ACNT1I AN1ACNT0I	Setting the number of AD1 external trigger A counting (at the first AD conversion)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor A is counted.
3-0	AN1ACNT3 AN1ACNT2 AN1ACNT1 AN1ACNT0	Setting the number of AD1 external trigger A counting (at AD conversion after the second time)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor A is counted.

■ A/D1Start Trigger B Count Register (AN1CTREGB: 0x0000A44D) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	AN1B CNT3I	AN1B CNT2I	AN1B CNT1I	AN1B CNT0I	AN1B CNT3	AN1B CNT2	AN1B CNT1	AN1B CNT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-4	AN1BCNT3I AN1BCNT2I AN1BCNT1I AN1BCNT0I	Setting the number of AD1 external trigger B counting (at the first AD conversion)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor B is counted.
3-0	AN1BCNT3 AN1BCNT2 AN1BCNT1 AN1BCNT0	Setting the number of AD1 external trigger B counting (at AD conversion after the second time)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor B is counted.

■ A/D2 Start Trigger Count Register (AN2CTREGA: 0x0000A48C) [8-bit Access Register]

bp	7	6	5	4	3	2	1	0
Flag	AN2A CNT3I	AN2A CNT2I	AN2A CNT1I	AN2A CNT0I	AN2A CNT3	AN2A CNT2	AN2A CNT1	AN2A CNT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	Setting condition
7-4	AN2ACNT3I AN2ACNT2I AN2ACNT1I AN2ACNT0I	Setting the number of AD2 external trigger counting (at the first AD conversion)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor B is counted.
3-0	AN2ACNT3 AN2ACNT2 AN2ACNT1 AN2ACNT0	Setting the number of AD2 external trigger counting (at AD conversion after the second time)	0000~1111: 0 to 15 times AD starts after the set number of counts of trigger factor B is counted.

Do not write to the ANnCTREG during counting operation. Because when writing to the ANnCTREG is executed, the internal counter that counts trigger factors is cleared.

14.2.5 Data Buffers

A/D conversion result (10 bits) is stored in A/D conversion data buffers.

■ A/D0 Conversion Data Buffer 0 (AN0BUF00: 0x0000A410) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0 BUF 09	AN0 BUF 08	AN0 BUF 07	AN0 BUF 06	AN0 BUF 05	AN0 BUF 04	AN0 BUF 03	AN0 BUF 02	AN0 BUF 01	AN0 BUF 00
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF09 to AN0BUF00	A/D0 conversion result of ADIN00 pin	A/D0 conversion result of ADIN00 pin

■ A/D0 Conversion Data Buffer 1 (AN0BUF01: 0x0000A414) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0 BUF 19	AN0 BUF 18	AN0 BUF 17	AN0 BUF 16	AN0 BUF 15	AN0 BUF 14	AN0 BUF 13	AN0 BUF 12	AN0 BUF 11	AN0 BUF 10
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF19 to AN0BUF10	A/D0 conversion result of ADIN01 pin	A/D0 conversion result of ADIN01 pin

■ A/D0 Conversion Data Buffer 2 (AN0BUF02: 0x0000A418) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0 BUF 29	AN0 BUF 28	AN0 BUF 27	AN0 BUF 26	AN0 BUF 25	AN0 BUF 24	AN0 BUF 23	AN0 BUF 22	AN0 BUF 21	AN0 BUF 20
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF29 to AN0BUF20	A/D0 conversion result of ADIN02 pin	A/D0 conversion result of ADIN02 pin

■ A/D0 Conversion Data Buffer 3 (AN0BUF03: 0x0000A41C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0BUF39	AN0BUF38	AN0BUF37	AN0BUF36	AN0BUF35	AN0BUF34	AN0BUF33	AN0BUF32	AN0BUF31	AN0BUF30
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF39 to AN0BUF30	A/D0 conversion result of ADIN03 pin	A/D0 conversion result of ADIN03 pin

■ A/D0 Conversion Data Buffer 4 (AN0BUF04: 0x0000A420) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0BUF49	AN0BUF48	AN0BUF47	AN0BUF46	AN0BUF45	AN0BUF44	AN0BUF43	AN0BUF42	AN0BUF41	AN0BUF40
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF49 to AN0BUF40	A/D0 conversion result of ADIN04 pin	A/D0 conversion result of ADIN04 pin

■ A/D0 Conversion Data Buffer 5 (AN0BUF05: 0x0000A424) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0BUF59	AN0BUF58	AN0BUF57	AN0BUF56	AN0BUF55	AN0BUF54	AN0BUF53	AN0BUF52	AN0BUF51	AN0BUF50
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF59 to AN0BUF50	A/D0 conversion result of ADIN05 pin	A/D0 conversion result of ADIN05 pin

■ A/D0 Conversion Data Buffer 0B (AN0BUF0B: 0x0000A430) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN0 BUF 0B9	AN0 BUF 0B8	AN0 BUF 0B7	AN0 BUF 0B6	AN0 BUF 0B5	AN0 BUF 0B4	AN0 BUF 0B3	AN0 BUF 0B2	AN0 BUF 0B1	AN0 BUF 0B0
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN0BUF0B9 to AN0BUF0B0	Conversion result of AD input pin selected with conversion channel selection (AN0CH0B2-0) at trigger B generation of AD0 conversion control register (AN0CTR1)	Conversion result of AD input pin selected with conversion channel selection (AN0CH0B2-0) at trigger B generation of AD0 conversion control register (AN0CTR1)

■ A/D1 Conversion Data Buffer 2 (AN1BUF02: 0x0000A450) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF29	AN1BUF28	AN1BUF27	AN1BUF26	AN1BUF25	AN1BUF24	AN1BUF23	AN1BUF22	AN1BUF21	AN1BUF20
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF29 to AN1BUF20	A/D1 conversion result of ADIN02 pin	A/D1 conversion result of ADIN02 pin

■ A/D1 Conversion Data Buffer 3(AN1BUF03: 0x0000A454) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF39	AN1BUF38	AN1BUF37	AN1BUF36	AN1BUF35	AN1BUF34	AN1BUF33	AN1BUF32	AN1BUF31	AN1BUF30
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF39 to AN1BUF30	A/D1 conversion result of ADIN03 pin	A/D1 conversion result of ADIN03 pin

■ A/D1 Conversion Data Buffer 4 (AN2BUF04: 0x0000A458) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF49	AN1BUF48	AN1BUF47	AN1BUF46	AN1BUF45	AN1BUF44	AN1BUF43	AN1BUF42	AN1BUF41	AN1BUF40
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF49 to AN1BUF40	A/D1 conversion result of ADIN04 pin	A/D1 conversion result of ADIN04 pin

■ A/D1 Conversion Data Buffer 5 (AN1BUF05: 0x0000A45C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF59	AN1BUF58	AN1BUF57	AN1BUF56	AN1BUF55	AN1BUF54	AN1BUF53	AN1BUF52	AN1BUF51	AN1BUF50
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF59 to AN1BUF50	A/D1 conversion result of ADIN05 pin	A/D1 conversion result of ADIN05 pin

■ A/D1 Conversion Data Buffer 6 (AN1BUF06: 0x0000A460) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF69	AN1BUF68	AN1BUF67	AN1BUF66	AN1BUF65	AN1BUF64	AN1BUF63	AN1BUF62	AN1BUF61	AN1BUF60
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF69 to AN1BUF60	A/D1 conversion result of ADIN06 pin	A/D1 conversion result of ADIN06 pin

■ A/D1 Conversion Data Buffer 7 (AN1BUF07: 0x0000A464)[16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF79	AN1BUF78	AN1BUF77	AN1BUF76	AN1BUF75	AN1BUF74	AN1BUF73	AN1BUF72	AN1BUF71	AN1BUF70
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF79 to AN1BUF70	A/D1 conversion result of ADIN07 pin	A/D1 conversion result of ADIN07 pin

■ A/D1 Conversion Data Buffer 8 (AN1BUF08: 0x0000A468) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF89	AN1BUF88	AN1BUF87	AN1BUF86	AN1BUF85	AN1BUF84	AN1BUF83	AN1BUF82	AN1BUF81	AN1BUF80
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF89 to AN1BUF80	A/D1 conversion result of ADIN08 pin	A/D1 conversion result of ADIN08 pin

■ A/D1 Conversion Data Buffer 9 (AN1BUF09: 0x0000A46C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF99	AN1BUF98	AN1BUF97	AN1BUF96	AN1BUF95	AN1BUF94	AN1BUF93	AN1BUF92	AN1BUF91	AN1BUF90
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF99 to AN1BUF90	A/D1 conversion results of ADIN09 pin	A/D1 conversion results of ADIN09 pin

■ A/D1 Conversion Data Buffer 0B (AN1BUF0B: 0x0000A470) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN1BUF0B9	AN1BUF0B8	AN1BUF0B7	AN1BUF0B6	AN1BUF0B5	AN1BUF0B4	AN1BUF0B3	AN1BUF0B2	AN1BUF0B1	AN1BUF0B0
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN1BUF0B9 to AN1BUF0B0	Conversion result of AD input pin selected with conversion channel selection (AN1CH0B2-0) at trigger B generation of AD1 conversion control register (AN1CTR1)	Conversion result of AD input pin selected with conversion channel selection (AN1CH0B2-0) at trigger B generation of AD1 conversion control register (AN1CTR1)

■ A/D2 Conversion Data Buffer 6 (AN2BUF06: 0x0000A490) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF69	AN2BUF68	AN2BUF67	AN2BUF66	AN2BUF65	AN2BUF64	AN2BUF63	AN2BUF62	AN2BUF61	AN2BUF60
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF69 to AN2BUF60	A/D2 conversion result of ADIN06 pin	A/D2 conversion result of ADIN06 pin

■ A/D2 Conversion Data Buffer 7 (AN2BUF07: 0x0000A494) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF79	AN2BUF78	AN2BUF77	AN2BUF76	AN2BUF75	AN2BUF74	AN2BUF73	AN2BUF72	AN2BUF71	AN2BUF70
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF79 to AN2BUF70	A/D2 conversion result of ADIN07 pin	A/D2 conversion result of ADIN07 pin

■ A/D2 Conversion Data Buffer 8 (AN2BUF08: 0x0000A498) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF89	AN2BUF88	AN2BUF87	AN2BUF86	AN2BUF85	AN2BUF84	AN2BUF83	AN2BUF82	AN2BUF81	AN2BUF80
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF89 to AN2BUF80	A/D2 conversion result of ADIN08 pin	A/D2 conversion result of ADIN08 pin

■ A/D2 Conversion Data Buffer 9 (AN2BUF09: 0x0000A49C) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF99	AN2BUF98	AN2BUF97	AN2BUF96	AN2BUF95	AN2BUF94	AN2BUF93	AN2BUF92	AN2BUF91	AN2BUF90
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF99 to AN2BUF90	A/D2 conversion result of ADIN09 pin	A/D2 conversion result of ADIN09 pin

■ A/D2 Conversion Data Buffer 10 (AN2BUF10: 0x0000A4A0) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF109	AN2BUF108	AN2BUF107	AN2BUF106	AN2BUF105	AN2BUF104	AN2BUF103	AN2BUF102	AN2BUF101	AN2BUF100
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF109 to AN2BUF100	A/D2 conversion result of ADIN10 pin	A/D2 conversion result of ADIN10 pin

■ A/D2 Conversion Data Buffer 11 (AN2BUF11: 0x0000A4A4) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF119	AN2BUF118	AN2BUF117	AN2BUF116	AN2BUF115	AN2BUF114	AN2BUF113	AN2BUF112	AN2BUF111	AN2BUF110
At reset	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUFB119 to AN2BUFB110	A/D2 conversion result of ADIN11 pin	A/D2 conversion result of ADIN11 pin

■ A/D2 Conversion Data Buffer 12 (AN2BUF12: 0x0000A4A8) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF129	AN2BUF128	AN2BUF127	AN2BUF126	AN2BUF125	AN2BUF124	AN2BUF123	AN2BUF122	AN2BUF121	AN2BUF120
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF129 to AN2BUF120	A/D2 conversion result of ADIN12 pin	A/D2 conversion result of ADIN12 pin

■ A/D2 Conversion Data Buffer 13 (AN2BUF13: 0x0000A4AC) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF139	AN2BUF138	AN2BUF137	AN2BUF136	AN2BUF135	AN2BUF134	AN2BUF133	AN2BUF132	AN2BUF131	AN2BUF130
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF139 to AN2BUF130	A/D2 conversion result of ADIN13 pin	A/D2 conversion result of ADIN13 pin

■ A/D2 Conversion Data Buffer 14 (AN2BUF14: 0x0000A4B0) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF149	AN2BUF148	AN2BUF147	AN2BUF146	AN2BUF145	AN2BUF144	AN2BUF143	AN2BUF142	AN2BUF141	AN2BUF140
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF149 to AN2BUF140	A/D2 conversion result of ADIN14 pin	A/D2 conversion result of ADIN14 pin

■ A/D2 Conversion Data Buffer 15 (AN2BUF15: 0x0000A4B4) [16-bit Access Register]

bp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	AN2BUF159	AN2BUF158	AN2BUF157	AN2BUF156	AN2BUF155	AN2BUF154	AN2BUF153	AN2BUF152	AN2BUF151	AN2BUF150
At reset	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bp	Flag	Description	Setting condition
15-10	-	-	-
9-0	AN2BUF159 to AN2BUF150	A/D2 conversion result of ADIN15 pin	A/D2 conversion result of ADIN15 pin

14.3 Operation

14.3.1 A/D Converter Operation

■ A/D Converter Timing

Figure: 14.3.1 shows A/D converter timing. The conversion time of A/D converter is the total of the sampling hold (S/H) time , 10 bit conversion time and transfer time. When S/H time is 1 cycle, conversion time is 12 conversion clock cycles. When S/H time is 4 cycles, conversion time is 15 conversion clock cycles.

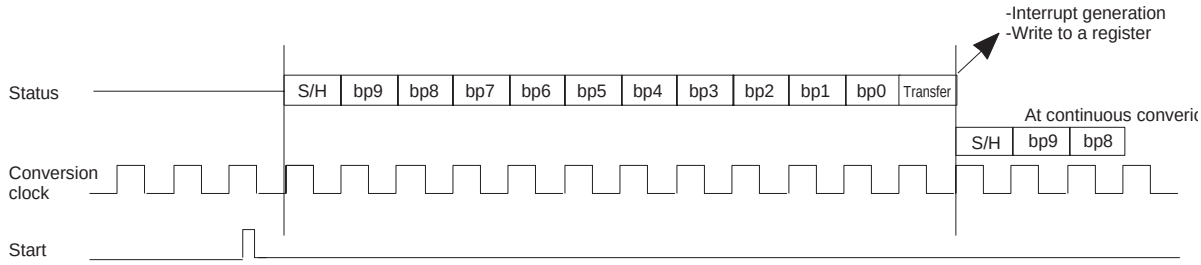


Figure:14.3.1 A/D Converter Timing (S/H 1 Cycle)

■ Setting Clock for A/D Converter

A/D conversion clock can be selected from 1, 2, 3, 4, 8 and 16 dividing of IOCLK. However, it have to be selected so that the conversion time is over 1.0μs and S/H time is over 200ns. The following table shows the conversion time at IOCLK=30MHz.

The conversion clock should be selected from 2, 3, 4, 8, and 16 dividing at IOCLK=30MHz.

Table:14.3.1 A/D Conversion Time

Set value		A/D converter time			
Conversion clock (cycle)	S/H cycle	S/H time	10 bit conversion time	Transfer time	Total
IOCLK × 3 (100 ns)	2 cycles	200 ns	1 cycle × 10 bits (1.0 μs)	1 cycle (100 ns)	13 cycles (1.3 μs)
IOCLK × 2 (66.7 ns)	4 cycles	267 ns	1 cycle × 10 bits (667 ns)	1 cycle (66.7 ns)	15 cycles (1.0 μs)
IOCLK: 30 MHz					

■ Setting Sampling/Hold Time

Sampling/hold time can be selected from 1, 2 , 4 and 6 cycles of the conversion clock. Select the proper value with the A/D input impedance. If the A/D input impedance is high, select 6 cycles.

■ Selecting Operation Mode

Operation mode is set by the AN0MD1-0 flags of the AN0CTR0 register and the AN1MD1-0 flags of the AN1CTR0 register and the AN2MD1-0 flags of the AN2CTR0 register. Table: 14.3.2 shows the operation mode to be set. One-time conversion means that one-time input to the ADINn pin is converted by the any single channel or multiple channels. Continuous conversion means that the conversion is continued until it is stopped by the any single channel or multiple channels.

Table:14.3.2 Operation Mode of A/D Conversion

ANnMD1	ANnMD0	Operation mode
0	0	Any single channel/one-time conversion
0	1	Multiple channels/one-time conversion for each
1	0	Any single channel/continuous conversion
1	1	Multiple channels/continuous conversion

■ A/D Converter Start

A/D conversion is started when the set-up start trigger is generated.

Table:14.3.3 Converter Start Trigger (AD0, 1, 2)

Start trigger	AN0TRG (AN0CTR)	ADnAST2-0 (ADSTn)	ANnTRGB (ANnCTR1	Description
Register set by instruction	0	-	-	Conversion is started by setting the ANnEN flag of the conversion control register (ANnCTR0) to “1”.
PWM0 overflow	1	000	1	Conversion is started by PWN0 overflow signal.
PWM0 underflow	1	001	1	Conversion is started by PWN0 underflow signal.
Timer 12 compare A	1	010	1	Conversion is started by the timer 12 compare A interrupt.
Timer 12 compare B	1	011	1	Conversion is started by the timer 12 compare B interrupt.
PWM1 overflow	1	100	1	Conversion is started by PWN1 overflow signal.
PWM1 underflow	1	101	1	Conversion is started by PWN1 underflow signal.
Timer 13 compare A	1	110	1	Conversion is started by the timer 13 compare A interrupt.
Timer 13 compare B	1	111	1	Conversion is started by the timer 13 compare B interrupt.

■ A/D Converter Stop

A/D converter stop differs depending on the conversion mode to be selected.

Table:14.3.4 A/D Converter Stop

Operation mode	Stop operation
Any single channel/one time conversion	When one-time conversion ends, all the conversion operation is completed and the conversion operation is stopped.
Multiple channels/one time conversion for each	
Any single channel/continuous conversion	The conversion operation is not stopped even if one-time conversion ends. To stop the conversion, the ANnEN flag needs to be cleared to “0”.
Multiple channels/continuous conversion	

■ Power-down Mode

Power-down mode is used to minimize the standby power requirement. Set the ANnOFF flag of the ANnCTR0 register to “0”, for power-down mode and to “1” for operation mode. Set it to operation mode at conversion operation. 100 ns wait is required from operation mode starting to A/D converter starting.

■ Any Single Channel/One-time Conversion (AD0, AD1)

One channel A/D input is converted only once. The A/D interrupt is generated at the same time when conversion ends. Set the channel number to be converted to the ANnCH2-0 flags of the ANnCTR0 register (conversion channel at any single channel conversion). When conversion is started by the ANnEN flag (conversion start-execution flag), set the ANnTRG flag to “0” and the ANnEN flag to “1”. The ANnEN flag is “1” during conversion and “0” after conversion ends.

■ Any Single Channel/One-time Conversion (AD2)

One channel A/D input is converted only once. The A/D interrupt is generated at the same time when conversion ends. Set the channel number to be converted to the AN2CH3-0 flags of the AN2CTR0 register (conversion channel at any single channel conversion). When conversion is started by the AN2EN flag (conversion start-execution flag), set the AN2TRG flag to “0” and the AN2EN flag to “1”. The AN2EN flag is “1” during conversion and “0” after conversion ends.

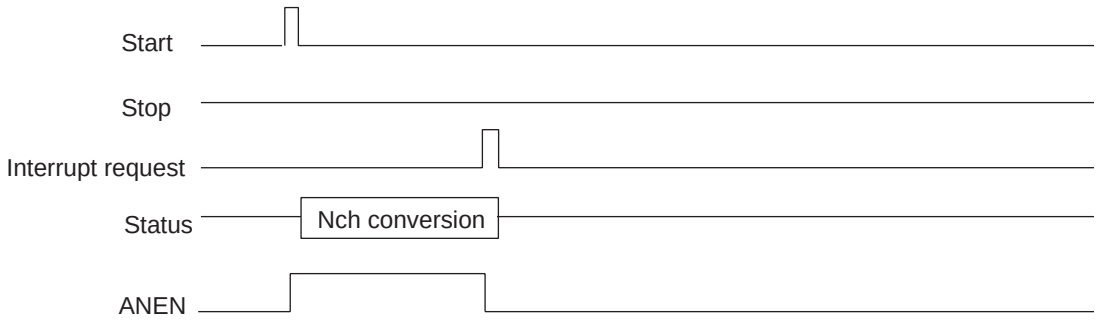


Figure:14.3.2 Any Single Channel/One-time Conversion Timing

■ Multiple Channels/One-time Conversion for Each (AD0 , AD1)

Continuous multiple A/D input is converted only once. The A/D interrupt is generated at the same time when all conversions of multiple channels end. Set the first channel to be converted by the ANnCH2-0 flags of the ANnCTR0 register and the last channel by the ANnNCH2-0 flags of the ANnCTR1 register.

When conversion is started by the ANnEN flag (conversion start-execution flag), set the ANnTRG flag to “0” and the ANnEN flag to “1”. The ANnEN flag is “1” during conversion and changes to “0” after conversion of all channels is completed. The ANnCH2-0 flags become the channel number being converted during conversion and change to the first channel number after conversion of all multiple channels is completed.

■ Multiple Channels/One-time Conversion for Each (AD2)

Continuous multiple A/D input is converted only once. The A/D interrupt is generated at the same time when all conversions of multiple channel end. Set the first channel number to be converted by the AN2CH3-0 flags of the AN2CTR0 register and the last channel by the AN2NCH3-0 flags of the AN2CTR1 register.

When conversion is started by the AN2EN flag (conversion start-execution flag), set the AN2TRG flag to “0” and the AN2EN flag to “1”. The AN2EN flag is “1” during conversion and changes to “0” after conversion ends. The AN2CH3-0 flags become the channel number being converted during conversion and change to the first channel number after conversion of all multiple channels is completed.

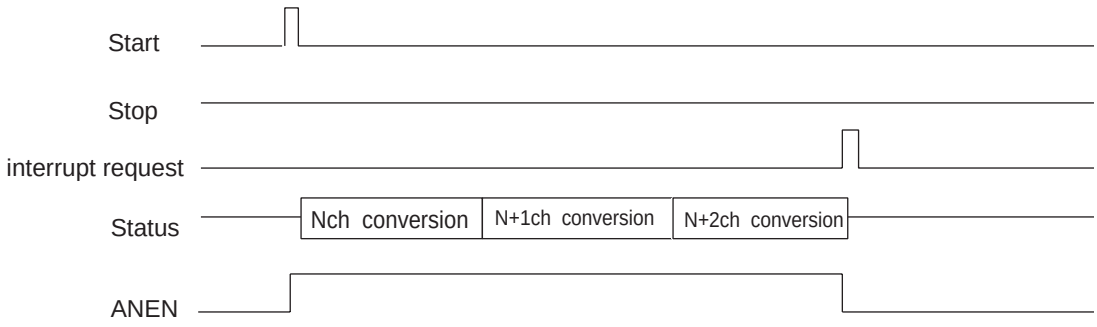


Figure:14.3.3 Multiple Channels/Timing of One-time Conversion for Each

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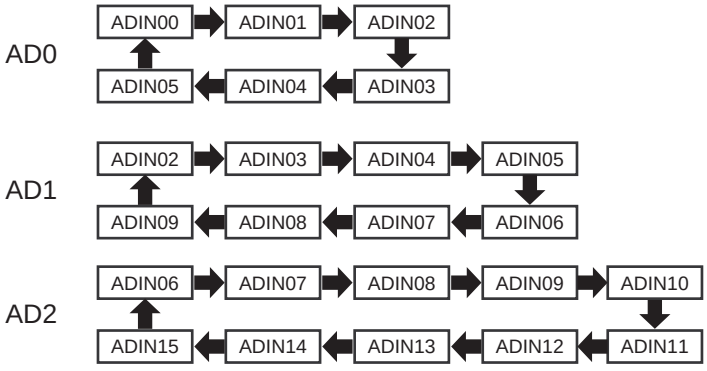
Multiple channels are converted in the following order.



■ Any Single Channel/Continuous Conversion (AD0, AD1)

A/D input of single channel is converted continuously. The A/D interrupt is generated every time conversion ends. Set the channel number to be converted to the ANnCH2-0 flags of the ANnCTR0 register (conversion channel at any single channel conversion). Set the ANnTRG flag to “0” and the ANnEN flag to “1” in order to start conversion by the ANnEN flag (conversion start-execution flag). Conversion is terminated when the ANnEN flag is set to “0” forcedly.

■ Any Single Channel/Continuous Conversion (AD2)

A/D input of single channel is converted continuously. The A/D interrupt is generated every time conversion ends. Set the channel number to be converted to the AN2CH3-0 flags of the AN2CTR0 register (conversion channel at any single channel conversion). Set the AN2TRG flag to “0” and the AN2EN flag to “1” in order to start conversion by the AN2EN flag (conversion start-execution flag). Conversion is terminated when the AN2EN flag is set to “0” forcedly.

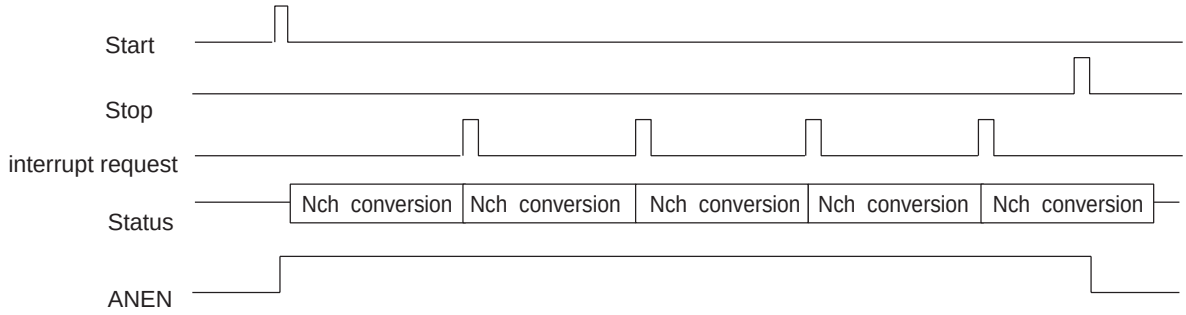


Figure:14.3.4 Any SIngle Channel/Timing of Continuous Conversion

The ANnNCH2-0 flags of the ANnCTR0 register and the ANnNCH3-0 flags of the AN2CTR0 register are ignored.

■ Multiple Channels/Continuous Conversion (AD0, AD1)

Continuous multiple A/D input is converted continuously. The A/D interrupt is generated every time all conversions of multiple channels end. Set the first channel to be converted by the ANnCH2-0 flags of the ANnCTR0 and the last channel by the ANnNCH2-0 flags of the ANnCTR1 register.

When conversion is started by the ANnEN flag (conversion start-execution flag), set the ANnTRG flag to “0” and the ANnEN flag to “1”. Conversion is terminated by setting the ANnEN flag to”0” forcedly. The ANnEN flag is “1” during conversion and changes to “0” after conversion of all channels end. The AN2CH3-0 flags become the channel number being converted during conversion and change to the first channel number after conversion of all channels is completed.

■ Multiple Channels/Continuous Conversion (AD2)

Continuous multiple A/D input is converted continuously. The A/D interrupt is generated every time all conversions of multiple channels end. Set the first channel to be converted by the AN2CH3-0 flags of the AN2CTR0 and the last channel by the AN2NCH3-0 flags of the AN2CTR1 register.

When conversion is started by the AN2EN flag (conversion start-execution flag), set the AN2TRG flag to “0” and the AN2EN flag to “1”. Conversion is terminated by setting the AN2EN flag to”0” forcedly. The AN2EN flag is “1” during conversion and changes to “0” after conversion of all channels end. The AN2CH3-0 flags become the channel number being converted during conversion and change to the first channel number after conversion of all channels is completed.

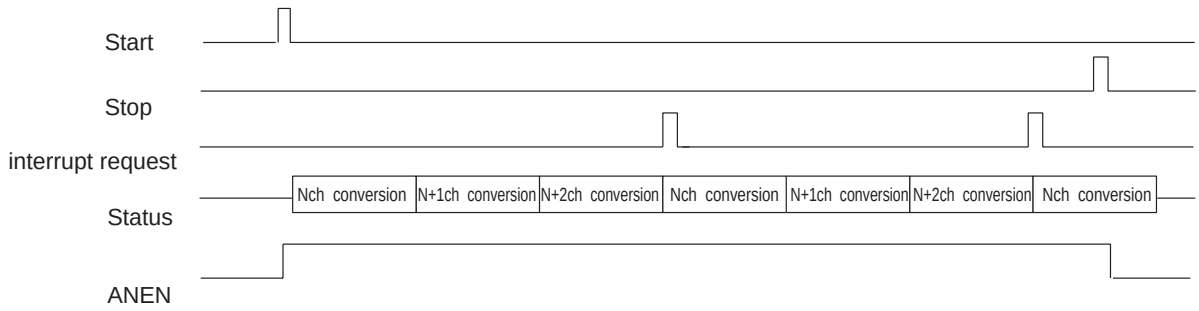
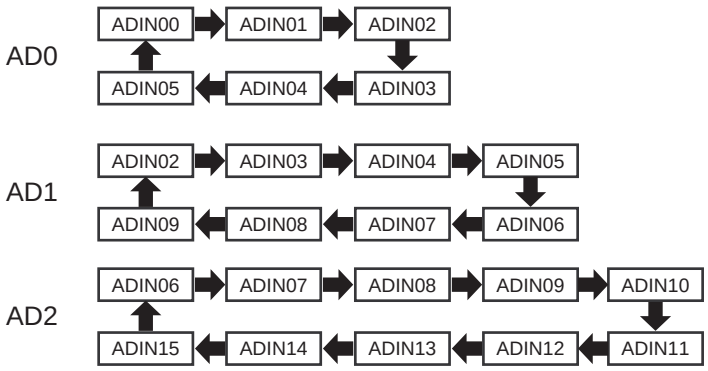


Figure:14.3.5 Multiple Channels/Continuous Conversion Timing

Multiple channels are converted in the following order.



14.3.2 Setup Example

■ Setup Example for Single Channel/One-time Conversion

The following shows an example of 1-channel A/D converter. Analog voltage (VDD to VSS) is fed to the ANIN00 pin to obtain A/D conversion result.

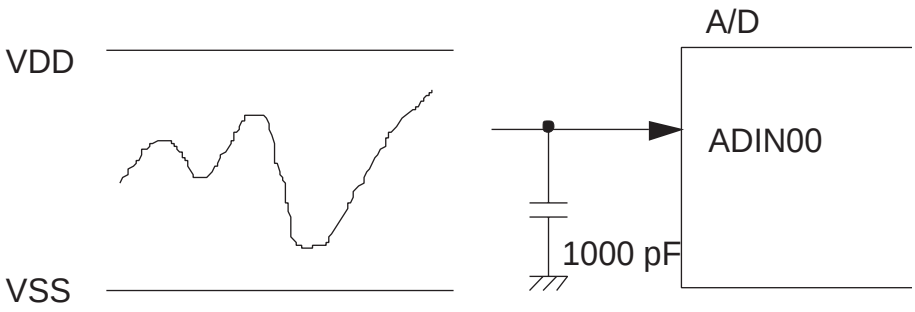


Figure:14.3.6 1-Channel A/D Conversion

Table:14.3.5 Conditions of 1-Channel A/D Conversion

Setting item	Description
Input pin	ADIN00 pin
Operation mode	Any Single Channel/One-time Conversion
IOCLK	30MHz

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the A/D converter operation AN0CTR0(0x0000A400) bp7: AN0EN=0 bp5: AN0TRG=0	(1) Set the AN0EN and AN0TRG flags of the A/D0 conversion control register (AN0CTR0) to “0” to stop the A/D conversion.
(2) Set the AN0CTR0 register Set the operation mode AN0CTR0(0x0000A400) bp1-0: AN0MD1-0=00 Set the conversion clock AN0CTR0(0x0000A400) bp4-2: AN0CK2-0=010 Set the conversion channel AN0CTR0(0x0000A400) bp10-8: AN0CH2-0=000 Set the power-down mode AN0CTR0(0x0000A400) bp6: AN0OFF=1 Set the AN0CTR1 register Set the S/H cycle bp5-4: AN0SHC1-0=10	(2) Set the AN0MD1-0 flags of the AN0CTR0 register to “00”to set “any single channel/one-time conversion” to operation mode. Set the AN0CK2-0 flags of the AN0CTR0 register to “010” to set 3 dividing of IOCLK to the conversion clock. Set the AN0CH2-0 flags of the ANOCTR0 register to “000” to set “channel 0” to the conversion channel. Set the AN0OFF flag of the ANOCTR0 register to “1” to set operation mode to the power-mode flag. Set the AN0SHC1-0 flags of the AN0CTR0 register to “10” to set 4 cycles to S/H cycle. *After shifted to operation mode, more than 100nsec wait time is necessary until A/D conversion starts. .
(3) Start the A/D converter operation AN0CTR00(0x0000A400) bp7: AN0EN=1	(3) Set the AN0EN flag of the AN0CTR0 register to “1” to start A/D conversion. Conversion is started at the rising edge of the first A/D conversion clock after the flag is set to “1”. The conversion time is 15cycles of the A/D conversion clock (1.5μs).
(4) Wait the A/D conversion operation completed AN0CTR00(0x0000A400) bp7: AN0EN	(4) Wait for conversion to be completed . The AN0EN flag of the AN0CTR0 register is to “1” during conversion and cleared to “0” after conversion is completed. Wait for The AN0EN flag to be to “0” by program.
(5) Read the A/D value AN0BUF00(0x0000A410)	(5) The A/D0 conversion data buffer 0 (AN0BUF00) is read out.

The result of conversion can be read out by generating an interrupt. In that case, it is not necessary to wait for the AN0EN flag since an interrupt is generated after the result is stored in AN0BUF00.

■ Setup Example of Multiple Channels/One-Time Conversion for Each

A/D converter result can be obtained with feeding analog voltage by the ADIN00 and ADIN01 pins. Conversion is performed regularly with the timer 12 compare A matching.

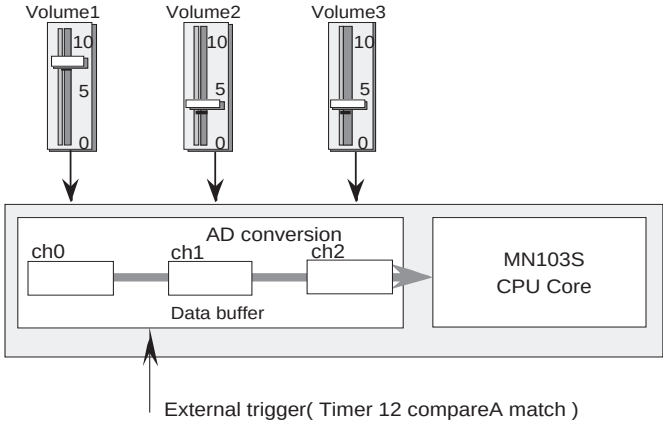


Figure:14.3.7 1-channel A/D Conversion

Table:14.3.6 Conditions for Multiple Channel A/D Conversion ·

Setting item	Description
Input pin	ADIN00 pin ADIN01 pin ADIN02 pin
Operation mode	Multiple channels/one-time conversion for each
A/D converter start trigger	Timer 12 compare A
A/D converter start cycle	1ms
IOCLK	30MHz

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the AD0: Stop the A/D conversion operation AN0CTR0(0x0000A400) bp7: AN0EN=0 bp5:AN0TRG=0	(1) Set the AN0EN and AN0TRG flags of the A/D0 conversion control register (AN0CTR0) to “0” to stop A/D conversion.
(2) Set the AD0: Disable the AD0 complete interrupt G26ICR(0x00008968) bp8: G26IE0=0	(2) Set the G26IE0 flag of the G26ICR register to “0” to disable the AD0 conversion complete interrupt.
(3) Set the timer 11: Stop the timer 12 TM12MD(0x0000A280) bp6: TMLDE=0 bp7: TMCNE=0	(3) Set the TMLDE and TMCNE flags of the timer 12 mode register (TM12MD) to “0” to stop the timer 12 counting.

Setup Procedure	Description
(4) Set the AD0: Set the AN0CTR0 register Set the operation mode AN0CTR0(0x0000A400) bp1-0: AN0MD1-0=01 Set the conversion clock AN0CTR0(0x0000A400) bp4-2: AN0CK2-0=011 Set the conversion start channel AN0CTR0(0x0000A400) bp10-8: AN0CH2-0=000 Set the conversion complete channel AN0CTR1(0x0000A404) bp14-12: AN0NCH2-0=010 Set the power-down mode AN0CTR0(0x0000A400) bp6: AN0OFF=1	(4) Set the AN0MD1-0 flags of the AN0CTR0 register to “01” to set “multiple channels/one-timer conversion” to operation mode. Set the AN0CK2-0 flags of the AN0CTR0 register to “011” to set the conversion clock to4 dividing of IOCLK. Set the AN0CH2-0 flags of the AN0CTR0 register to “000” to set “channel 0” to the conversion channel. Set the AN0NCH2-0 flags of the AN0CTR0 register to “010” to set “channel 2) to the last channel to be converted. Set the AN0OFF flag of the AN0CTR0 register to “1” to set operation mode to the power-down mode flag. *After shifted to operation mode, more than 100nsec wait time is necessary until A/D conversion start.
(5) Set the AD0: Select the AD0 start trigger ADST0(0x0000A408) bp2-0: AD0ST2-0=010	(5) Set the AD0ST2-0 flags of the A/D start selection register (ADST0) to “010” to start the A/D conversion by the timer 12 compare A interrupt.
(6) Set the external trigger conversion start enabled AN0CTR0(0x0000A400) bp5: AN0TRG=1	(6) Set the AN0TRG flag of the AN0CTR0 register to “1” to set conversion start by the timer 11 compare A interrupt.
(7) Set the AD0: Set the interrupt level G26ICR(0x00008968) bp14-12: G26LV2-0=100	(7) Set the AD0 complete interrupt level by the G26LV2-0 flags of the G26ICR register. When the interrupt request flag is already set, clear the request flag.
(8) Set the AD0: Enable the interrupt G26ICR(0x00008968) bp8: G26IE0=1	(8) Set the G26IE0 flag of the G26ICR register to “1” to enable the AD0 complete interrupt.
(9) Set the timer 12: Select the cycle TM12CA(0x0000A288)=0x752F	(9) Set the cycle to the timer 12 compare/capture A register (TM12CA). Due to 30000 dividing, the set value is 29999 (0x752F).
(10) Set the timer 12: Set the count clock source TM12MD(0x0000A280) bp2-0: TMCK2-0=000	(10) Select the count clock source (IOCLK) by the TMCK2-0 flags of the TM12MD register.
(11) Set the timer 12: Select up/down TM12MD(0x0000A280) bp9-8: TMUD1-0=00	(11) Select the timer up counting by the TMUD1-0 flags of the TM12MD register.
(12) Set the timer 12: Set the counter clear enabled TM12MD(0x0000A280) bp11: TMCLE=1	(12) Set the TMCLE flag of the TM12MD register to “1” to enable the clear operation of the TM11BC counter. When the TM12CA register and the TM12BC counter match, the TM12BC counter is cleared.

Setup Procedure	Description
(13) Set the timer 12: Select the timer compare/ capture A operation mode TM12MDA(0x0000A284) bp7-6: TMAM1-0=00	(13) Set the compare register (double buffer) to the function of the timer 12 compare/capture register by the TMAM1-0 flags of the timer 12 compare/capture A mode register (TM12MDA).
(14) Set the timer 12: Initialize the timer 12 TM12MD(0x0000A280) bp6: TMLDE=1	(14) Set the TMLDE flag of the TM11MD register to “1” to initialize the timer 12. The value of the compare register buffer is loaded into the TM12CA register. Reset the TMLDE flag to “0” after setting.
(15) Set the timer 12: Start the timer operation TM12MD(0x0000A280) bp7: TMCNE=1	(15) Set the TMCNE flag of the TM12MD register to “1” to operate the timer 8.
(16) Set the AD0: Read the A/D value AN0BUF00 (0x0000A410) AN0BUF01 (0x0000A414) AN0BUF02 (0x0000A418)	(16) A/D0 conversion data buffer 0 and 1 (ANOBUF0, ANOBUF1) are read by the AD0 complete interrupt processing after A/D conversion ends .

When the timer 12 operation is started, A/D conversion is started every 1 ms. When A/D conversion is completed with channel 0 and 1, the AD0 complete interrupt is generated.

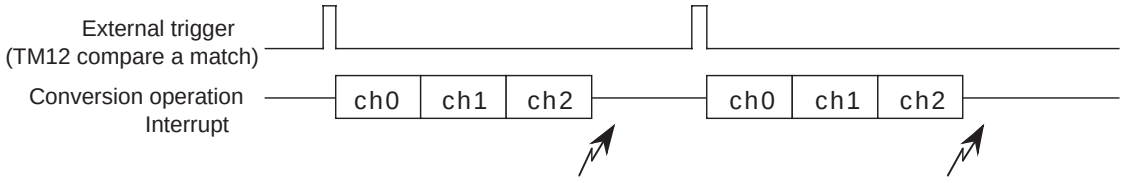


Figure:14.3.8 A/D Conversion Timing (0 to 2 Channel Converted Once Each)

■ Setup Example of Multiple Channel A/D Converter Simultaneous Conversion Using PWM as External trigger

A/D converter result can be obtained with feeding analog voltage by the ADIN00 and ADIN02 to activate A/D0 and A/D1 byPWM0 and by the ADIN01 and ADIN03 pins to activate A/D0 and A/D1 by PWM1. Conversion is performed regularly PWM0 underflow.

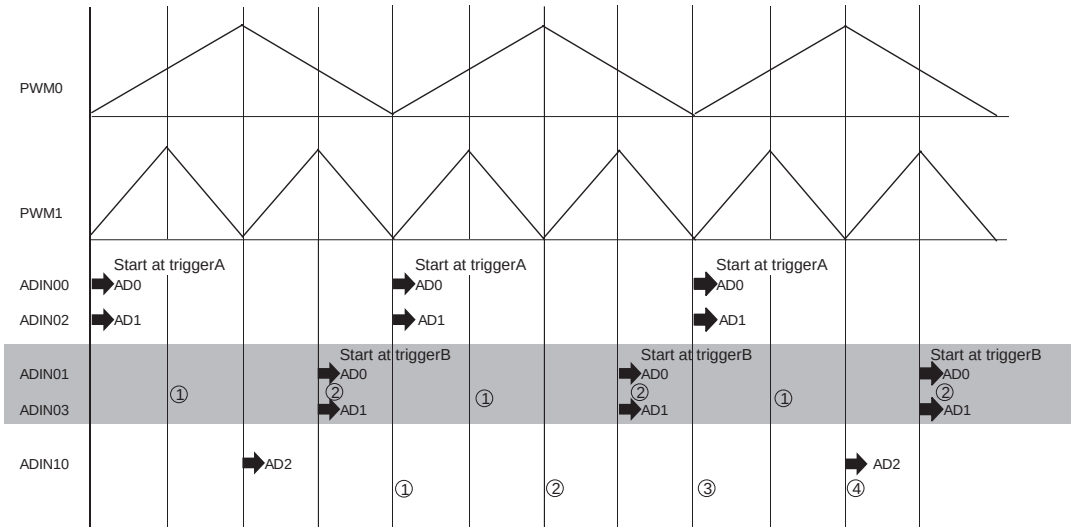


Figure:14.3.9 1-channel A/D conversion

Table:14.3.7 1 Conditions for Channel A/D Conversion

Setting item	Description
Input pin	ADIN00 pin ADIN01 pin ADIN02 pin ADIN03 pin ADIN10 pin
Operation mode	Any single channel /one-time conversion
A/D converter start trigger	PWM0, 1 overflow/underflow
A/D converter start cycle	Setting by PWM0, 1 cycles and the number of counts of the A/D start trigger count register
IOCLK	30MHz

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the AD0: Stop the A/D converter operation AN0CTR0(0x0000A400) bp7: AN0EN=0 bp5: AN0TRG=0 Set the AD1: Stop the A/D converter operation AN1CTR0(0x0000A440) bp7: AN1EN=0 bp5: AN1TRG=0 Set the AD2: Stop the A/D converter operation AN2CTR0(0x0000A480) bp7: AN2EN=0 bp5: AN2TRG=0	(1) Set the AN0EN flag and the AN0TRG flag of the A/D0 conversion control register 0 (AN0CTR0) to “0” to stop the A/D conversion. Set the AN1EN flag and the AN1TRG flag of the A/D1 conversion control register 0 (AN1CTR0) to “0” to stop the A/D conversion. Set the AN2EN flag and the AN2TRG flag of the A/D2 conversion control register 0 (AN2CTR0) to “0” to stop the A/D conversion.
(2) Set the AD0: Disable the AD0 complete interrupt G26ICR(0x00008968) bp8: G26IE0=0 bp9: G26IE1=0 Set the AD1: Disable the AD1 complete interrupt G27ICR(0x0000896C) bp8: G27IE0=0 bp9: G27IE1=0 Set the AD2: Disable the AD2 complete interrupt G28ICR(0x00008970) bp8: G28IE0=0	(2) Set the IE flags of the G26ICR, G27ICR and G28ICR registers to “0” to disable the AD0, 1 and 2 conversion complete interrupts.
(3) Set the PWM0 and 1	(3) Set PWM0 and 1. * Do not execute PWM start at this point. PWMMD0 (0x0000A300), PWMMD1 (0x0000A330) bp: TCENn=0

Setup Procedure	Description
(4) Set the AD0: Set the AN0CTR0 register Set the operation mode AN0CTR0(0x0000A400) bp1-0: AN0MD1-0=01 Set the conversion clock AN0CTR0(0x0000A400) bp4-2: AN0CK2-0=010 Set the external trigger A conversion start enabled AN0CTR0(0x0000A400) bp5: AN0TRG=1 Set the conversion channel (trigger factor A) AN0CTR0(0x0000A400) bp10-8: AN0CH2-0=000 Set the power-down mode AN0CTR0(0x0000A400) bp6: AN0OFF=1 Set the external trigger B conversion start enabled AN0CTR1(0x0000A404) bp6: AN0TRGB=1 Set the conversion channel (trigger factor B) AN0CTR1(0x0000A404) bp10-8: AN0CH0B2-0=001 Set the sample/hold cycle AN0CTR1(0x0000A404) bp5-4: AN0SHC1-0=10	(4) Set the AN0MD1-0 flags of the AN0CTR0 register to “00” to set “any channels/one-time conversion for each” to operation mode. Set the AN0CK2-0 flags of the AN0CTR0 register to “010I” to set 3 dividing of IOCLK to the conversion clock. Set the AN0TRG flag of the AN0CTR0 register to “1” to enable the external trigger factor A starting. Set the AN0CH2-0 flags of the AN0CTR0 register to “000” to set “channel 0” to the conversion channel of the external trigger factor A. Set the AN0OFF flag of the AN0CTR0 register to “1” to set operation mode to the power-down mode flag. *After shifted to operation mode, more than 100nsec wait time is necessary until A/D conversion stars. Set the AN0TRGB flag of the AN0CTR1 register to “1” to enable the external trigger factor B starting. Set the AN0CH0B2-0 flags of the AN0CTR1 register to “001” to set “channel 1” to the conversion channel of the external trigger factor B.
(5) Set the AD0: Set the ADST0 register Select the external trigger factor A ADST0(0x0000A408) bp2-0: AD0AST2-0=000 Select the external trigger factor B ADST0(0x0000A408) bp6-4: AD0BST2-0=100	(5) Set the AD0AST2-0 flags of the A/D0 start trigger selection register (ADST0) to “000” to set the PWM0 underflow to start factor A. Set the AD0BST2-0 flags of the A/D0 start trigger selection register (ADST0) to “000” to set the PWM1 over to start factor B.
(6) Set the AD0: Set the AD0CTREGB register AD0CTREGB(0x0000A40D) bp7-4: AD0BCNT3I-0I=0001 bp3-0: AD0BCNT3-0=0001	(6) Set the AN0BCT3I-0I flags to “0001” to start AD conversion after the first time the trigger factor B is counted. Set the AN0BCT3-0 flags to “0001” to start AD conversion every two times the trigger factor B is generated.

Setup Procedure	Description
(7) Set the AD1: Set the AN1CTR0 register Set the operation mode AN1CTR0(0x0000A440) bp1-0: AN1MD1-0=00 Set the conversion clock AN1CTR0(0x0000A440) bp4-2: AN1CK2-0=010 Set the external trigger A conversion start enabled AN1CTR0(0x0000A440) bp5: AN1TRG=1 Set the conversion channel (trigger factor A) AN1CTR0(0x0000A440) bp10-8: AN1CH2-0=000 Set the power-down mode AN1CTR0(0x0000A440) bp6: AN1OFF=1 Set the external trigger B conversion start enabled AN1CTR1(0x0000A444) bp6: AN1TRGB=1 Set the conversion channel (trigger factor B) AN1CTR1(0x0000A444) bp10-8: AN1CH0B2-0=001 Set the sample/hold cycle AN1CTR1(0x0000A444) bp5-4: AN1SHC1-0=10	(7) Set the AN1MD1-0 flags of the AN1CTR0 register to “00” to set “any channels/one-time conversion for each” to operation mode. Set the AN1CK2-0 flags of the AN1CTR0 register to “010l” to set 3 dividing of IOCLK to the conversion clock. Set the AN1TRG flag of the AN1CTR0 register to “1” to enable the external trigger factor A starting. Set the AN1CH2-0 flags of the AN1CTR0 register to “000” to set “channel 2” to the conversion channel of the external trigger factor A. Set the AN1OFF flag of the AN1CTR0 register to “1” to set operation mode to the power-down mode flag. *After shifted to operation mode, more than 100nsec wait time is necessary until A/D conversion starts. Set the AN1TRGB flag of the AN1CTR1 register to “1” to enable the external trigger factor B starting. Set the AN1CH0B2-0 flags of the AN1CTR1 register to “001” to set “channel 3” to the conversion channel of the external trigger factor B.
(8) Set the AD1: Set the ADST1 register Select the external trigger factor A ADST1(0x0000A448) bp2-0: AD1AST2-0=000 Select the external trigger factor B ADST1(0x0000A448) bp6-4: AD1BST2-0=100	(8) Set the AD1AST2-0 flags of the A/D1 start trigger selection register (ADST1) to “000” to set the PWM0 underflow to start factor A. Set the AD1BST2-0 flags of the A/D1 start trigger selection register (ADST1) to “000” to set the PWM1 over to start factor B.
(9) Set the AD1: Set the AD1CTREGB register AD1CTREGB(0x0000A44D) bp7-4: AD1BCNT3I-0I=0001 bp3-0: AD1BCNT3-0=0001	(9) Set the AN1BCT3I-0I flags to “0001” to start AD conversion after the first time of the trigger factor B is counted. Set the AN0BCT3-0 flags to “0001” to start AD conversion every two times the trigger factor B is generated.

Setup Procedure	Description
(10) Set the AD2: Set the AN2CTR0 register Set the operation mode AN2CTR0(0x0000A480) bp1-0: AN2MD1-0=00 Set the conversion clock AN2CTR0(0x0000A480) bp4-2: AN2CK2-0=010 Set the external trigger A conversion start enabled AN2CTR0(0x0000A480) bp5: AN2TRG=1 Set the conversion channel AN2CTR0(0x0000A480) bp101-8: AN2CH3-0=0100 Set the power-down mode AN2CTR0(0x0000A480) bp6: AN2OFF=1 Set the sample/hold cycle AN2CTR1(0x0000A484) bp5-4: AN2SHC1-0=10	(10) Set the AN2MD1-0 flags of the AN2CTR0 register to “00” to set “any channels/one-time conversion for each” to operation mode. Set the AN2CK2-0 flags of the AN2CTR0 register to “010I” to set 3 dividing of IOCLK to the conversion clock. Set the AN2TRG flag of the AN2CTR0 register to “1” to enable the external trigger factor A starting. Set the AN2CH3-0 flags of the AN2CTR0 register to “0100” to set “channel10” to the conversion channel of the external trigger factor A. Set the AN2OFF flag of the AN2CTR0 register to “1” to set operation mode to the power-down mode flag. *After shifted to operation mode, more than 100nsec wait time is necessary until A/D conversion start.s
(11) Set the AD2: Set the ADST2 register Select the external trigger factor ADST2(0x0000A488) bp2-0: AD2ST2-0=101	(11) Set the AD2ST2-0 flags of the A/D2 start trigger selection register (ADST2) to “101” to set the PWM1 underflow to start factor.
(12) Set the AD2: Set the AN2CTREGA register AN2CTREGA(0x0000A48C) bp7-4: AN2ACNT3I-0I=0000 bp3-0: AN2ACNT3-0=0011	(12) Set the AN2ACNT3I-0I flags to “0000” to start AD conversion after the first time of the trigger factor is counted. Set the AN2ACNT3-0 flags to “0011” to start AD conversion every time the trigger factor is generated two times.
(13) Set the AD0: Disable the AD0 complete interrupt G26ICR(0x00008968) bp8: G26IE0=1 bp9: G26IE1=1 Set the AD2: Disable the AD2 complete interrupt G28ICR(0x00008970) bp8: G28IE0=1	(13) Set the IE flags of the G26ICR and G28ICR registers to “0” to enable the AD0 and 2 conversion complete interrupts. *In this set-up example, AD1 and AD0 interrupts are generated at the same time; so, the interrupt of AD1 is disabled at this point.
(14) Start the PWM0 and 1 PWMMD0(0x0000A300) bp1: TCEN0=1 PWMMD1(0x0000A330) bp1: TCEN1=1	(14) Start the PWM0 and 1.
(15) Read the A/D value AN0BUF0 (0x0000A410) AN1BUF2 (0x0000A450)	(15) Read the A/D0 conversion data buffer 00 and A/D1 conversion data buffer 02 (AN0BUF00, AN1BUF02) by the AD0 complete interrupt processing after the A/D0 conversion is completed.

Setup Procedure	Description
(16) Read the A/D value AN0BUF0B (0x0000A430) AN1BUF0B (0x0000A470)	(16) Read the A/D0 conversion data buffer 0B and A/D1 conversion data buffer 0B (AN0BUF0B, AN1BUF0B) by the AD0 complete B interrupt processing after the A/D0 conversion is completed.
(17) Read the A/D value AN2BUF10 (0x0000A4A0)	(17) Read the A/D2 conversion data buffer 10 (AN2BUF10) by the AD2 complete B interrupt processing after the A/D2 conversion is completed..

Do not start the same AD conversion using the external trigger B during AD conversion. Conversion result is not stored properly. AD conversion start timing should be well considered in using the external trigger B.

14.3.3 Cautions

A/D converter can be damaged by noise easily; therefore, anti-noise measures should be taken adequately.

The following shows cautions for anti-noise measures and the recommended circuit when A/D converter is used.

■ Anti-noise Measures

To A/D input (analog input pin ADINn), add condenser near the VSS pins of micro controller.

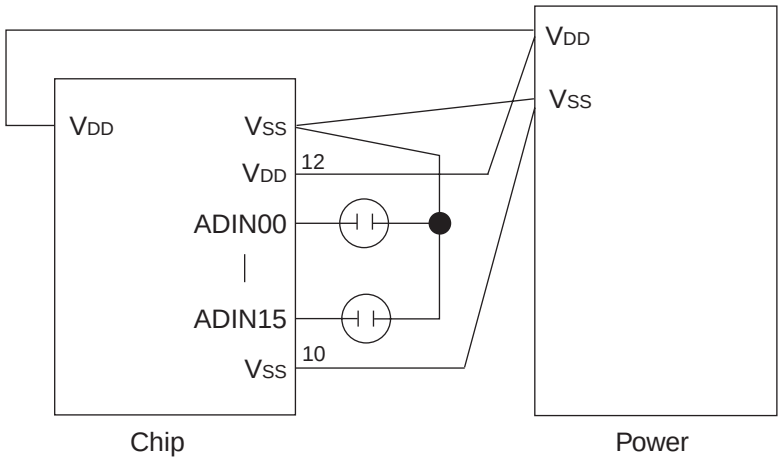


Figure:14.3.10 A/D Converter Recommended Example

■ Recommended Circuit

For high precision of A/D conversion, the following cautions on A/D converter should be kept.

1. The input impedance R of A/D input pin should be under 500 kΩ, *1 and the external capacitor C which is more than 1000 pF, under 1 µF *1 should be connected to it.
2. The A/D conversion frequency should be set in regard to R, C.
3. At the A/D conversion, if the output level of microcontroller is changed, or the peripheral added circuit is switched to ON/OFF, the A/D conversion could work wrongly, as the analog input pins and power pins can not be fixed. At the setup checking confirm the waveform of analog input pins.

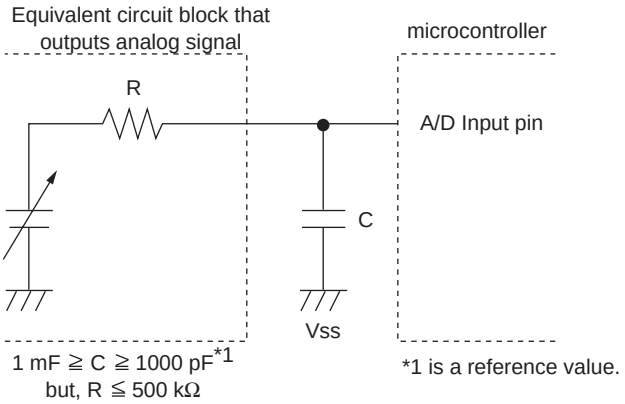


Figure:14.3.11 Recommended Circuit

Chapter 15 Regulator

15

15.1 Overview

The regulator converts 5 V VDD which is supplied externally and supplies it into the internal circuit of the microcontroller.

15.1.1 Setup

Insert a capacitor which is more than 10 µF between each VDD pin and VSS. And insert a capacitor which is more then 1 µF between each VDD2 and VSS. And insert a capacitor which is more then 2 µF between VDD3 and VSS. A capacitor should be near each pin.

It is recommended that total capacitance between all of the VDD and VSS is more than 10-times sum of capacitance between all of the VDD2 and VSS plus capacitance etween VDD3 and VSS.

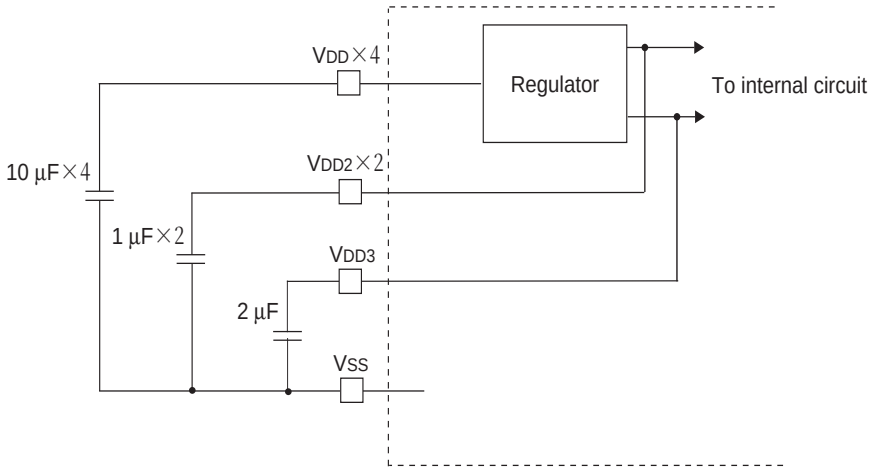


Figure:15.1.1 Setting Regulator

15.1.2 Operation

The regulator operates by application of power.

Use the regulator output as power supply only for the microcontroller.

Chapter 16 Appendix

16

16.1 Cautions for Circuit Setup

16.1.1 General Usage

■ Connection of V_{DD} pin and V_{SS} pin

All of the VDD and VSS pins should be connected directly to the power supply and GND in the external. Put them on printed circuit board after the location of LSI (package) pin is confirmed. Connection error may lead a fusion and breakdown of a microcontroller.

■ Cautions for Operation

1. If you install the product close to high-field emissions (under the cathode ray tube, etc.), shield the package surface to ensure normal performance.
2. Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, improper operation could be occurred.
3. Operation voltage should be also well considered. Each product has different operating range.
    - If the operation voltage is over the operating range, duration of the product could be shortened.
    - If the operation voltage is below the operating range, improper operation could be occurred.

16.1.2 Unused Pins

■ Unused Functions

Disable all unused functions.

■ Unused Pin (Only for Output)

Leave all unused output-dedicated pins open.

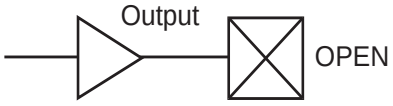


Figure:16.1.1 Unused pin (Output Pins)

■ Unused Pin (Only for Input)

Insert some 10 kΩ resistor to unused pins (only for input) to pull up or down.

If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

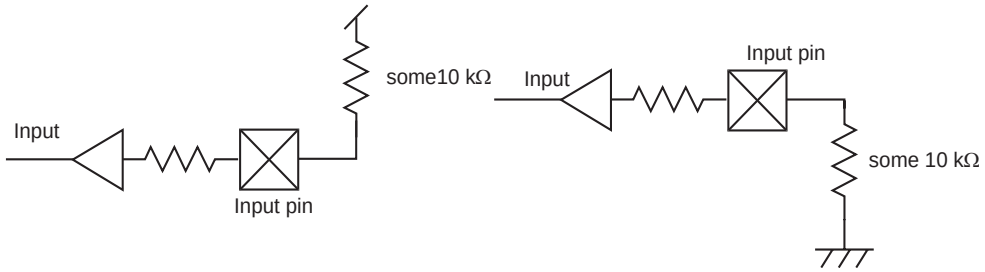


Figure:16.1.2 Unused Pins (Only for Input)

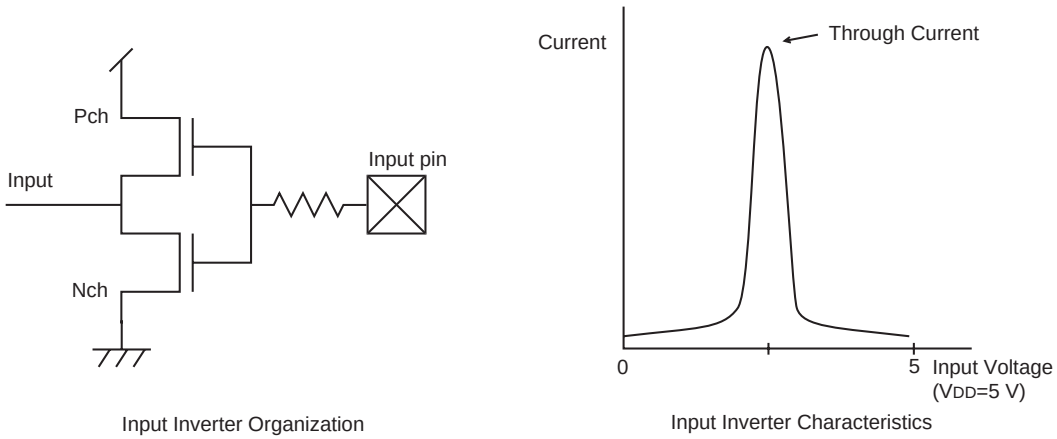


Figure:16.1.3 Input Inverter Organization and Characteristics

■ Unused Pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor: output off) at reset, to stabilize input, set some 10 kΩ resistor to pull up or down. If the output is on at reset, set them open. Do not switch between input and output by software.

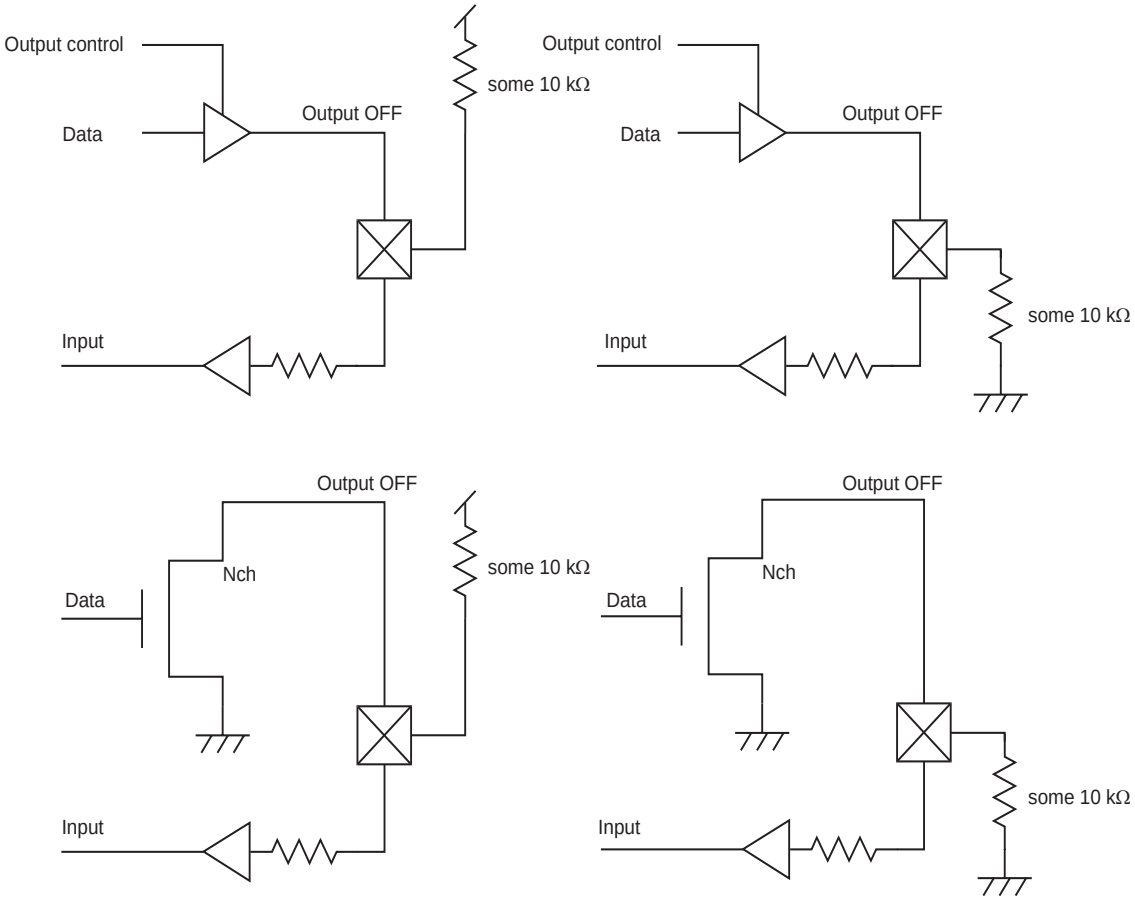


Figure:16.1.4 Unused I/O Pins (High Impedance Output at Reset)

16.1.3 Power Supply

■ The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed, the destruction of microcontroller by a large current flow could be occurred.

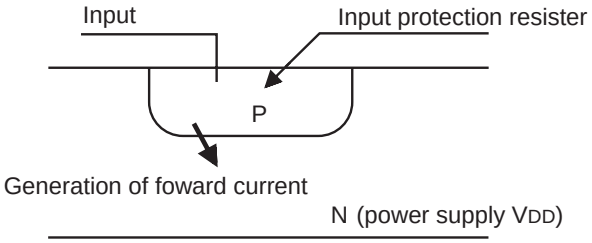


Figure:16.1.5 Power Supply and Input Pin Voltage

■ The Relation between Power Supply and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising, in order to be recognized as a reset signal.

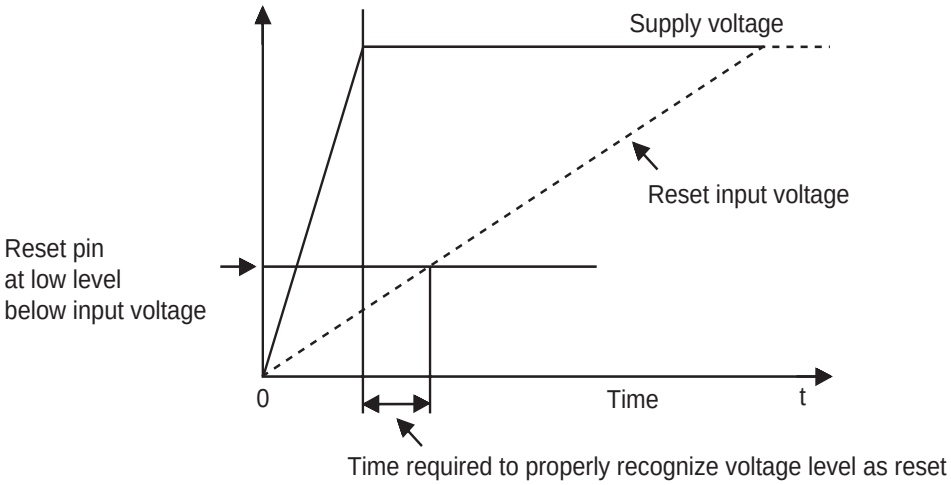


Figure:16.1.6 Power Supply and Reset Input Voltage

16.1.4 Power Supply Circuit

■ Cautions for Setting Circuit with V_{DD}

The MOS logic such a microcontroller is high speed and high density; so, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver.

Figure: 16.1.7 shows an example for a circuit with VDD (Emitter follower type).

■ An Example for a Circuit with VDD (Emitter Follower Type)

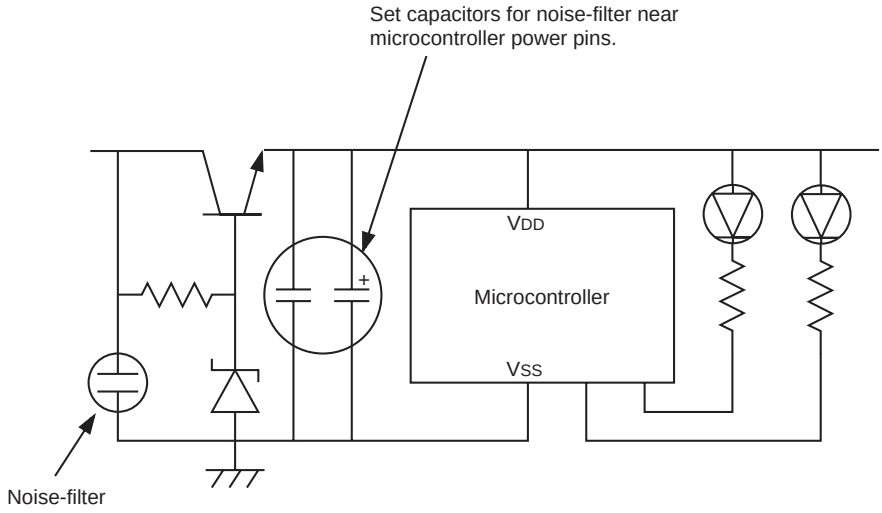


Figure:16.1.7 An Example for a Circuit of VDD Supply (Emitter Follower Type)

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
MOV	MOV Dm,Dn	Dm → Dn	-	-	-	-	1	1	S0	1000	DmDn													
	MOV Dm,An	Dm → An	-	-	-	-	2	1	D0	1111	0001	1110	DmAn											
	MOV Am,Dn	Am → Dn	-	-	-	-	2	1	D0	1111	0001	1101	AmDn											
	MOV Am,An	Am → An	-	-	-	-	1	1	S0	1001	AmAn													
	MOV SP,An	SP → An	-	-	-	-	1	1	S0	0011	11An													
	MOV Am,SP	An → SP	-	-	-	-	2	1	D0	1111	0010	1111	Am00											
	MOV PSW,Dn	PSW(zero_ext) → Dn	-	-	-	-	2	1	D0	1111	0010	1110	01Dn											
	MOV Dm,PSW	Dm → PSW	●	●	●	●	2	1	D0	1111	0010	1111	Dm11											
	MOV MDR,Dn	MDR → Dn	-	-	-	-	2	1	D0	1111	0010	1110	00Dn											
	MOV Dm,MDR	Dm → MDR	-	-	-	-	2	1	D0	1111	0010	1111	Dm11											
	MOV (Am),Dn	mem32(Am) → Dn	-	-	-	-	1	1	S0	0111	DnAm													
	MOV (d8,Am),Dn	mem32(d8(sign_ext)+Am) → Dn	-	-	-	-	3	1	D1	1111	1000	0000	DnAm	<d8.	...>									
	MOV (d16,Am),Dn	mem32(d16(sign_ext)+Am) → Dn	-	-	-	-	4	1	D2	1111	1010	0000	DnAm	<d16	....	....	....>							
	MOV (d32,Am),Dn	mem32(d32+Am) → Dn	-	-	-	-	6	2	D4	1111	1100	0000	DnAm	<d32	....	....	....	....	....	....	....>			
	MOV (d8,SP),Dn	mem32(d8(zero_ext)+SP) → Dn	-	-	-	-	2	1	S1	0101	10Dn	<d8	....>											
	MOV (d16,SP),Dn	mem32(d16(zero_ext)+SP) → Dn	-	-	-	-	4	1	D2	1111	1010	1011	01Dn	<d16	....	....	....>							
	MOV (d32,SP),Dn	mem32(d32+SP) → Dn	-	-	-	-	6	2	D4	1111	1100	1011	01Dn	<d32	....	....	....	....	....	....	....>			
	MOV (Di,Am),Dn	mem32(Di+Am) → Dn	-	-	-	-	2	1	D0	1111	0011	00Dn	DiAm											
	MOV (abs16),Dn	mem32(abs16(zero_ext)) → Dn	-	-	-	-	3	1	S2	0011	00Dn	<abs16....	....	....>										
	MOV (abs32),Dn	mem32(abs32) → Dn	-	-	-	-	6	2	D4	1111	1100	1010	01Dn	<abs32....	....	....	....	....	....	....	....>			
	MOV (Am),An	mem32(Am) → An	-	-	-	-	2	1	D0	1111	0000	0000	AnAm											
	MOV (d8,Am),An	mem32(d8(sign_ext)+Am) → An	-	-	-	-	3	1	D1	1111	1000	0010	AnAm	<d8	....>									
	MOV (d16,Am),An	mem32(d16(sign_ext)+Am) → An	-	-	-	-	4	1	D2	1111	1010	0010	AnAm	<d16	....	....	....>							
	MOV (d32,Am),An	mem32(d32+Am) → An	-	-	-	-	6	2	D4	1111	1100	0010	AnAm	<d32	....	....	....	....	....	....	....>			
	MOV (d8,SP),An	mem32(d8(zero_ext)+SP) → An	-	-	-	-	2	1	S1	0101	11An	<d8	....>											
	MOV (d16,SP),An	mem32(d16(zero_ext)+SP) → An	-	-	-	-	4	1	D2	1111	1010	1011	00An	<d16	....	....	....>							
	MOV (d32,SP),An	mem32(d32+SP) → An	-	-	-	-	6	2	D4	1111	1100	1011	00An	<d32	....	....	.....	....	....	....	....>			
	MOV (Di,Am),An	mem32(Di+Am → An	-	-	-	-	2	1	D0	1111	0011	10An	DiAm											
	MOV (abs16),An	mem32(abs16(zero_ext)) → An	-	-	-	-	4	1	D2	1111	1010	1010	00An	<abs16....	....	....>								
	MOV (abs32),An	mem32(abs32) → An	-	-	-	-	6	2	D4	1111	1100	1010	00An	<abs32....	....	....	....	....	....	....	....>			
	MOV (d8,Am),SP	mem32(d8(sign_ext)+Am) → SP	-	-	-	-	3	1	D1	1111	1000	1111	00Am	<d8	....>									
	MOV Dm,(An)	Dm → mem32(An)	-	-	-	-	1	1	S0	0110	DmAn													
	MOV Dm,(d8,An)	Dm → mem32(d8(sign_ext)+An)	-	-	-	-	3	1	D1	1111	1000	0111	DmAn	<d8	....>									
	MOV Dm,(d16,An)	Dm → mem32(d16(sign_ext)+An)	-	-	-	-	4	1	D2	1111	1010	0001	DmAn	<d16	....	....	....>							
	MOV Dm,(d32,An)	Dm → mem32(d32+An)	-	-	-	-	6	2	D4	1111	1100	0001	DmAn	<d32	....	....	....	....	....	....	....>			
	MOV Dm,(d8,SP)	Dm → mem32(d8(zero_ext)+SP)	-	-	-	-	2	1	S1	0100	Dm10	<d8	....>											
	MOV Dm,(d16,SP)	Dm → mem32(d16(zero_ext)+SP)	-	-	-	-	4	1	D2	1111	1010	1001	Dm01	<d16	....	....	....>							
	MOV Dm,(d32,SP)	Dm → mem32(d32+SP)	-	-	-	-	6	2	D4	1111	1100	1001	Dm01	<d32.	....	....	....	....	....	....	....>			
	MOV Dm,(Di,An)	Dm → mem32(Di+An)	-	-	-	-	2	2	D0	1111	0011	01Dm	DiAn											
	MOV Dm,(abs16)	Dm → mem32(abs16(zero_ext))	-	-	-	-	3	1	S2	0000	Dm01	<abs16....	....	....>										
	MOV Dm,(abs32)	Dm → mem32(abs32)	-	-	-	-	6	2	D4	1111	1100	1000	Dm01	<abs32....	....	....	....	....	....	....	....>			

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
MOV	MOV Am,(An)	Am → mem32(An)	-	-	-	-	2	1	D0	1111	0000	0001	AmAn											
	MOV Am,(d8,An)	Am → mem32(d8(sign_ext)+An)	-	-	-	-	3	1	D1	1111	1000	0011	AmAn	<d8	....>									
	MOV Am,(d16,An)	Am → mem32(d16(sign_ext)+An)	-	-	-	-	4	1	D2	1111	1010	0011	AmAn	<d16	....	....	....>							
	MOV Am,(d32,An)	Am → mem32(d32+An)	-	-	-	-	6	2	D4	1111	1100	0011	AmAn	<d32	....	....	....	....	....	....	....>			
	MOV Am,(d8,SP)	Am → mem32(d8(zero_ext)+SP)	-	-	-	-	2	1	S1	0100	Am11	<d8	....>											
	MOV Am,(d16,SP)	Am → mem32(d16(zero_ext)+SP)	-	-	-	-	4	1	D2	1111	1010	1001	Am00	<d16	....	....	....>							
	MOV Am,(d32,SP)	Am → mem32(d32+SP)	-	-	-	-	6	2	D4	1111	1100	1001	Am00	<d32	....	....	....	....	....	....	....>			
	MOV Am,(Di,An)	Am → mem32(Di+An)	-	-	-	-	2	2	D0	1111	0011	11Am	DiAn											
	MOV Am,(abs16)	Am → mem32(abs16(zero_ext))	-	-	-	-	4	1	D2	1111	1010	1000	Am00	<abs16...	....	....	....>							
	MOV Am,(abs32)	Am → mem32(abs32)	-	-	-	-	6	2	D4	1111	1100	1000	Am00	<abs32...	....	....	....	....	....	....	....>			
	MOV SP,(d8,An)	SP → mem32(d8(sign_ext)+An)	-	-	-	-	3	1	D1	1111	1000	1111	01An	<d8	....>									
	MOV imm8,Dn	imm8(sign_ext) → Dn	-	-	-	-	2	1	S1	1000	DnDn	<imm8	...>											
	MOV imm16,Dn	imm16(sign_ext) → Dn	-	-	-	-	3	1	S2	0010	11Dn	<imm16	....	....	....>									
	MOV imm32,Dn	imm32 → Dn	-	-	-	-	6	2	D4	1111	1100	1100	10Dn	<imm32..	....	....	....	....	....	....	....>			
	MOV imm8,An	imm8(zero_ext] → An	-	-	-	-	2	1	S1	1001	AnAn	<imm8	....>											
	MOV imm16,An	imm16(zero_ext) → An	-	-	-	-	3	1	S2	0010	01An	<imm16....	....	....	....>									
	MOV imm32,An	imm32 → An	-	-	-	-	6	2	D4	1111	1100	1101	11An	<imm32..	....	....	....	....	....	....	....>			
MOVBU	MOVBU (Am),Dn	mem8(Am)(zero_ext) → Dn	-	-	-	-	2	1	D0	1111	0000	0100	DnAm											
	MOVBU (d8,Am),Dn	mem8(d8(sign_ext)+Am)(zero_ext) → Dn	-	-	-	-	3	1	D1	1111	1000	0100	DnAm	<d8	....>									
	MOVBU (d16,Am),Dn	mem8(d16(sign_ext)+Am)(zero_ext) → Dn	-	-	-	-	4	1	D2	1111	1010	0100	DnAm	<d16	....	....	....>							
	MOVBU (d32,Am),Dn	mem8(d32+Am)(zero_ext] → Dn	-	-	-	-	6	2	D4	1111	1100	0100	DnAm	<d32	....	....	....	....	....	....	....>			
	MOVBU (d8,SP),Dn	mem8(d8(zero_ext)+SP)(zero_ext) → Dn	-	-	-	-	3	1	D1	1111	1000	1011	10Dn	<d8	....>									
	MOVBU (d16,SP),Dn	mem8(d16(zero_ext)+SP)(zero_ext) → Dn	-	-	-	-	4	1	D2	1111	1010	1011	10Dn	<d16	....	....	....>							
	MOVBU (d32,SP),Dn	mem8(d32+SP)(zero_ext) → Dn	-	-	-	-	6	2	D4	1111	1100	1011	10Dn	<d32	....	....	....	....	....	....	....>			
	MOVBU (Di,Am),Dn	mem8(Di+Am)(zero_ext) → Dn	-	-	-	-	2	1	D0	1111	0100	00Dn	DiAm											
	MOVBU (abs16),Dn	mem8(abs16(zero_ext))(zero_ext] → Dn	-	-	-	-	3	1	S2	0011	01Dn	<abs16	....	....	....>									
	MOVBU (abs32),Dn	mem8(abs32)(zero_ext) → Dn	-	-	-	-	6	2	D4	1111	1100	1010	10Dn	<abs32	....	....	....	....	....	....	....>			
	MOVBU Dm,(An)	Dm → mem8(An)	-	-	-	-	2	1	D0	1111	0000	0101	DmAn											
	MOVBU Dm,(d8,An)	Dm → mem8(d8+An)	-	-	-	-	3	1	D1	1111	1000	0101	DmAn	<d8	....>									
	MOVBU Dm,(d16,An)	Dm → mem8(d16+An)	-	-	-	-	4	1	D2	1111	1010	0101	DmAn	<d16	....	....	....>							
	MOVBU Dm,(d32,An)	Dm → mem8(d32+An)	-	-	-	-	6	2	D4	1111	1100	0101	DmAn	<d32	....	....	....	....	....	....	....>			
	MOVBU Dm,(d8,SP)	Dm → mem8(d8(zero_ext)+SP)	-	-	-	-	3	1	D1	1111	1000	1001	Dm10	<d8	....>									
	MOVBU Dm,(d16,SP)	Dm → mem8(d16(zero_ext)+SP)	-	-	-	-	4	1	D2	1111	1010	1001	Dm10	<d16	....	....	....>							
	MOVBU Dm,(d32,SP)	Dm → mem8(d32+SP)	-	-	-	-	6	2	D4	1111	1100	1001	Dm10	<d32	....	....	....	....	....	....	....>			
	MOVBU Dm,(Di,An)	Dm → mem8(Di+An)	-	-	-	-	2	2	D0	1111	0100	01Dm	DiAn											
	MOVBU Dm,(abs16)	Dm → mem8(abs16(zero_ext))	-	-	-	-	3	1	S2	0000	Dm10	<abs16	....	....	....>									
	MOVBU Dm,(abs32)	Dm → mem8(abs32)	-	-	-	-	6	2	D4	1111	1100	1000	Dm10	<abs32	....	....	....	....	....	....	....>			

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
MOVB	MOVB (Am),Dn	mem8(Am)(sign_ext) → Dn	-	-	-	-	3	2																
	MOVB (d8,Am),Dn	mem8(d8(sign_ext)+Am)(sign_ext) → Dn	-	-	-	-	4	2																
	MOVB (d16,Am),Dn	mem8(d16(sign_ext)+Am)(sign_ext) → Dn	-	-	-	-	5	2																
	MOVB (d32,Am),Dn	mem8(d32+Am)(sign_ext) → Dn	-	-	-	-	7	3																
	MOVB (d8,SP),Dn	mem8(d8(zero_ext)+SP)(sign_ext) → Dn	-	-	-	-	4	2																
	MOVB (d16,SP),Dn	mem8(d16(zero_ext)+SP)(sign_ext) → Dn	-	-	-	-	5	2																
	MOVB (d32,SP),Dn	mem8(d32+SP)(sign_ext) → Dn	-	-	-	-	7	3																
	MOVB (Di,Am),Dn	mem8(Di+Am)(sign_ext) → Dn	-	-	-	-	3	2																
	MOVB (abs16),Dn	mem8(abs16(zero_ext))(sign_ext) → Dn	-	-	-	-	4	2																
	MOVB (abs32),Dn	mem8(abs32)(sign_ext) → Dn	-	-	-	-	7	3																
	MOVB Dm,(An)	Dm → mem8(An)	-	-	-	-	2	1																
	MOVB Dm,(d8,An)	Dm → mem8(d8(sign_ext)+An)	-	-	-	-	3	1																
	MOVB Dm,(d16,An)	Dm → mem8(d16(sign_ext)+An)	-	-	-	-	4	1																
	MOVB Dm,(d32,An)	Dm → mem8(d32+An)	-	-	-	-	6	2																
	MOVB Dm,(d8,SP)	Dm → mem8(d8(zero_ext)+SP)	-	-	-	-	3	1																
	MOVB Dm,(d16,SP)	Dm → mem8(d16(zero_ext)+SP)	-	-	-	-	4	1																
	MOVB Dm,(d32,SP)	Dm → mem8(d32+SP)	-	-	-	-	6	2																
	MOVB Dm,(Di,An)	Dm → mem8(Di+An)	-	-	-	-	2	2																
	MOVB Dm,(abs16)	Dm → mem8(abs16(zero_ext))	-	-	-	-	3	1																
	MOVB Dm,(abs32)	Dm → mem8(abs32)	-	-	-	-	6	2																
MOVHU	MOVHU (Am),Dn	mem16(Am)(zero_ext) → Dn	-	-	-	-	2	1	D0	1111	0000	0110	DnAm											
	MOVHU (d8,Am),Dn	mem16(d8(sign_ext)+Am)(zero_ext) → Dn	-	-	-	-	3	1	D1	1111	1000	0110	DnAm	<d8	....>									
	MOVHU (d16,Am),Dn	mem16(d16(sign_ext)+Am)(zero_ext) → Dn	-	-	-	-	4	1	D2	1111	1010	0110	DnAm	<d16	....	....	....>							
	MOVHU (d32,Am),Dn	mem16(d32+Am)(zero_ext) → Dn	-	-	-	-	6	2	D4	1111	1100	0110	DnAm	<d32	....	....	....	....	....	....	....>			
	MOVHU (d8,SP),Dn	mem16(d8(zero_ext)+SP)(zero_ext) → Dn	-	-	-	-	3	1	D1	1111	1000	1011	11Dn	<d8	....>									
	MOVHU (d16,SP),Dn	mem16(d16(zero_ext)+SP)(zero_ext) → Dn	-	-	-	-	4	1	D2	1111	1010	1011	11Dn	<d16	....	....	....>							
	MOVHU (d32,SP),Dn	mem16(d32+SP)(zero_ext) → Dn	-	-	-	-	6	2	D4	1111	1100	1011	11Dn	<d32	....	....	....	....	....	....	....>			
	MOVHU (Di,Am),Dn	mem16(Di+Am)(zero_ext) → Dn	-	-	-	-	2	1	D0	1111	0100	10Dn	DiAm											
	MOVHU (abs16),Dn	mem16(abs16(zero_ext))(zero_ext) → Dn	-	-	-	-	3	1	S2	0011	10Dn	<abs16	....	....	....>									
	MOVHU (abs32),Dn	mem16(abs32)(zero_ext) → Dn	-	-	-	-	6	2	D4	1111	1100	1010	11Dn	<abs32	....	....	....	....	....	....	....>			
	MOVHU Dm,(An)	Dm → mem16(An)	-	-	-	-	2	1	D0	1111	0000	0111	DmAn											
	MOVHU Dm,(d8,An)	Dm → mem16(d8(sign_ext)+An)	-	-	-	-	3	1	D1	1111	1000	0111	DmAn	<d8	....>									
	MOVHU Dm,(d16,An)	Dm → mem16(d16(sign_ext)+An)	-	-	-	-	4	1	D2	1111	1010	0111	DmAn	<d16	....	....	....>							
	MOVHU Dm,(d32,An)	Dm → mem16(d32+An)	-	-	-	-	6	2	D4	1111	1100	0111	DmAn	<d32	....	....	....	....	....	....	....>			
	MOVHU Dm,(d8,SP)	Dm → mem16(d8(zero_ext)+SP)	-	-	-	-	3	1	D1	1111	1000	1001	Dm11	<d8	....>									
	MOVHU Dm,(d16,SP)	Dm → mem16(d16(zero_ext)+SP)	-	-	-	-	4	1	D2	1111	1010	1001	Dm11	<d16	....	....	....>							
	MOVHU Dm,(d32,SP)	Dm → mem16(d32+SP)	-	-	-	-	6	2	D4	1111	1100	1001	Dm11	<d32	....	....	....	....	....	....	....>			
	MOVHU Dm,(Di,An)	Dm → mem16(Di+An)	-	-	-	-	2	2	D0	1111	0100	11Dm	DiAn											
	MOVHU Dm,(abs16)	Dm → mem16(abs16(zero_ext))	-	-	-	-	3	1	S2	0000	Dm11	<abs16	....	....	....>									
	MOVHU Dm,(abs32)	Dm → mem16(abs32)	-	-	-	-	6	2	D4	1111	1100	1000	Dm11	<abs32	....	....	....	....	....	....	....>			

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code															Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
MOVH	MOVH (Am),Dn	mem16(Am)(sign_ext) → Dn	-	-	-	-	3	2																	
	MOVH (d8,Am),Dn	mem16(d8(sign_ext)+Am)(sign_ext) → Dn	-	-	-	-	4	2																	
	MOVH (d16,Am),Dn	mem16(d16(sign_ext)+Am)(sign_ext) → Dn	-	-	-	-	5	2																	
	MOVH (d32,Am),Dn	mem16(d32+Am)(sign_ext) → Dn	-	-	-	-	7	3																	
	MOVH (d8,SP),Dn	mem16(d8(zero_ext)+SP)(sign_ext) → Dn	-	-	-	-	4	2																	
	MOVH (d16,SP),Dn	mem16(d16(zero_ext)+SP)(sign_ext) → Dn	-	-	-	-	5	2																	
	MOVH (d32,SP),Dn	mem16(d32+SP)(sign_ext) → Dn	-	-	-	-	7	3																	
	MOVH (Di,Am),Dn	mem16(Di+Am)(sign_ext) → Dn	-	-	-	-	3	2																	
	MOVH (abs16),Dn	mem16(abs16(zero_ext))(sign_ext) → Dn	-	-	-	-	4	2																	
	MOVH (abs32),Dn	mem16(abs32)(sign_ext) → Dn	-	-	-	-	7	3																	
	MOVH Dm,(An)	Dm → mem16(An)	-	-	-	-	2	1																	
	MOVH Dm,(d8,An)	Dm → mem16(d8(sign_ext)+An)	-	-	-	-	3	1																	
	MOVH Dm,(d16,An)	Dm → mem16(d16(sign_ext)+An)	-	-	-	-	4	1																	
	MOVH Dm,(d32,An)	Dm → mem16(d32+An)	-	-	-	-	6	2																	
	MOVH Dm,(d8,SP)	Dm → mem16(d8(zero_ext)+SP)	-	-	-	-	3	1																	
	MOVH Dm,(d16,SP)	Dm → mem16(d16(zero_ext)+SP)	-	-	-	-	4	1																	
	MOVH Dm,(d32,SP)	Dm → mem16(d32+SP)	-	-	-	-	6	2																	
	MOVH Dm,(Di,An)	Dm → mem16(Di+An)	-	-	-	-	2	2																	
	MOVH Dm,(abs16)	Dm → mem16(abs16(zero_ext))	-	-	-	-	3	1																	
	MOVH Dm,(abs32)	Dm → mem16(abs32)	-	-	-	-	6	2																	
MOVM	MOVM (SP),[reg1,..,regn]	PC+2 → PC	-	-	-	-	2	1	S1	1100	1110	<regs	....>												registers specified with regs = 0
		mem32(SP) → reg,SP+4 → SP	-	-	-	-	2	2																	registers specified with regs = 1
		mem32(SP+4) → reg1,mem32(SP) → reg2, SP+8 → SP	-	-	-	-	2	3																	registers specified with regs = 2(*1)
		mem32(SP+8) → reg1,mem32(SP+4) → reg2, mem32(SP) → reg3,SP+12 → SP	-	-	-	-	2	4																	registers specified with regs = 3(*1)
		mem32(SP+12) → D2,mem32(SP+8) → D3, mem32(SP+4) → A2,mem32(SP) → A3, SP+16 → SP	-	-	-	-	2	5																	registers specified with regs = =4(*1)
		mem32(SP+28) → D0,mem32(SP+24) → D1, mem32(SP+20) → A0,mem32(SP+16) → A1, mem32(SP+12) → MDR,mem32(SP+8) → LIR, mem32(SP+4) → LAR,SP+32 → SP	-	-	-	-	2	8																	registers specified with regs = 7
		mem32(SP+32) → reg,mem32(SP+28) → D0, mem32(SP+24) →D1,mem32(SP+20) →A0, mem32(SP+16) →A1,mem32(SP+12) →MDR, mem32(SP+8) →LIR,mem32(SP+4) →LAR, SP+36 →SP	-	-	-	-	2	9																	registers specified with regs = 8
		mem32(SP+36)→reg1, mem32(SP+32)→reg2, mem32(SP+28)→D0,mem32(SP+24)→D1, mem32(SP+20)→A0,mem32(SP+16)→A1, mem32(SP+12)→MDR,mem32(SP+8)→LIR, mem32(SP+4)→LAR,SP+40 →SP	-	-	-	-	2	10																	registers specified with regs = 9(*1)

*1: registers specified with regn are returned in the order; D2, D3, A2 and A3 no matter when the assembler srites these registers. Skip the registers which is not specified.

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code															Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
MOVM	MOVM (SP),[reg1,.,regn]	mem32(SP+40)→reg1,mem32(SP+36)→reg2, mem32(SP+32)→reg3,mem32(SP+28)→D0, mem32(SP+24)→D1,mem32(SP+20)→A0, mem32(SP+16)→A1,mem32(SP+12)→MDR, mem32(SP+8)→LIR,mem32(SP+4)→LAR, SP+44→SP	-	-	-	-	2	11	S1	1100	1110	<regs ....>												registers specified with regs=10(*1)
		mem32(SP+44)→D2,mem32(SP+40)→D3, mem32(SP+36)→A2,mem32(SP+32)→A3, mem32(SP+28)→D0,mem32(SP+24)→D1, mem32(SP+20)→A0,mem32(SP+16)→A1, mem32(SP+12)→MDR,mem32(SP+8)→LIR, mem32(SP+4)→LAR,SP+48→SP	-	-	-	-	2	12																rregisters specified with regs=11
	MOVM [reg1,.,regn],(SP)	PC+2→PC	-	-	-	-	2	1	S1	1100	1111	<regs ....>												registers specified with regs =0
		reg→mem32(SP-4),SP-4→SP	-	-	-	-	2	1																registers specified with regs=1
		reg1→mem32(SP-4),reg2→mem32(SP-8), SP-8→SP	-	-	-	-	2	2																registers specified with regs= 2(*2)
		reg1→mem32(SP-4),reg2→mem32(SP-8), reg3→mem32(SP-12),SP-12→SP	-	-	-	-	2	3																registers specified with regs= 3(*2)
		D2→mem32(SP-4),D3→mem32(SP-8), A2→mem32(SP-12),A3→mem32(SP-16), SP-16→SP	-	-	-	-	2	4																registers specified with regs= 4
		D0→mem32(SP-4),D1→mem32(SP-8), A0→mem32(SP-12),A1→mem32(SP-16), MDR→mem32(SP-20),LIR→mem32(SP-24), LAR→mem32(SP-28),SP-32→SP	-	-	-	-	2	8																registers specified with regs= 7
		reg→mem32(SP-4),D0→mem32(SP-8), D1→mem32(SP-12),A0→mem32(SP-16), A1→mem32(SP-20),MDR→mem32(SP-24), LIR→mem32(SP-28),LAR→mem32(SP-32), SP-36→SP	-	-	-	-	2	9																registers specified with regs= 8(*2)
		reg1→mem32(SP-4),reg2→mem32(SP-8), D0→mem32(SP-12),D1→mem32(SP-16), A0→mem32(SP-20),A1→mem32(SP-24), MDR→mem32(SP-28),LIR→mem32(SP-32), LAR→mem32(SP-36),SP-40→SP	-	-	-	-	2	10																registers specified with regs= 9(*2)
		reg1→mem32(SP-4),reg2→mem32(SP-8), reg3→mem32(SP-12),D0→mem32(SP-16), D1→mem32(SP-20),A0→mem32(SP-24), A1→mem32(SP-28),MDR→mem32(SP-32), LIR→mem32(SP-36),LAR→mem32(SP-40),, SP-44→SP	-	-	-	-	2	11																registers specified with regs= 10(*2)

*1: Registers specified with regn are returned in the order; D2, D3, A2 and A3 no matter when the assembler writes theses registers. Skip the registers which is not specified

*2: Registers specified with regn are saved in the order; D2, D3, A2 and A3 no matter when the assembler write these registers. Skip the registers which is not specified.

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
MOVM	MOVM regs,(SP)	D2 → mem32(SP-4),D3 → mem32(SP-8) A2 → mem32(SP-12),A3 → mem32(SP-16) D0 → mem32(SP-20),D1 → mem32(SP-24) A0 → mem32(SP-28),A1 → mem32(SP-32) MDR → mem32(SP-36),LIR → mem32(SP-40) LAR → mem32(SP-44),SP-48 → SP	-	-	-	-	2	12	S1	1100	1111	<regs												Registers specified with regs =11
EXT	EXT Dn	IF (Dn.bp31=0), 0x00000000 → MDR IF (Dn.bp31=1), 0xFFFFFFFF → MDR	-	-	-	-	2	1	D0	1111	0010	1101	00Dn											
EXTB	EXTB Dn	IF (Dn.bp7=0), Dn & 0x000000FF → Dn IF (Dn.bp7=1), Dn | 0xFFFFFF00 → Dn	-	-	-	-	1	1	S0	0001	00Dn													
EXTBU	EXTBU Dn	Dn & 0x000000FF → Dn	-	-	-	-	1	1	S0	0001	01Dn													
EXTH	EXTH Dn	IF (Dn.bp15=0), Dn & 0x0000FFFF → Dn IF (Dn.bp15=1), Dn | 0xFFFF0000 → Dn	-	-	-	-	1	1	S0	0001	10Dn													
EXTHU	EXTHU Dn	Dn & 0x0000FFFF → Dn	-	-	-	-	1	1	S0	0001	11Dn													
CLR	CLR Dn	0 → Dn	0	0	0	1	1	1	S0	0000	Dn00													
Arithmetic Operation Instructions																								
ADD	ADD Dm,Dn	Dm + Dn → Dn	●	●	●	●	1	1	S0	1110	DmDn													
	ADD Dm,An	Dm + An → An	●	●	●	●	2	1	D0	1111	0001	0101	AmDn											
	ADD Am,Dn	Am + Dn → Dn	●	●	●	●	2	1	D0	1111	0001	0110	DmAn											
	ADD Am,An	Am + An → An	●	●	●	●	2	1	D0	1111	0001	0111	AmAn											
	ADD imm8,Dn	imm8(sign_ext) + Dn → Dn	●	●	●	●	2	1	S1	0010	10Dn	<imm8 ....>												
	ADD imm16,Dn	imm16(sign_ext) + Dn → Dn	●	●	●	●	4	1	D2	1111	1010	1100	00Dn	<imm16....	....	....>								
	ADD imm32,Dn	imm32 + Dn → Dn	●	●	●	●	6	2	D4	1111	1100	1100	00Dn	<imm32....	....	....	....	....	....	....	....>			
	ADD imm8,An	imm8(sign_ext) + An → An	●	●	●	●	2	1	S1	0010	00An	<imm8 ....>												
	ADD imm16,An	imm16(sign_ext) + An → An	●	●	●	●	4	1	D2	1111	1010	1101	00An	<imm16....	....	....>								
	ADD imm32,An	imm32 + An → An	●	●	●	●	6	2	D4	1111	1100	1101	00An	<imm32....	....	....	....	....	....	....	....>			
	ADD imm8,SP	imm8(sign_ext) + SP → SP	-	-	-	-	3	1	D1	1111	1000	1111	1110	<imm8 ....>										
	ADD imm16,SP	imm16(sign_ext) + SP → SP	-	-	-	-	4	1	D2	1111	1010	1111	1110	<imm16....	....	....>								
	ADD imm32,SP	imm32 + SP → SP	-	-	-	-	6	2	D4	1111	1100	1111	1110	<imm32....	....	....	....	....	....	....	....>			
ADDC	ADDC Dm,Dn	Dm + Dn + CF → Dn	●	●	●	●	2	1	D0	1111	0001	0100	DmDn											
SUB	SUB Dm,Dn	Dn - Dm → Dn	●	●	●	●	2	1	D0	1111	0001	0000	DmDn											
	SUB Dm,An	An - Dm → An	●	●	●	●	2	1	D0	1111	0001	0010	DmAn											
	SUB Am,Dn	Dn - Am → Dn	●	●	●	●	2	1	D0	1111	0001	0001	AmDn											
	SUB Am,An	An - Am → An	●	●	●	●	2	1	D0	1111	0001	0011	AmAn											
	SUB imm32,Dn	Dn - imm32 → Dn	●	●	●	●	6	2	D4	1111	1100	1100	10Dn	<imm32....	....	....	....	....	....	....	....>			
	SUB imm32,An	An - imm32 → An	●	●	●	●	6	2	D4	1111	1100	1101	01An	<imm32....	....	....	....	....	....	....	....>			
SUBC	SUBC Dm,Dn	Dn - Dm - CF → Dn	●	●	●	●	2	1	D0	1111	0001	1000	DmDn											
MUL	MUL Dm,Dn	(Dn* Dn) → { MDR , Dn }	?	?	●	●	2	3	D0	1111	0010	0100	DmDn											Dn =0
								13																Dn =value by 1 byte
								21																Dn =value by 2-byte
								29																Dn =value by 3-byte
								34																Dn =value by 4-byte

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Group	Mnemonic	Operation	Flag VF	Flag CF	Flag NF	Flag ZF	Code Size	Cycle	For -mat	Machine Code 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Notes
MULU	MULU Dm,Dn	(Dn* Dn) → { MDR , Dn }	?	?	●	●	2	3	D0	1111	0010	0101	DmDn											Dn = 0
								13																Dn = value by 1 byte
								21																Dn = value by 2-byte
								29																Dn = value by 3-byte
								34																Dn = value by 4-byte
DIV	DIV Dm,Dn	((MDR<< 32) & 0xFFFFFFFF00000000 + Dn)	0/1	?/?	●/?	●/?	2	4	D0	1111	0010	0110	DmDn											{MDR,Dn} = 0
		/ Dm → Dn						14																{MDR,Dn}= value by 1 byte
		((MDR<< 32) & 0xFFFFFFFF00000000 + Dn)						22																{MDR,Dn} = value by 2- byte
		% Dm → MDR						30																{MDR,Dn} = value by 3-byte
								38																{MDR,Dn} = value by 4- byte or more
DIVU	DIVU Dm,Dn	((MDR<< 32) & 0xFFFFFFFF00000000 + Dn)	0/1	?/?	●/?	●/?	2	4	D0	1111	0010	0111	DmDn											{MDR,Dn} = 0
		/ Dm → Dn						14																{MDR,Dn} = value by 1 byte
		((MDR<< 32) & 0xFFFFFFFF00000000+ Dn)						22																{MDR,Dn} = value by 2- byte
		% Dm → MDR						30																{MDR,Dn} = value by 3-byte
								38																{MDR,Dn} = value by 4- byte or more
INC	INC Dn	Dn + 1 → Dn	●	●	●	●	1	1	S0	0100	Dn00													
	INC An	An + 1 → An	-	-	-	-	1	1	S0	0100	An01													
INC4	INC4 An	An + 4 → An	-	-	-	-	1	1	S0	0101	00An													
Comparative Instructions																								
CMP	CMP Dm,Dn	Dn - Dm : PSW	●	●	●	●	1	1	S0	1010	DmDn													
	CMP Dm,An	An - Dm : PSW	●	●	●	●	2	1	D0	1111	0001	1010	DmAn											
	CMP Am,Dn	Dn - Am : PSW	●	●	●	●	2	1	D0	1111	0001	1001	AmDn											
	CMP Am,An	An - Am : PSW	●	●	●	●	1	1	S0	1011	AmAn													
	CMP imm8,Dn	Dn - imm8(sign_ext) : PSW	●	●	●	●	2	1	S1	1010	DnDn	<imm8 ....>												
	CMP imm16,Dn	Dn - imm16(sign_ext) : PSW	●	●	●	●	4	1	D2	1111	1010	1100	10Dn	<imm16	....	....>							....>	
	CMP imm32,Dn	Dn - imm32 : PSW	●	●	●	●	6	2	D4	1111	1100	1100	10Dn	<imm32	....	....	....	....	....					
	CMP imm8,An	An - imm8(zero_ext) : PSW	●	●	●	●	2	1	S1	1011	AnAn	<imm8 ....>												
	CMP imm16,An	An - imm16(zero_ext) : PSW	●	●	●	●	4	1	D2	1111	1010	1101	10An	<imm16	....	....>							....>	
	CMP imm32,An	An - imm32 : PSW	●	●	●	●	6	2	D4	1111	1100	1101	10An	<imm32	....	....	....	....	....					
Logical Operation Instructions																								
AND	AND Dm,Dn	Dm & Dn → Dn	0	0	●	●	2	1	D0	1111	0010	0000												
	AND imm8,Dn	imm8(zero_ext) & Dn → Dn	0	0	●	●	3	1	D1	1111	1000	1110	00Dn	<imm8 ....>										
	AND imm16,Dn	imm16(zero_ext) & Dn → Dn	0	0	●	●	4	1	D2	1111	1010	1110	00Dn	<imm16	....	....>							....>	
	AND imm32,Dn	imm32 & Dn → Dn	0	0	●	●	6	2	D4	1111	1100	1110	00Dn	<imm32	....	....	....	....	....					
	AND imm16,PSW	imm16(zero_ext) & PSW → PSW	●	●	●	●	4	1	D2	1111	1010	1111	1100	<imm16	....	....>								
OR	OR Dm,Dn	Dm | Dn → Dn	0	0	●	●	2	1	D0	1111	0010	0001	DmDn											
	OR imm8,Dn	imm8(zero_ext) | Dn → Dn	0	0	●	●	3	1	D1	1111	1000	1110	01Dn	<imm8 ....>										
	OR imm16,Dn	imm16(zero_ext) | Dn → Dn	0	0	●	●	4	1	D2	1111	1010	1110	01Dn	<imm16	....	....>							....>	
	OR imm32,Dn	imm32 | Dn → Dn	0	0	●	●	6	2	D4	1111	1100	1110	0?Dn	<imm32	....	....	....	....	....					
	OR imm16,PSW	imm16(zero_ext) | PSW → PSW	●	●	●	●	4	1	D2	1111	1010	1111?	1101	<imm16	....	....>								

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code															Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
XOR	XOR Dm,Dn	Dm ^ Dn → Dn	0	0	●	●	2	1	D0	1111	0010	0010	DmDn												
	XOR imm16,Dn	imm16(zero_ext) ^ Dn → Dn	0	0	●	●	4	1	D2	1111	1010	1110	10Dn	<imm16....		....	....>								
	XOR imm32,Dn	imm32 ^ Dn → Dn	0	0	●	●	6	2	D4	1111	1100	1110	10Dn	<imm32....		....	....	....	....	....	....	....>			
NOT	NOT Dn	Dn ^ 0xFFFFFFFF → Dn	0	0	●	●	2	1	D0	1111	0010	0011	00Dn												
Bit Instructions																									
BTST	BTST imm8,Dn	imm8(zero_ext) & Dn : PSW	0	0	●	●	3	1	D1	1111	1000	1110	11Dn	<imm8 ....>											
	BTST imm16,Dn	imm16(zero_ext) & Dn : PSW	0	0	●	●	4	1	D2	1111	1010	1110	11Dn	<imm16....		....	....>								
	BTST imm32,Dn2	imm32 & Dn : PSW	0	0	●	●	6	2	D4	1111	1100	1110	11Dn	<imm32....		....	....	....	....	....	....	....>			
	BTST imm8,(d8,An)	imm8(zero_ext) & mem8(d8(sign_ext)+An)(zero_ext) : PSW	0	0	0	●	4	4	D2	1111	1010	1111	10An	<d8 ....>		<imm8 ....>									
	BTST imm8,(abs16)	imm8(zero_ext) & mem8(abs16(zero_ext))(zero_ext) : PSW	0	0	0	●	5	4	D3	1111	1110	1000	0010	<abs16....		....	....>	<imm8 ....>						Not used for AM30/AM31
	BTST imm8,(abs32)	imm8(zero_ext) & mem8(abs32)(zero_ext) : PSW	0	0	0	●	7	5	D5	1111	1110	0000	0010	<abs32....		....	....	....	....	....	....	....>	<imm8....>		
BSET	BSET Dm,(An)	mem8(An)(zero_ext) → temp, temp & Dm : PSW, temp | Dm → mem8(An)	0	0	0	●	2	5	D0	1111	0000	1000	DmAn												
	BSET imm8,(d8,An)	mem8(d8(sign_ext) + An)(zero_ext) → temp, temp & imm8(zero_ext): PSW, temp | imm8(zero_ext) → mem8(d8(sign_ext) + An)	0	0	0	●	4	5	D2	1111	1010	1111	00An	<d8 ....>		<imm8 ....>									
	BSET imm8,(abs16)	mem8(abs16(zero_ext))(zero_ext) → temp , temp & imm8(zero_ext) : PSW, temp | imm8(zero_ext) → mem8(abs16(zero_ext))	0	0	0	●	5	5	D3	1111	1110	1000	0000	<abs16....		....	....>	<imm8 ....>						Not used for AM30/AM31
	BSET imm8,(abs32)	mem8(abs32)(zero_ext) → temp , temp & imm8(zero_ext) : PSW, temp | imm8(zero_ext) → mem8(abs32)	0	0	0	●	7	6	D5	1111	1110	0000	0000	<abs32....		....	....	....	....	....	....	....>	<imm8....>		
BCLR	BCLR Dm,(An)	mem8(An)(zero_ext) → temp , temp & Dm : PSW, temp & (Dm ^ 0xFFFFFFFF) → mem8(An)	0	0	0	●	2	5	D0	1111	0000	1001	DmAn												
	BCLR imm8,(d8,An)	mem(d8(sign_ext) + An)(zero_ext) → temp, temp & imm8(zero_ext) : PSW, temp & (imm8(zero_ext) ^ 0xFFFFFFFF) → mem8(d8(sign_ext) + An)	0	0	0	●	4	5	D2	1111	1010	1111	01An	<d8 ....>		<imm8 ....>									
	BCLR imm8,(abs16)	mem8(abs16(zero_ext))(zero_ext) → temp , temp & imm8(zero_ext) : PSW, temp & (imm8(zero_ext) ^ 0xFFFFFFFF) → mem8(abs16(zero_ext))	0	0	0	●	5	5	D3	1111	1110	1000	0001	<abs16....		....	....>	<imm8 ....>						Not used for AM30/AM31
	BCLR imm8,(abs32)	mem8(abs32)(zero_ext) → temp , temp & imm8(zero_ext) : PSW, temp & (imm8(zero_ext) ^ 0xFFFFFFFF) → mem8(abs32)	0	0	0	●	7	6	D5	1111	1110	0000	0001	<abs32....		....	....	....	....	....	....	....>	<imm8....>		

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Shift Instructions																								
ASR	ASR Dm,Dn	IF ((Dm&0x0000001F) ≠ 0) , Dn.lsb → CF,	?	●	●	●	2	1	D0	1111	0010	1011	DmDn											
		(Dn >> (Dm & 0x0000001F))(sign_ext) → Dn																						
		IF ((Dm&0x0000001F)=0),PC + 2 → PC	?	?	●	●																		
	ASR imm8,Dn	IF ((imm8 & 0x1F) ≠0) , Dn.lsb → CF,	?	●	●	●	3	1	D1	1111	1000	1100	10Dn	<imm8 ....>										
		(Dn >> (imm8 & 0x1F))(sign_ext) → Dn																						
		IF ((imm8 & 0x1F)=0) , PC + 3 → PC	?	?	●	●																		
	ASR Dn	Dn.lsb → CF, (Dn >> 1)(sign_ext) → Dn	?	●	●	●	3	1																
LSR	LSR Dm,Dn	IF ((Dm&0x0000001F) ≠ 0),Dn.lsb → CF,	?	●	●	●	2	1	D0	1111	0010	1010	DmDn											
		(Dn >> (Dm & 0x0000001F))(zero_ext) → Dn																						
		IF ((Dm&0x0000001F)=0), PC + 2 → PC	?	?	●	●																		
	LSR imm8,Dn	IF ((imm8 & 0x1F) ≠ 0),Dn.lsb → CF,	?	●	●	●	3	1	D1	1111	1000	1100	01Dn	<imm8 ....>										
		(Dn >> (imm8 & 0x1F))(zero_ext) → Dn																						
		IF ((imm8 & 0x1F)=0), PC + 3 → PC	?	?	●	●																		
	LSR Dn	Dn.lsb → CF, (Dn >> 1)(zero_ext) → Dn	?	●	●	●	3	1																
ASL	ASL Dm,Dn	IF ((Dm & 0x0000001F) ≠ 0),	?	?	●	●	2	1	D0	1111	0010	1001	DmDn											
		Dn << (Dm & 0x0000001F) → Dn																						
		IF ((Dm & 0x0000001F)=0), PC + 2 → PC																						
	ASL imm8,Dn	IF ((imm8 & 0x1F) ≠0),	?	?	●	●	3	1	D1	1111	1000	1100	00Dn	<imm8 ....>										
		Dn << (imm8 & 0x1F) → Dn																						
		IF ((imm8 & 0x1F)=0), PC + 3 → PC																						
ASL2	ASL2 Dn	(Dn << 2) & 0xFFFFFFFC → Dn	?	?	●	●	1	1	S0	0101	01Dn													
ROR	ROR Dn	CF << 31 → temp, Dn.lsb → CF,	0	●	●	●	2	1	D0	1111	0010	1000	01Dn											
		(Dn >> 1)(zero_ext) | temp → Dn																						
ROL	ROL Dn	CF → temp, Dn.msb → CF,	0	●	●	●	2	1	D0	1111	0010	1000	00Dn											
		(Dn << 1) | temp → Dn																						

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Branch Instructions																								
Bcc	BEQ (d8,PC)	IF (ZF=1), PC + d8(sign_ext)→ PC IF (ZF=0),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	1000	<d8	....>											Branch enable/disable
	BNE (d8,PC)	IF (ZF=0), PC + d8(sign_ext) → PC IF (ZF=1), PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	1001	<d8	....>											Branch enable/disable
	BGT (d8,PC)	IF ((ZF | (NF^VF))=0),PC + d8(sign_ext) → PC IF ((ZF | (NF^VF))=1),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0001	<d8	....>											Branch enable/disable
	BGE (d8,PC)	IF ((NF ^ VF)=0),PC + d8(sign_ext) → PC IF ((NF ^ VF)=1),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0010	<d8	....>											Branch enable/disable
	BLE (d8,PC)	IF ((ZF | (NF^VF))=1),PC + d8(sign_ext) → PC IF ((ZF | (NF^VF))=0),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0011	<d8	....>											Branch enable/disable
	BLT (d8,PC)	IF ((NF ^ VF)=1),PC + d8(sign_ext) →PC IF ((NF ^ VF)=0),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0000	<d8	....>											Branch enable/disable
	BHI (d8,PC)	IF ((CF | ZF)=0),PC + d8(sign_ext) → PC IF ((CF | ZF)=1),PC + 2 →PC	-	-	-	-	2	3/1*	S1	1100	0101	<d8	....>											Branch enable/disable
	BCC (d8,PC)	IF (CF = 0),PC + d8(sign_ext) → PC IF (CF = 1),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0110	<d8	....>											Branch enable/disable
	BLS (d8,PC)	IF ((CF | ZF)=1),PC + d8(sign_ext) → PC IF ((CF | ZF)=0),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0111	<d8	....>											Branch enable/disable
	BCS (d8,PC)	IF (CF = 1),PC + d8(sign_ext) → PC IF (CF = 0),PC + 2 → PC	-	-	-	-	2	3/1*	S1	1100	0100	<d8	....>											Branch enable/disable
	BVC (d8,PC)	IF (VF = 0),PC + d8(sign_ext) → PC IF (VF = 1),PC + 3 → PC	-	-	-	-	3	4/2*	D1	1111	1000	1110	1000	<d8	....>									Branch enable/disable
	BVS (d8,PC)	IF (VF = 1),PC + d8(sign_ext) → PC IF (VF = 0),PC + 3 → PC	-	-	-	-	3	4/2*	D1	1111	1000	1110	1001	<d8	....>									Branch enable/disable
	BNC (d8,PC)	IF (NF = 0),PC + d8(sign_ext) → PC IF (NF = 1),PC + 3 → PC	-	-	-	-	3	4/2*	D1	1111	1000	1110	1010	<d8	....>									Branch enable/disable
	BNS (d8,PC)	IF (NF = 1),PC + d8(sign_ext) → PC IF (NF = 0),PC + 3 → PC	-	-	-	-	3	4/2*	D1	1111	1000	1110	1011	<d8	....>									Branch enable/disable
	BRA (d8,PC)	PC + d8(sign_ext) →PC	-	-	-	-	2	3	S1	1100	1010	<d8	....>											
Lcc	LEQ	IF (ZF=1), LAR - 4 →PC IF (ZF=0),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	1000													Branch enable/disable
	LNE	IF (ZF=0), LAR - 4 →PC IF (ZF=1), PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	1001													Branch enable/disable

*:Depends on the status of Instruction queue.

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Lcc	LGT	IF ((ZF | (NF^VF))=0), LAR - 4 → PC IF ((ZF | (NF^VF))=1),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0001													Branch enable/disable
	LGE	IF ((NF ^ VF)=0), LAR - 4 →PC IF ((NF ^ VF)=1),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0010													Branch enable/disable
	LLE	IF ((ZF | (NF ^ VF))=1),LAR - 4 →PC IF ((ZF | (NF ^ VF))=0),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0011													Branch enable/disable
	LLT	IF ((NF ^ VF)=1),LAR - 4 →PC IF ((NF ^ VF)=0),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0000													Branch enable/disable
	LHI	IF ((CF | ZF)=0), LAR - 4 →PC IF ((CF | ZF)=1),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0101													Branch enable/disable
	LCC	IF (CF = 0), LAR - 4 →PC IF (CF = 1),PC + 1 → PC	-	-	-	-	1	1/2*	S0	1101	0110													Branch enable/disable
	LLS	IF ((CF | ZF)=1), LAR - 4 →PC IF ((CF | ZF)=0),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	0111													Branch enable/disable
	LCS	IF (CF = 1), LAR - 4 →PC IF (CF = 0),PC + 1 →PC	-	-	-	-	1	1/2*	S0	1101	1001													Branch enable/disable
	LRA	LAR - 4 →PC	-	-	-	-	1	1	S0	1101	1010													
SETLB	SETLB	mem32 (PC + 1) →LIR , PC + 5 →LAR	-	-	-	-	1	1	S0	1101	1011													
JMP	JMP (An)	An → PC	-	-	-	-	2	3	D0	1111	0000	1111	01An											
	JMP label	IF (label = (d16,PC)),PC + d16(sign_ext) →PC	-	-	-	-	3	2	S2	1100	1100	<d16.	....	....>										
		IF (label = (d32,PC)),PC + d32 →PC	-	-	-	-	5	3**	S4	1101	1100	<d32	....	....	....	....	....	....	....>					**4 cycyes for AM30
CALL	CALL label	PC + 5 →mem32(SP), SP - imm8(zero_ext) →SP,PC + 5 →MDR, PC + d16(sign_ext) →PC	-	-	-	-	5	2	S4	1100	1101	<d16.	....	....>	<regs ....>	<imm8 ....>								If label = (d16,PC), registers specified with regs = 0
		PC + 5 →mem32(SP),reg1 →mem32(SP-4), SP - imm8(zero_ext) →SP,PC + 5 →MDR, PC + d16(sign_ext) →PC	-	-	-	-	5	3																If label = (d16,PC), registers specified with regs = 1
		PC + 5 →mem32(SP),reg1→mem32(SP-4), reg2→mem32(SP),SP - imm8(zero_ext) →SP, PC + 5 →MDR,PC + d16(sign_ext) →PC	-	-	-	-	5	4																If label = (d16,PC), registers specified with regs = 2
		PC + 5 →mem32(SP),reg1→mem32(SP-4), reg2→mem32(SP-8),reg3→mem32(SP), SP - imm8(zero_ext) →SP,PC + 5 →MDR, PC + d16(sign_ext) →PC	-	-	-	-	5	5																If label = (d16,PC), registers specified with regs = 3
		PC + 5 →mem32(SP),D2→mem32(SP-4), D3→mem32(SP-8),A2→mem32(SP-12), A3→mem32(SP-16), SP - imm8(zero_ext) →SP,PC + 5 →MDR, PC + d16(sign_ext) →PC	-	-	-	-	5	6																If label = (d16,PC), registers specified with regs = 4

*: Depends on the status of Instruction queue.

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
CALL	CALL label	PC + 5 → mem32(SP),D0 → mem32(SP-4), D1→ mem32(SP-8),A0→ mem32(SP-12), A1→ mem32(SP-16),MDR→ mem32(SP-20), LIR→ mem32(SP-24),LAR→ mem32(SP-28), SP - imm8(zero_ext) → SP,PC + 5 → MDR, PC + d16(sign_ext) → PC	-	-	-	-	5	9	S4	1100	1101	<d16.	....	....	....>	<regs	....>	<imm8 ....>						If label = (d16,PC), registers specified with regs = 7
		PC + 5 → mem32(SP),reg1→ mem32(SP-4), D0→ mem32(SP-8),D1→ mem32(SP-12), A0→ mem32(SP-16),A1→ mem32(SP-20), MDR→ mem32(SP-24),LIR→ mem32(SP-28), LAR→ mem32(SP-32), SP - imm8(zero_ext) → SP,PC + 5 → MDR, PC + d16(sign_ext) → PC	-	-	-	-	5	10																If label = (d16,PC), registers specified with regs = 8
		PC + 5 → mem32,(SP)reg1→ mem32(SP-4), reg2 → mem32(SP-8),D0→ mem32(SP-12), D1→ mem32(SP-16),A0→ mem32(SP-20), A1→ mem32(SP-24),MDR→ mem32(SP-28), LIR→ mem32(SP-32),LAR→ mem32(SP-36), SP - imm8(zero_ext) → SP,PC + 5 → MDR, PC + d16(sign_ext) → PC	-	-	-	-	5	11																If label = (d16,PC), registers specified with regs = 9
		PC + 5 → mem32(SP),reg1→ mem32(SP-4), reg2→ mem32(SP-8),reg3→ mem32(SP-12), D0→ mem32(SP-16),D1→ mem32(SP-20), A0→ mem32(SP-24),A1→ mem32(SP-28), MDR→ mem32(SP-32),LIR→ mem32(SP-36), LAR→ mem32(SP-40), SP - imm8(zero_ext) → SP,PC + 5 → MDR, PC + d16(sign_ext) → PC	-	-	-	-	5	12																If label = (d16,PC), registers specifiied with regs = 10
		PC + 5 →mem32(SP),D2→ mem32(SP-4), D3→ mem32(SP-8),A2→ mem32(SP-12), A3→ mem32(SP-16),D0→ mem32(SP-20), D1→ mem32(SP-24),A0→ mem32(SP-28), A1→ mem32(SP-32),MDR→ mem32(SP-36), LIR→ mem32(SP-40),LAR→ mem32(SP-44) SP - imm8(zero_ext) → SP,PC + 5 → MDR, PC+d16(sign_ext) → PC,	-	-	-	-	5	13																If label = (d16,PC), registers specified with regs = 11
		PC+7 → mem32(SP), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	4*	S6	1101	1101	<d32	....	....	....	....	....	....>	<regs	...>	<imm8 ....>			If label = (d32,PC), registers specified with regs = 0 *: 5 cycyles for AM30
		PC + 7 → mem32(SP),reg1 → mem32(SP-4), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	4*																If label = (d32,PC), register specified with regs = 1 *: 5 cycles for AM30

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code															Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
CALL	CALL label	PC + 7 → mem32(SP),reg1→ mem32(SP-4), reg2→ mem32(SP),SP - imm8(zero_ext) → SP, PC + 7 → MDR,PC + d32 → PC	-	-	-	-	7	5*	S6	1101	1101	<d32	....	....	....	....	....	....	....>	<regs	....>	<imm8	....>		If label = (d32,PC), registers specified with regs = 2 *: 6 cycyles for AM30
		PC + 7 → mem32(SP), reg1→ mem32(SP-4),reg2→ mem32(SP-8), reg3→ mem32(SP),SP - imm8(zero_ext) → SP, PC + 7 → MDR,PC + d32 → PC	-	-	-	-	7	6*																	If label = (d32,PC), registers specified wtih regs = 3 *: 7 cycles for AM30
		PC + 7 → mem32(SP),D2→ mem32(SP-4), D3→ mem32(SP-8),A2→ mem32(SP-12), A3→ mem32(SP-16), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	7*																	If label = (d32,PC), registers specified with regs = 4 *: 8 cycles for AM30
		PC + 7 → mem32(SP),D0→ mem32(SP-4), D1→ mem32(SP-8),A0→ mem32(SP-12), A1→ mem32(SP-16),MDR→ mem32(SP-20), LIR→ mem32(SP-24),LAR→ mem32(SP-28), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	10*																	If label = (d32,PC), registers specified with regs = 7 *: 11 cycles for AM30
		PC + 7 → mem32(SP),reg1→ mem32(SP-4), D0→ mem32(SP-8),D1→ mem32(SP-12), A0→ mem32(SP-16),A1→ mem32(SP-20), MDR→ mem32(SP-24),LIR→ mem32(SP-28), LAR→ mem32(SP-32), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	11*																	If label = (d32,PC), registers specified with regs = 8 *: 12 cycles for AM30
		PC + 7 → mem32(SP),reg1→ mem32(SP-4), reg2 → mem32(SP-8),D0→ mem32(SP-12), D1→ mem32(SP-16),A0→ mem32(SP-20), A1→ mem32(SP-24),MDR→ mem32(SP-28), LIR→ mem32(SP-32),LAR→ mem32(SP-36), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	12*																	If label = (d32,PC), registers specified with regs = 9 *: 13 cycles for AM30
		PC + 7 → mem32(SP),reg1→ mem32(SP-4), reg2→ mem32(SP-8),reg3→ mem32(SP-12), D0→ mem32(SP-16),D1→ mem32(SP-20), A0→ mem32(SP-24),A1→ mem32(SP-28), MDR→ mem32(SP-32),LIR→ mem32(SP-36), LAR→ mem32(SP-40), SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	13*																	If label = (d32,PC), registers specified with regs =10 * 14 cycles for AM30

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
CALL	CALL label	PC + 7 → mem32(SP),D2→ mem32(SP-4), D3→ mem32(SP-8),A2→ mem32(SP-12), A3→ mem32(SP-16),D0→ mem32(SP-20), D1→ mem32(SP-24),A0→ mem32(SP-28), A1→ mem32(SP-32),MDR→ mem32(SP-36), LIR→ mem32(SP-40),LAR→ mem32(SP-44) SP - imm8(zero_ext) → SP,PC + 7 → MDR, PC + d32 → PC	-	-	-	-	7	14*	S6	1101	1101	<d32	....	....	....	....	....	....	....>	<regs	....>	<imm8	....>	If label = (d32,PC), registersspecified with regs =11 *: 5 cycles for AM30
CALLS	CALLS (An)	PC + 2 → mem32(SP),PC + 2 → MDR, An → PC	-	-	-	-	2	3	D0	1111	0000	1111	00An											
	CALLS label	IF (label = (d16,PC)), PC + 4 → mem32(SP), PC + 4 → MDR, PC +d16 (sign_ext) → PC	-	-	-	-	4	3	D2	1111	1010	1111	1111	<d16	....	....	....>								*: 4 cycles for AM30
		IF ((label = (d32,PC)), PC + 6 → mem32(SP), PC + 6 → MDR, PC + d32 → PC	-	-	-	-	6	3*	D4	1111	1100	1111	1111	<d32	....	....	....	....	....	....	....	....>			registers specified with regs =0 *:4 cycles for AM30
RET	RET	SP + imm8(zero_ext) → SP,mem32(SP) → PC	-	-	-	-	3	5*	S2	1101	1111	<regs	....>	<imm8	....>									registers specified with regs =1 *:4 cycles for AM30
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg, mem32(SP) → PC	-	-	-	-	3	5*																registers specified with regs =2 *:4 cycles for AM30
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP) → PC	-	-	-	-	3	5*																registers specified with regs =3 *:4 cycles for AM30
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ reg3,mem32(SP) → PC	-	-	-	-	3	5*																registers specified with regs =4
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ D2,mem32(SP-8)→ D3, mem32(SP-12)→ A2,mem32(SP-16)→ A3, mem32(SP) → PC	-	-	-	-	3	5																registers specified with regs =7
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ D0,mem32(SP-8)→ D1, mem32(SP-12)→ A0,mem32(SP-16)→ A1, mem32(SP-20)→ MDR,mem32(SP-24)→ LIR, mem32(SP-28)→ LAR,mem32(SP) → PC	-	-	-	-	3	8																registers specified with regs =8
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg1,mem32(SP-8)→ D0, mem32(SP-12)→ D1,mem32(SP-16)→ A0, mem32(SP-20)→ A1,mem32(SP-24)→ MDR, mem32(SP-28)→ LIR,mem32(SP-32)→ LAR, mem32(SP) → PC	-	-	-	-	3	9																

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code															Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
RET	RET	SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ D0,mem32(SP-16)→ D1, mem32(SP-20)→ A0,mem32(SP-24)→ A1, mem32(SP-28)→ MDR,mem32(SP-32)→ LIR, mem32(SP-36)→ LAR,mem32(SP) → PC	-	-	-	-	3	10	S2	1101	1111	<regs ....>		<imm8 ....>										registers specified with regs = 9
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ reg3,mem32(SP-16)→ D0, mem32(SP-20)→ D1,mem32(SP-24)→ A0, mem32(SP-28)→ A1,mem32(SP-32)→ MDR, mem32(SP-36)→ LIR,mem32(SP-40)→ LAR, mem32(SP) → PC	-	-	-	-	3	11																registers specified with regs= 10
		SP + imm8(zero_ext) → SP, mem32(SP-4)→ D2,mem32(SP-8)→ D3, mem32(SP-12)→ A2,mem32(SP-16)→ A3, mem32(SP-20)→ D0,mem32(SP-24)→ D1, mem32(SP-28)→ A0,mem32(SP-32)→ A1, mem32(SP-36)→ MDR,mem32(SP-40)→ LIR, mem32(SP-44)→ LAR,mem32(SP) → PC	-	-	-	-	3	12																registers specified with regs= 11
RETF	RETF	SP + imm8(zero_ext) → SP,MDR → PC,	-	-	-	-	3	2	S2	1101	1110	<regs ....>		<imm8 ....>										register specified with regs = 0
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg	-	-	-	-	3	2																register specified with regs= 1
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2,	-	-	-	-	3	3																registers specified with regs = 2
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ reg3	-	-	-	-	3	4																registers specified with regs= 3
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ D2,mem32(SP-8)→ D3, mem32(SP-12)→ A2,mem32(SP-16)→ A3,	-	-	-	-	3	5																registers specified with regs= 4
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ D0,mem32(SP-8)→ D1, mem32(SP-12)→ A0,mem32(SP-16)→ A1, mem32(SP-20)→ MDR,mem32(SP-24)→ LIR, mem32(SP-28)→ LAR	-	-	-	-	3	8																registers specified with regs = 7
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg1,mem32(SP-8)→ D0, mem32(SP-12)→ D1,mem32(SP-16)→ → A0, mem32(SP-20)→ A1,mem32(SP-24)→ MDR, mem32(SP-28)→ LIR,mem32(SP-32)→ LAR,	-	-	-	-	3	9																registers specified with regs = 8

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
RETF	RETF	SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ D0,mem32(SP-16)→ D1, mem32(SP-20)→ A0,mem32(SP-24)→ A1, mem32(SP-28)→ MDR,mem32(SP-32)→ LIR, mem32(SP-36)→ LAR	-	-	-	-	3	10	S2	1101	1110	<regs ....>		<imm8 ....>										registers specified with regs = 9
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ reg1,mem32(SP-8)→ reg2, mem32(SP-12)→ reg3,mem32(SP-16)→ D0, mem32(SP-20)→ D1,mem32(SP-24)→ A0, mem32(SP-28)→ A1,mem32(SP-32)→ MDR, mem32(SP-36)→ LIR,mem32(SP-40)→ LAR,	-	-	-	-	3	11																registers specified with regs= 10
		SP + imm8(zero_ext) → SP,MDR → PC, mem32(SP-4)→ D2,mem32(SP-8)→ D3, mem32(SP-12)→ A2,mem32(SP-16)→ A3, mem32(SP-20)→ D0,mem32(SP-24)→ D1, mem32(SP-28)→ A0,mem32(SP-32)→ A1, mem32(SP-36)→ MDR,mem32(SP-40)→ LIR, mem32(SP-44)→ LAR	-	-	-	-	3	10																registers specified with regs= 11
RETS	RETS	mem32(SP) → PC	-	-	-	-	2	5*	D0	1111	0000	1111	1100											*: 4 cycles for AM30
JSR	JSR (An)	SP - 4 → SP,PC + 2 → mem32(SP) PC + 2 → MDR,An → PC, (execute subroutine) SP + 4 → SP	●	●	●	●	8	5																
	JSR label	IF (label = (d16,PC)), SP - 4 → SP,PC + 4 → mem32(SP), PC + 4 → MDR,PC + d16 (sign_ext) → PC (execute subroutine) SP+4 → SP	●	●	●	●	10	5																
		IF (label = (d32,PC)), SP - 4 → SP,PC + 6 → (SP+3), PC + 6 → MDR,PC + d32 → PC (execute subroutine) SP+4 → SP	●	●	●	●	12	5*																*: 6 cycles for AM30
RTS	RTS	mem32(SP) → PC	-	-	-	-	2	4	D0	1111	0000	1111	1101											
RTI	RTI	mem16(SP) → PSW,mem32(SP+4) → PC, SP + 8 → SP	●	●	●	●	2	4																
TRAP	TRAP	PC + 2 → mem32(SP),0x40000010 → PC	-	-	-	-	2	4	D0	1111	0000	1111	1110											
NOP	NOP	PC + 1 → PC	-	-	-	-	1	1	S0	1100	1011													

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code													Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Extension Instructions																								
UDF	UDF00 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0000	DmDn											
	UDF01 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0001	DmDn											
	UDF02 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0010	DmDn											
	UDF03 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0011	DmDn											
	UDF04 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0100	DmDn											
	UDF05 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0101	DmDn											
	UDF06 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0110	DmDn											
	UDF07 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	0111	DmDn											
	UDF08 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1000	DmDn											
	UDF09 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1001	DmDn											
	UDF10 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1010	DmDn											
	UDF11 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1011	DmDn											
	UDF12 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1100	DmDn											
	UDF13 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1101	DmDn											
	UDF14 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1110	DmDn											
	UDF15 Dm,Dn	Dm op Dn → Dn	*	*	*	*	2	*	D0	1111	0110	1111	DmDn											
	UDF20 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0000	DmDn											
	UDF21 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0001	DmDn											
	UDF22 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0010	DmDn											
	UDF23 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0011	DmDn											
	UDF24 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0100	DmDn											
	UDF25 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0101	DmDn											
	UDF26 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0110	DmDn											
	UDF27 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	0111	DmDn											
	UDF28 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1000	DmDn											
	UDF29 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1001	DmDn											
	UDF30 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1010	DmDn											
	UDF31 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1011	DmDn											
	UDF32 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1100	DmDn											
	UDF33 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1101	DmDn											
	UDF34 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1110	DmDn											
	UDF35 Dm,Dn	Dm op Dn	-	-	-	-	2	*	D0	1111	0101	1111	DmDn											
	UDF00 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0000	00Dn	<imm8 ....>										
	UDF01 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0001	00Dn	<imm8 ....>										
	UDF02 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0010	00Dn	<imm8 ....>										
	UDF03 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0011	00Dn	<imm8 ....>										
	UDF04 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0100	00Dn	<imm8 ....>										
	UDF05 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0101	00Dn	<imm8 ....>										
	UDF06 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0110	00Dn	<imm8 ....>										

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
UDFnn	UDF07 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	0111	00Dn	<imm8....>										
	UDF08 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1000	00Dn	<imm8....>										
	UDF09 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1001	00Dn	<imm8....>										
	UDF10 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1010	00Dn	<imm8....>										
	UDF11 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1011	00Dn	<imm8....>										
	UDF12 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1100	00Dn	<imm8....>										
	UDF13 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1101	00Dn	<imm8....>										
	UDF14 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1110	00Dn	<imm8....>										
	UDF15 imm8,Dn	imm8(sign_ext) op Dn → Dn	*	*	*	*	3	*	D1	1111	1001	1111	00Dn	<imm8....>										
	UDF20 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0000	10Dn	<imm8....>										Not used for AM30
	UDF21 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0001	10Dn	<imm8....>										Not used for AM30
	UDF22 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0010	10Dn	<imm8....>										Not used for AM30
	UDF23 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0011	10Dn	<imm8....>										Not used for AM30
	UDF24 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0100	10Dn	<imm8....>										Not used for AM30
	UDF25 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0101	10Dn	<imm8....>										Not used for AM30
	UDF26 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0110	10Dn	<imm8....>										Not used for AM30
	UDF27 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0111	10Dn	<imm8....>										Not used for AM30
	UDF28 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1000	10Dn	<imm8....>										Not used for AM30
	UDF29 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1001	10Dn	<imm8....>										Not used for AM30
	UDF30 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1010	10Dn	<imm8....>										Not used for AM30
	UDF31 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1011	10Dn	<imm8....>										Not used for AM30
	UDF32 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1100	10Dn	<imm8....>										Not used for AM30
	UDF33 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1101	10Dn	<imm8....>										Not used for AM30
	UDF34 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1110	10Dn	<imm8....>										Not used for AM30
	UDF35 imm8,Dn	imm8(sign_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1111	10Dn	<imm8....>										Not used for AM30
	UDF00 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0000	00Dn	<imm16...	....	....>								
	UDF01 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0001	00Dn	<imm16...	....	....>								
	UDF02 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0010	00Dn	<imm16...	....	....>								
	UDF03 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0011	00Dn	<imm16...	....	....>								
	UDF04 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0100	00Dn	<imm16...	....	....>								
	UDF05 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0101	00Dn	<imm16...	....	....>								
	UDF06 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0110	00Dn	<imm16...	....	....>								
	UDF07 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0111	00Dn	<imm16...	....	....>								
	UDF08 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1000	00Dn	<imm16...	....	....>								
	UDF09 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1001	00Dn	<imm16...	....	....>								
	UDF10 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1010	00Dn	<imm16...	....	....>								
	UDF11 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1011	00Dn	<imm16...	....	....>								
	UDF12 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1100	00Dn	<imm16...	....	....>								
	UDF13 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1101	00Dn	<imm16...	....	....>								
	UDF14 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1110	00Dn	<imm16...	....	....>								
	UDF15 imm16,Dn	imm16(sign_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1111	00Dn	<imm16...	....	....>								

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
UDFnn	UDF20 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0000	10Dn	<imm16...	....	....>								Not used for AM30
	UDF21 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0001	10Dn	<imm16...	....	....>								Not used for AM30
	UDF22 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0010	10Dn	<imm16...	....	....>								Not used for AM30
	UDF23 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0011	10Dn	<imm16...	....	....>								Not used for AM30
	UDF24 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0100	10Dn	<imm16...	....	....>								Not used for AM30
	UDF25 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0101	10Dn	<imm16...	....	....>								Not used for AM30
	UDF26 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0110	10Dn	<imm16...	....	....>								Not used for AM30
	UDF27 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0111	10Dn	<imm16...	....	....>								Not used for AM30
	UDF28 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1000	10Dn	<imm16...	....	....>								Not used for AM30
	UDF29 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1001	10Dn	<imm16...	....	....>								Not used for AM30
	UDF30 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1010	10Dn	<imm16...	....	....>								Not used for AM30
	UDF31 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1011	10Dn	<imm16...	....	....>								Not used for AM30
	UDF32 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1100	10Dn	<imm16...	....	....>								Not used for AM30
	UDF33 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1101	10Dn	<imm16...	....	....>								Not used for AM30
	UDF34 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1110	10Dn	<imm16...	....	....>								Not used for AM30
	UDF35 imm16,Dn	imm16(sign_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1111	10Dn	<imm16...	....	....>				....				Not used for AM30
	UDF00 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0000	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF01 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0001	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF02 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0010	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF03 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0011	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF04 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0100	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF05 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0101	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF06 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0110	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF07 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0111	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF08 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1000	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF09 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1001	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF10 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1010	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF11 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1011	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF12 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1100	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF13 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1101	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF14 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1110	00Dn	<imm32...	....	....	....	....	....	..	....>			
	UDF15 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1111	00Dn	<imm32...	....	....	....	....	....	....	....>			
	UDF20 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0000	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF21 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0001	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF22 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0010	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF23 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0011	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF24 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0100	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF25 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0101	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF26 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0110	10Dn	<imm32...	....	....	....	....	....	.....	....>			Not used for AM30
	UDF27 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0111	10Dn	<imm32...	....	....	....	....			....>			Not used for AM30

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
																....								
UDFnn	UDF28 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1000	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF29 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1001	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF30 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1010	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF31 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1011	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF32 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1100	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF33 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1101	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF34 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1110	10Dn	<imm32...	....	....	....	....	....	....	....>			Not used for AM30
	UDF35 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1111	10Dn	<imm32...		....	....	....	....	....	....>			Not used for AM30
UDFUnn	UDFU00 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0000	01Dn	<imm8 ....>										
	UDFU01 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0001	01Dn	<imm8 ....>										
	UDFU02 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0010	01Dn	<imm8 ....>										
	UDFU03 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0011	01Dn	<imm8 ....>										
	UDFU04 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0100	01Dn	<imm8 ....>										
	UDFU05 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0101	01Dn	<imm8 ....>										
	UDFU06 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0110	01Dn	<imm8 ....>										
	UDFU07 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	0111	01Dn	<imm8 ....>										
	UDFU08 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1000	01Dn	<imm8 ....>										
	UDFU09 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1001	01Dn	<imm8 ....>										
	UDFU10 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1010	01Dn	<imm8 ....>										
	UDFU11 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1011	01Dn	<imm8 ....>										
	UDFU12 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1100	01Dn	<imm8 ....>										
	UDFU13 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1101	01Dn	<imm8 ....>										
	UDFU14 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1110	01Dn	<imm8 ....>										
	UDFU15 imm8,Dn	imm8(zero_ext) op Dn →Dn	*	*	*	*	3	*	D1	1111	1001	1111	01Dn	<imm8 ....>										
	UDFU20 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0000	11Dn	<imm8 ....>										Not used for AM30
	UDFU21 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0001	11Dn	<imm8 ....>										Not used for AM30
	UDFU22 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0010	11Dn	<imm8 ....>										Not used for AM30
	UDFU23 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0011	11Dn	<imm8 ....>										Not used for AM30
	UDFU24 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0100	11Dn	<imm8 ....>										Not used for AM30
	UDFU25 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0101	11Dn	<imm8 ....>										Not used for AM30
	UDFU26 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0110	11Dn	<imm8 ....>										Not used for AM30
	UDFU27 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	0111	11Dn	<imm8 ....>										Not used for AM30
	UDFU28 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1000	11Dn	<imm8 ....>										Not used for AM30
	UDFU29 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1001	11Dn	<imm8 ....>										Not used for AM30
	UDFU30 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1010	11Dn	<imm8 ....>										Not used for AM30
	UDFU31 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1011	11Dn	<imm8 ....>										Not used for AM30
	UDFU32 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1100	11Dn	<imm8 ....>										Not used for AM30
	UDFU33 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1101	11Dn	<imm8 ....>										Not used for AM30
	UDFU34 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1110	11Dn	<imm8 ....>										Not used for AM30
	UDFU35 imm8,Dn	imm8(zero_ext) op Dn	-	-	-	-	3	*	D1	1111	1001	1111	11Dn	<imm8 ....>										Not used for AM30

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code														Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
UDFUnn	UDFU00 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0000	01Dn	<imm16...	....	....>								
	UDFU01 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0001	01Dn	<imm16...	....	....>								
	UDFU02 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0010	01Dn	<imm16...	....	....>								
	UDFU03 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0011	01Dn	<imm16...	....	....>								
	UDFU04 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0100	01Dn	<imm16...	....	....>								
	UDFU05 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0101	01Dn	<imm16...	....	....>								
	UDFU06 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0110	01Dn	<imm16...	....	....>								
	UDFU07 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	0111	01Dn	<imm16...	....	....>								
	UDFU08 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1000	01Dn	<imm16...	....	....>								
	UDFU09 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1001	01Dn	<imm16...	....	....>								
	UDFU10 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1010	01Dn	<imm16...	....	....>								
	UDFU11 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1011	01Dn	<imm16...	....	....>								
	UDFU12 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1100	01Dn	<imm16...	....	....>								
	UDFU13 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1101	01Dn	<imm16...	....	....>								
	UDFU14 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1110	01Dn	<imm16...	....	....>								
	UDFU15 imm16,Dn	imm16(zero_ext) op Dn → Dn	*	*	*	*	4	*	D2	1111	1011	1111	01Dn	<imm16...	....	....>								
	UDFU20 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0000	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU21 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0001	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU22 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0010	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU23 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0011	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU24 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0100	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU25 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0101	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU26 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0110	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU27 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	0111	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU28 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1000	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU29 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1001	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU30 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1010	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU31 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1011	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU32 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1100	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU33 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1101	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU34 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1110	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU35 imm16,Dn	imm16(zero_ext) op Dn	-	-	-	-	4	*	D2	1111	1011	1111	11Dn	<imm16...	....	....>								Not used for AM30
	UDFU00 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0000	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU01 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0001	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU02 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0010	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU03 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0011	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU04 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0100	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU05 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0101	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU06 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0110	01Dn	<imm32...	....	....	....	....	....	....	....>			
	UDFU07 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	0111	01Dn	<imm32...	....	....	....	....	....	....	....>			

MN1030/MN103S SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	For -mat	Machine Code													Notes
			VF	CF	NF	ZF				1	2	3	4	5	6	7	8	9	10	11	12	13	14	
UDFUnn	UDFU08 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1000	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU09 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1001	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU10 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1010	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU11 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1011	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU12 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1100	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU13 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1101	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU14 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1110	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU15 imm32,Dn	imm32 op Dn → Dn	*	*	*	*	6	*	D4	1111	1101	1111	01Dn	<imm32...	....	....	....	....	....	....>			
	UDFU20 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0000	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU21 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0001	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU22 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0010	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU23 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0011	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU24 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0100	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU25 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0101	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU26 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0110	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU27 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	0111	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU28 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1000	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU29 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1001	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU30 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1010	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU31 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1011	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU32 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1100	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU33 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1101	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU34 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1110	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30
	UDFU35 imm32,Dn	imm32 op Dn	-	-	-	-	6	*	D4	1111	1101	1111	11Dn	<imm32...	....	....	....	....	....	....>			Not used for AM30

MN1030/MN103S SERIES INSTRUCTION SET

INSTRUCTION SET

■ Description

Dn,Dm,Di	data registers
An,Am	address registers
MDR	multiply/divide register
PSW	processor status word
PC	program counter
SP	stack pointer
LIR	loop instruction registers
LAR	loop address registers
imm8,imm16,imm32	immediate value(8, 16 or 32 bits)
d8,d16,d32	displacement(8, 16 or 32 bits)
abs16,abs32	absolute address (16 or 32 bits)
mem8(An)	lower 8-bit data in memory referred by () address
mem16(An)	lower 16bit data in memory referred by ()address
mem32(An)	lower 32-bit data in memory referred by () address
regs	registers
.lsb,.msb	bit location(lowest/highest)
&	logical AND
|	logical OR
^	exclusive OR
~	bit inverted
op	operation defined by users
<<,>>	bit shift(right/left)
	performsa bit shift for specified value
VF	overflow flags
CF	carry flags
NF	negative flags
ZF	zero flags
temp	temporary registers
→	move
:	reflects operation result
(sign_ext)	sign-extend
(zero_ext)	zero-extend
{MDR,Dn}	64-bit data defined whose upper 32-bit data are in MDR and lower 32-bit in register Dn within "{}".
0x....	hexadecimal(hexadecimal following to 0x.)

■ Flag

●	changes
-	no changes
0	always 0
1	alwayas 1
?	not defined
*	defined by users

■ CodeSize

byte:

■ Cycles

Cycles may be changed the status of the pipline, memory space to access.

Cycles are calculated on those conditions;

(1) no pipeline installation

(2) Instruction queue: 2 cycles

data load/store: 1 cycle

(ROM/RAM/ internal flash:

Instructions: access to internal ROM/RAM space

data: access to internal RAM space

with cache

Instructions/data :access to cachable area and hit the chache)

Please see the LSI manuals for how the pipeline installation affects the cycles.

If using extended instructions, the users define the cycles.

■ Format

Please refer to “Chapter 1, 6 Instruction Formats” in MN1030/MN103S Instruction Manual.

■ IInstructions replaced to other instructions by Assembler

Format or Mchine Codeare not written

usable CodeSize and Cycles are written

MOVB Reg,Mem , MOVH Reg,Mem,

ASR Dn , LSR Dn , RTS

■ Instructions replaced to multiple instructions by Assembler

Format or Mchine Code are not written

usable CodeSize and Cycles are written

MOVB Mem,Reg , MOVH Reg,Mem ,

JSR (An) , JSR label

16.3 Instruction Map

1st byte

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CLR D0	MOV D0,(abs16)	MOVBU D0,(abs16)	MOVHU D0,(abs16)	CLR D1	MOV D1,(abs16)	MOVBU D1,(abs16)	MOVHU D1,(abs16)	CLR D2	MOV D2,(abs16)	MOVBU D2,(abs16)	MOVHU D2,(abs16)	CLR D3	MOV D3,(abs16)	MOVBU D3,(abs16)	MOVHU D3,(abs16)
1	EXTB Dn				EXTBU Dn				EXTH Dn				EXTHU Dn			
2	ADD imm8,An				MOV imm16,An				ADD imm8,Dn				MOV imm16,Dn			
3	MOV (abs16),Dn				MOVBU (abs16),Dn				MOVHU (abs16),Dn				MOV SP,An			
4	INC D0	INC A0	MOV D0,(d8,SP)	MOV A0,(d8,SP)	INC D1	INC A1	MOV D1,(d8,SP)	MOV A1,(d8,SP)	INC D2	INC A2	MOV D2,(d8,SP)	MOV A2,(d8,SP)	INC D3	INC A3	MOV D3,(d8,SP)	MOV A3,(d8,SP)
5	INC4 An				ASL2 Dn				MOV (d8,SP),Dn				MOV (d8,SP),An			
6	MOV Dm,(An)															
7	MOV (Am),Dn															
8	MOV Dm,Dn (If m=nMOV, imm8,Dn)															
9	MOV Am,An (If m=nMOV, imm8,An)															
A	CMP Dm,Dn (If m=n, CMP imm8,Dn)															
B	CMP Am,An (If m=n, CMP imm8,An)															
C	BLT (d8,PC)	BGT (d8,PC)	BGE (d8,PC)	BLE (d8,PC)	BCS (d8,PC)	BHI (d8,PC)	BCC (d8,PC)	BLS (d8,PC)	BEQ (d8,PC)	BNE (d8,PC)	BRA (d8,PC)	NOP	JMP (d16,PC)	CALL (d16,PC)	MOVM (SP),regs	MOVM regs,(SP)
D	LLT	LGT	LGE	LLE	LCS	LHI	LCC	LLS	LEQ	LNE	LRA	SETLB	JMP (d32,PC)	CALL (d32,PC)	RETF	RET
E	ADD Dm,Dn															
F	Code extension (2-byte)								Code extension (3-byte)		Code extension		Code extension (6-byte)		Code extension (7-byte)	

2nd byte (1st byte:F0) Instruction for 2-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV (Am),An															
1	MOV Am,(An)															
2																
3																
4	MOVBU (Am),Dn															
5	MOVBU Dm,(An)															
6	MOVHU (Am),Dn															
7	MOVHU Dm,(An)															
8	BSET Dm,(An)															
9	BCLR Dm,(An)															
A																
B																
C																
D																
E																
F	CALLS (An)				JMP (An)								RETS	RTI	TRAP	

2nd byte (1st byte: F1)) Instruction for 2-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	SUB Dm,Dn															
1	SUB Am,Dn															
2	SUB Dm,An															
3	SUB Am,An															
4	ADDC Dm,Dn															
5	ADD Am,Dn															
6	ADD Dm,An															
7	ADD Am,An															
8	SUBC Dm,Dn															
9	CMP Am,Dn															
A	CMP Dm,An															
B																
C																
D	MOV Am,Dn															
E	MOV Dm,An															
F																

2nd byte(1st byte:F2) Instruction for 2-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND Dm,Dn															
1	OR Dm,Dn															
2	XOR Dm,Dn															
3	NOT Dn															
4	MUL Dm,Dn															
5	MULU Dm,Dn															
6	DIV Dm,Dn															
7	DIVU Dm,Dn															
8	ROL Dn				ROR Dn											
9	ASL Dm,Dn															
A	LSR Dm,Dn															
B	ASR Dm,Dn															
C																
D	EXT Dn															
E	MOV MDR,Dn				MOV PSW,Dn											
F	MOV A0,SP		MOV D0,MDR	MOV D0,PSW	MOV A1,SP		MOV D1,MDR	MOV D1,PSW	MOV A2,SP		MOV D2,MDR	MOV D2,PSW	MOV A3,SP		MOV D3,MDR	MOV D3,PSW

2nd byte (1st byte: F3) Instructions for 2-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 2 3	MOV (Di,Am),Dn															
4 5 6 7	MOV Dm,(Di,An)															
8 9 A B	MOV (Di,Am),An															
C D E F	MOV Am,(Di,An)															

2nd byte(1st byte: F4) Instruction for 2-byte)

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 2 3	MOVBU (Di,Am),Dn															
4 5 6 7	MOVBU Dm,(Di,An)															
8 9 A B	MOVHU (Di,Am),Dn															
C D E F	MOVHU Dm,(Di,An)															

2nd byte(1st byte:F5) Instruction for 2-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	UDF20 Dm,Dn															
1	UDF21 Dm,Dn															
2	UDF22 Dm,Dn															
3	UDF23 Dm,Dn															
4	UDF24 Dm,Dn															
5	UDF25 Dm,Dn															
6	UDF26 Dm,Dn															
7	UDF27 Dm,Dn															
8	UDF28 Dm,Dn															
9	UDF29 Dm,Dn															
A	UDF30 Dm,Dn															
B	UDF31 Dm,Dn															
C	UDF32 Dm,Dn															
D	UDF33 Dm,Dn															
E	UDF34 Dm,Dn															
F	UDF35 Dm,Dn															

2nd byte (1st byte: F6) Instruction for 2-byte)

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	UDF00 Dm,Dn															
1	UDF01 Dm,Dn															
2	UDF02 Dm,Dn															
3	UDF03 Dm,Dn															
4	UDF04 Dm,Dn															
5	UDF05 Dm,Dn															
6	UDF06 Dm,Dn															
7	UDF07 Dm,Dn															
8	UDF08 Dm,Dn															
9	UDF09 Dm,Dn															
A	UDF10 Dm,Dn															
B	UDF11 Dm,Dn															
C	UDF12 Dm,Dn															
D	UDF13 Dm,Dn															
E	UDF14 Dm,Dn															
F	UDF15 Dm,Dn															

2nd byte (1st byte:F8) Instruction for 3-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV (d8,Am),Dn															
1	MOV Dm,(d8,An)															
2	MOV (d8,Am),An															
3	MOV Am,(d8,An)															
4	MOVBU (d8,Am),Dn															
5	MOVBU Dm,(d8,An)															
6	MOVHU (d8,Am),Dn															
7	MOVHU Dm,(d8,An)															
8																
9		MOVBU D0,(d8,SP)	MOVHU D0,(d8,SP)			MOVBU D1,(d8,SP)	MOVHU D1,(d8,SP)			MOVBU D2,(d8,SP)	MOVHU D2,(d8,SP)			MOVBU D3,(d8,SP)	MOVHU D3,(d8,SP)	
A																
B									MOVBU (d8,SP),Dn				MOVHU (d8,SP),Dn			
C	ASL imm8,Dn				LSR imm8,Dn				ASR imm8,Dn							
D																
E	AND imm8,Dn				OR imm8,Dn				BVC (d8,PC)	BVS (d8,PC)	BNC (d8,PC)	BNS (d8,PC)	BTST imm8,Dn			
F	MOV (d8,An),SP				MOV SP,(d8,An)										ADD imm8,SP	

2nd byte (1st byte:F9) Instruction for 3-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	UDF00 imm8,Dn				UDFU00 imm8,Dn				UDF20 imm8,Dn*				UDFU20 imm8,Dn*			
1	UDF01 imm8,Dn				UDFU01 imm8,Dn				UDF21 imm8,Dn*				UDFU21 imm8,Dn*			
2	UDF02 imm8,Dn				UDFU02 imm8,Dn				UDF22 imm8,Dn*				UDFU22 imm8,Dn*			
3	UDF03 imm8,Dn				UDFU03 imm8,Dn				UDF23 imm8,Dn*				UDFU23 imm8,Dn*			
4	UDF04 imm8,Dn				UDFU04 imm8,Dn				UDF24 imm8,Dn*				UDFU24 imm8,Dn*			
5	UDF05 imm8,Dn				UDFU05 imm8,Dn				UDF25 imm8,Dn*				UDFU25 imm8,Dn*			
6	UDF06 imm8,Dn				UDFU06 imm8,Dn				UDF26 imm8,Dn*				UDFU26 imm8,Dn*			
7	UDF07 imm8,Dn				UDFU07 imm8,Dn				UDF27 imm8,Dn*				UDFU27 imm8,Dn*			
8	UDF08 imm8,Dn				UDFU08 imm8,Dn				UDF28 imm8,Dn*				UDFU28 imm8,Dn*			
9	UDF09 imm8,Dn				UDFU09 imm8,Dn				UDF29 imm8,Dn*				UDFU29 imm8,Dn*			
A	UDF10 imm8,Dn				UDFU10 imm8,Dn				UDF30 imm8,Dn*				UDFU30 imm8,Dn*			
B	UDF11 imm8,Dn				UDFU11 imm8,Dn				UDF31 imm8,Dn*				UDFU31 imm8,Dn*			
C	UDF12 imm8,Dn				UDFU12 imm8,Dn				UDF32 imm8,Dn*				UDFU32 imm8,Dn*			
D	UDF13 imm8,Dn				UDFU13 imm8,Dn				UDF33 imm8,Dn*				UDFU33 imm8,Dn*			
E	UDF14 imm8,Dn				UDFU14 imm8,Dn				UDF34 imm8,Dn*				UDFU34 imm8,Dn*			
F	UDF15 imm8,Dn				UDFU15 imm8,Dn				UDF35 imm8,Dn*				UDFU35 imm8,Dn*			

*: Installed for AM30/AM32. Not used for AM30.

2nd byte (1st byte: F4) Instruction for 4-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV (d16,Am),Dn															
1	MOV Dm,(d16,An)															
2	MOV (d16,Am),An															
3	MOV Am,(d16,An)															
4	MOVBU (d16,Am),Dn															
5	MOVBU Dm,(d16,An)															
6	MOVHU (d16,Am),Dn															
7	MOVHU Dm,(d16,An)															
8	MOV A0,(abs16)				MOV A1,(abs16)				MOV A2,(abs16)				MOV A3,(abs16)			
9	MOV A0,(d16,SP)	MOV D0,(d16,SP)	MOVBU D0,(d16,SP)	MOVHU D0,(d16,SP)	MOV A1,(d16,SP)	MOV D1,(d16,SP)	MOVBU D1,(d16,SP)	MOVHU D1,(d16,SP)	MOV A2,(d16,SP)	MOV D2,(d16,SP)	MOVBU D2,(d16,SP)	MOVHU D2,(d16,SP)	MOV A3,(d16,SP)	MOV D3,(d16,SP)	MOVBU D3,(d16,SP)	MOVHU D3,(d16,SP)
A	MOV (abs16),An															
B	MOV (d16,SP),An				MOV (d16,SP),Dn				MOVBU (d16,SP),Dn				MOVHU (d16,SP),Dn			
C	ADD imm16,Dn								CMP imm16,Dn							
D	ADD imm16,An								CMP imm16,An							
E	AND imm16,Dn				OR imm16,Dn				XOR imm16,Dn				BTST imm16,Dn			
F	BSET imm8,(d8,An)				BCLR imm8,(d8,An)				BTST imm8,(d8,An)				AND imm16,PSW	OR imm16,PSW	ADD imm16,SP	CALLS (d16,PC)

2nd byte (1st byte: FB) Instruction for 4-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	UDF00 imm16,Dn				UDFU00 imm16,Dn				UDF20 imm16,Dn*				UDFU20 imm16,Dn*			
1	UDF01 imm16,Dn				UDFU01 imm16,Dn				UDF21 imm16,Dn*				UDFU21 imm16,Dn*			
2	UDF02 imm16,Dn				UDFU02 imm16,Dn				UDF22 imm16,Dn*				UDFU22 imm16,Dn*			
3	UDF03 imm16,Dn				UDFU03 imm16,Dn				UDF23 imm16,Dn*				UDFU23 imm16,Dn*			
4	UDF04 imm16,Dn				UDFU04 imm16,Dn				UDF24 imm16,Dn*				UDFU24 imm16,Dn*			
5	UDF05 imm16,Dn				UDFU05 imm16,Dn				UDF25 imm16,Dn*				UDFU25 imm16,Dn*			
6	UDF06 imm16,Dn				UDFU06 imm16,Dn				UDF26 imm16,Dn*				UDFU26 imm16,Dn*			
7	UDF07 imm16,Dn				UDFU07 imm16,Dn				UDF27 imm16,Dn*				UDFU27 imm16,Dn*			
8	UDF08 imm16,Dn				UDFU08 imm16,Dn				UDF28 imm16,Dn*				UDFU28 imm16,Dn*			
9	UDF09 imm16,Dn				UDFU09 imm16,Dn				UDF29 imm16,Dn*				UDFU29 imm16,Dn*			
A	UDF10 imm16,Dn				UDFU10 imm16,Dn				UDF30 imm16,Dn*				UDFU30 imm16,Dn*			
B	UDF11 imm16,Dn				UDFU11 imm16,Dn				UDF31 imm16,Dn*				UDFU31 imm16,Dn*			
C	UDF12 imm16,Dn				UDFU12 imm16,Dn				UDF32 imm16,Dn*				UDFU32 imm16,Dn*			
D	UDF13 imm16,Dn				UDFU13 imm16,Dn				UDF33 imm16,Dn*				UDFU33 imm16,Dn*			
E	UDF14 imm16,Dn				UDFU14 imm16,Dn				UDF34 imm16,Dn*				UDFU34 imm16,Dn*			
F	UDF15 imm16,Dn				UDFU15 imm16,Dn				UDF35 imm16,Dn*				UDFU35 imm16,Dn*			

*: Installed for AM31/AM32. Not used for AM30.

2nd byte (1st byte: FC) Instruction for 6-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV (d32,Am),Dn															
1	MOV Dm,(d32,An)															
2	MOV (d32,Am),An															
3	MOV Am,(d32,An)															
4	MOVBU (d32,Am),Dn															
5	MOVBU Dm,(d32,An)															
6	MOVHU (d32,Am),Dn															
7	MOVHU Dm,(d32,An)															
8	MOV A0,(abs32)	MOV D0,(abs32)	MOVBU D0,(abs32)	MOVHU D0,(abs32)	MOV A1,(abs32)	MOV D1,(abs32)	MOVBU D1,(abs32)	MOVHU D1,(abs32)	MOV A2,(abs32)	MOV D2,(abs32)	MOVBU D2,(abs32)	MOVHU D2,(abs32)	MOV A3(abs32)	MOV D3,(abs32)	MOVBU D3,(abs32)	MOVHU D3,(abs32)
9	MOV A0,(d32,SP)	MOV D0,(d32,SP)	MOVBU D0,(d32,SP)	MOVHU D0,(d32,SP)	MOV A1,(d32,SP)	MOV D1,(d32,SP)	MOVBU D1,(d32,SP)	MOVHU D1,(d32,SP)	MOV A2,(d32,SP)	MOV D2,(d32,SP)	MOVBU D2,(d32,SP)	MOVHU D2,(d32,SP)	MOV A3,(d32,SP)	MOV D3,(d32,SP)	MOVBU D3,(d32,SP)	MOVHU D3,(d32,SP)
A	MOV (abs32),An				MOV (abs32),Dn				MOVBU (abs32),Dn				MOVHU (abs32),Dn			
B	MOV (d32,SP),An				MOV (d32,SP),Dn				MOVBU (d32,SP),Dn				MOVHU (d32,SP),Dn			
C	ADD imm32,Dn				SUB imm32,Dn				CMP imm32,Dn				MOV imm32,Dn			
D	ADD imm32,An				SUB imm32,An				CMP imm32,An				MOV imm32,An			
E	AND imm32,Dn				OR imm32,Dn				XOR imm32,Dn				BTST imm32,Dn			
F															ADD imm32,SP	CALLS (d32,PC)

2nd byte (1st byte: FD) Instruction for 6-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	UDF00 imm32,Dn				UDFU00 imm32,Dn				UDF20 imm32,Dn*				UDFU20 imm32,Dn*			
1	UDF01 imm32,Dn				UDFU01 imm32,Dn				UDF21 imm32,Dn*				UDFU21 imm32,Dn*			
2	UDF02 imm32,Dn				UDFU02 imm32,Dn				UDF22 imm32,Dn*				UDFU22 imm32,Dn*			
3	UDF03 imm32,Dn				UDFU03 imm32,Dn				UDF23 imm32,Dn*				UDFU23 imm32,Dn*			
4	UDF04 imm32,Dn				UDFU04 imm32,Dn				UDF24 imm32,Dn*				UDFU24 imm32,Dn*			
5	UDF05 imm32,Dn				UDFU05 imm32,Dn				UDF25 imm32,Dn*				UDFU25 imm32,Dn*			
6	UDF06 imm32,Dn				UDFU06 imm32,Dn				UDF26 imm32,Dn*				UDFU26 imm32,Dn*			
7	UDF07 imm32,Dn				UDFU07 imm32,Dn				UDF27 imm32,Dn*				UDFU27 imm32,Dn*			
8	UDF08 imm32,Dn				UDFU08 imm32,Dn				UDF28 imm32,Dn*				UDFU28 imm32,Dn*			
9	UDF09 imm32,Dn				UDFU09 imm32,Dn				UDF29 imm32,Dn*				UDFU29 imm32,Dn*			
A	UDF10 imm32,Dn				UDFU10 imm32,Dn				UDF30 imm32,Dn*				UDFU30 imm32,Dn*			
B	UDF11 imm32,Dn				UDFU11 imm32,Dn				UDF31 imm32,Dn*				UDFU31 imm32,Dn*			
C	UDF12 imm32,Dn				UDFU12 imm32,Dn				UDF32 imm32,Dn*				UDFU32 imm32,Dn*			
D	UDF13 imm32,Dn				UDFU13 imm32,Dn				UDF33 imm32,Dn*				UDFU33 imm32,Dn*			
E	UDF14 imm32,Dn				UDFU14 imm32,Dn				UDF34 imm32,Dn*				UDFU34 imm32,Dn*			
F	UDF15 imm32,Dn				UDFU15 imm32,Dn				UDF35 imm32,Dn*				UDFU35 imm32,Dn*			

*: Installed for AM31/AM32. Not used for AM30.

2nd byte (1st byte: FE) Instruction for 7/5-byte

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BSET imm8, (abs32)	BCLR imm8, (abs32)	BTST imm8 (abs32)													
1																
2																
3																
4																
5																
6																
7																
8	BSET imm8, (abs16)*	BCLR imm8, (abs16)*	BTST imm8, (abs16)*													
9																
A																
B																
C																
D																
E																
F																

* : Installed for AM32. Not used for AM30/AM31.

2nd byte (1st byte:F7) reserved map

Upper/lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

16.4 Extension Instruction Specification

16.4.1 Arithmetic extension function

■ Arithmetic Extension Function

The block diagram is shown below in which extension arithmetic units are connected to this series CPU core.

With the MN103S00 Series, multipliers capable of 32 × 32 multiply operation, multiply and accumulate arithmetic units capable of 32 × 32 + 64 multiply and accumulate operation, priority encoders and saturation compensation arithmetic units are incorporated as standard. Extension instructions using such extension arithmetic units are described in this section.

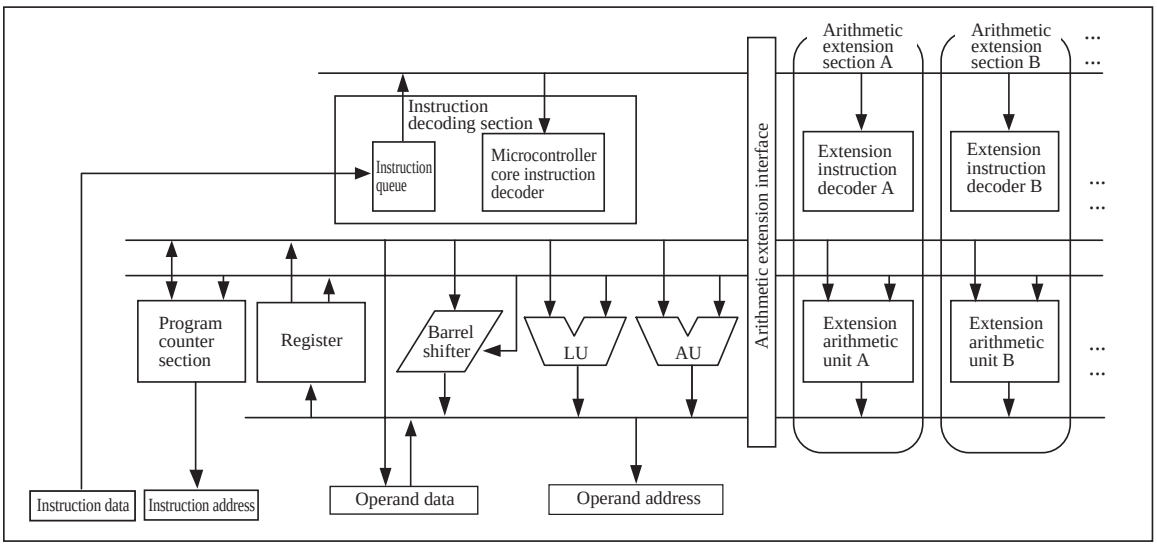


Figure:16.4.1 Block Diagram of the Extension Arithmetic Units

■ Extension Instructions

Description of symbols

Symbols used for description of extension instructions are listed below.

OP :	Instruction operation
Am, An :	Address register (m, n=3 to 0)
Dm, Dn :	Data register (m, n=3 to 0)
SP :	Stack pointer
imm :	Immediate (used in a general sense)
imm8 :	8-bit immediate
imm16 :	16-bit immediate
imm32 :	32-bit immediate
d8 :	8-bit displacement
d16 :	16-bit displacement
d32 :	32-bit displacement
abs16 :	16-bit absolute
abs32 :	32-bit absolute
MDR :	Multiply-divide register (built into core)
MDRQ :	High-speed multiply register (built into extension arithmetic unit)
MCRL :	Multiply and accumulate register (built into extension arithmetic unit)
MCRH :	Multiply and accumulate register (built into extension arithmetic unit)
MCVF :	Multiply and accumulate flag (built into extension arithmetic unit)
LIR :	Loop instruction register
LAR :	Loop address register
PSW :	Processor status word
PC :	Program counter
( ) :	Indirect addressing
regs :	Multiple registers specification
0x.... :	Hexadecimal number (number following “0x” represents hexadecimal number)

Refer to “@ Addressing Modes” for more information on indirect addressing.

The following shows symbols used in flag change tables:

- :	Flag unchanged
+ :	Flag changed
* :	Undefined
0 :	Reset
1 :	Set

Low-order 4 bits (V, C, N, Z) of PSW are collectively called “flags”.

■ Extension arithmetic unit register set

Each of the extension arithmetic units has the following dedicated registers to store high-speed multiply and multiply and accumulate results:

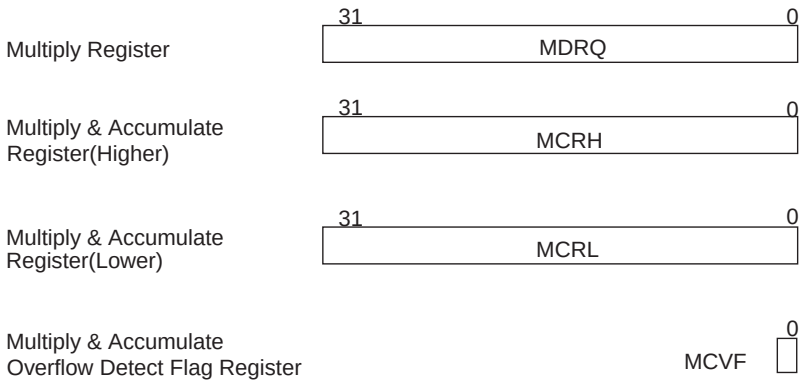


Figure:16.4.2 Extension Arithmetic Unit Register Set

Multiply register (one 32-bit register)
This register is provided for high-speed multiply instruction and stores high-order 32 bits of multiply result that is 64 bits long when multiply instruction is used.

Multiply and accumulate register (higher) (one 32-bit register)
This register is provided for multiply and accumulate instructions and stores high-order 32 bits of multiply and accumulate result that is 64 bits long when multiply and accumulate instruction is used.

Multiply and accumulate register (lower) (one 32-bit register)
This register is provided for multiply and accumulate instruction and stores low-order 32 bits of multiply and accumulate result that is 64 bits long when multiply and accumulate instruction is used.

Multiply and accumulate overflow detection flag register (one 1-bit register)
This register is set when an overflow occurs as a result of execution of multiply and accumulate instruction and is not cleared until the next CLRMAC or PUTCX instruction is executed.

■ Detailed description of extension instructions

PUTX (high-speed multiply register transfer instruction)

[Instruction format (macro name)]
PUTX Dm

[Assembler mnemonic]
udf20 Dm, Dm

[Operation]
This instruction transfers the content of Dm to the high-speed multiply register MDRQ.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

PUTCX (Multiply and accumulate register transfer instruction)

[Instruction format (macro name)]
PUTCX Dm, Dn

[Assembler mnemonic]
udf21 Dm, Dn

[Operation]
This instruction transfers the content of Dm to the multiply and accumulate register MCRH.
The register transfers the content of Dn to the multiply and accumulate register MCRL.
The instruction places the content of the V flag in the multiply and accumulate overflow detection flag register MCVF.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

GETX (high-speed multiply register transfer instruction)

[Instruction format (macro name)]
GETX Dn

[Assembler mnemonic]
udf15 Dn, Dn

[Operation]

This instruction transfers the content of the high-speed multiply register MDRQ to Dn.

[Flag changes]

Flag	Change	Condition
V	0	Always 0.
C	0	Always 0.
N	+	"1" if the MSB of the transfer result is "1." "0" in any other case.
Z	+	"1" if the transfer result is "0." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

GETCHX (transfer instruction of high-order 32 bits of multiply and accumulate register)

[Instruction format (macro name)]
GETCHX Dn

[Assembler mnemonic]
udf12 Dn, Dn

[Operation]
This instruction transfers the content of the multiply and accumulate register MCRH to Dn.
The instruction places the content of the multiply and accumulate overflow detection flag register MCVF in the V flag.

[Flag changes]

When multiply and accumulate overflow is not detected (MCVF = 0)

Flag	Change	Condition
V	0	Indicates that multiply and accumulate operation is valid.
C	0	Always 0.
N	*	Undefined
Z	*	Undefined

When multiply and accumulate overflow is detected (MCVF = 1)

Flag	Change	Condition
V	1	Indicates that multiply and accumulate operation is invalid.
C	0	Always 0.
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

GETCLX (transfer instruction of low-order 32 bits of multiply and accumulate register)

[Instruction format (macro name)]

GETCLX Dn

[Assembler mnemonic]

udf13 Dn, Dn

[Operation]

This instruction transfers the content of the multiply and accumulate register MCRL to Dn.
The instruction places the content of the multiply and accumulate overflow detection flag register MCVF in the V flag.

[Flag changes]

When multiply and accumulate overflow is not detected (MCVF = 0)

Flag	Change	Condition
V	0	Indicates that multiply and accumulate operation is valid.
C	0	Always 0.
N	*	Undefined
Z	*	Undefined

When multiply and accumulate overflow is detected (MCVF = 1)

Flag	Change	Condition
V	1	Indicates that multiply and accumulate operation is invalid.
C	0	Always 0.
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

CLRMAC (multiply and accumulate register clear instruction)

[Instruction format (macro name)]

CLRMAC

[Assembler mnemonic]

udf22 D0,D0

[Operation]

This instruction clears the multiply and accumulate registers MCRH and MCRL.
The instruction clears the multiply and accumulate overflow detection flag register MCVF.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

MULQ (signed high-speed multiply instruction: register to register)

[Instruction format (macro name)]

MULQ Dm, Dn

[Assembler mnemonic]

udf00 Dm, Dn

[Operation]

This instruction performs high-speed multiply operation by means of the multiplier provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (signed 32-bit integer: multiplicand) by the content of Dn (signed 32-bit integer: multiplier) and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the high-speed multiply register MDRQ and Dn.
The instruction determines the range within which the multiplier stored in Dn is significant (determination is made starting LSB and in units of 2 bytes) before performing operation. Only the range within which a significant value is contained is subject to multiply operation. That is, the smaller the content of Dn, the faster the operation result is obtained

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the low-order 32 bits of the result is "1." "0" in any other case.
Z	+	"1" if the low-order 32 bits of the result are "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MULQI (signed high-speed multiply instruction: immediate to register)

[Instruction format (macro name)]

MULQI imm, Dn

[Assembler mnemonic]

udf00 imm8,Dn : imm8 is sign-extended
udf00 imm16,Dn : imm16 is sign-extended
udf00 imm32,Dn

[Operation]

This instruction performs high-speed multiply operation by means of the multiplier provided in the extension arithmetic unit.
The instruction multiplies 32-bit data (multiplicand), obtained by sign-extending imm, by the content of Dn (signed 32-bit integer: multiplier) and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the high-speed multiply register MDRQ and Dn.
The instruction determines the range within which the multiplier stored in Dn is significant (determination is made starting LSB and in units of 2 bytes) before performing operation. Only the range within which a significant value is contained is subject to multiply operation. That is, the smaller the content of Dn, the faster the operation result is obtained.

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the low-order 32 bits of the result is "1." "0" in any other case.
Z	+	"1" if the low-order 32 bits of the result are "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MULQU (unsigned high-speed multiply instruction: register to register)

[Instruction format (macro name)]

MULQU Dm, Dn

[Assembler mnemonic]

udf01 Dm, Dn

[Operation]

This instruction performs high-speed multiply operation by means of the multiplier provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (unsigned 32-bit integer: multiplicand) by the content of Dn (unsigned 32-bit integer: multiplier) and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the high-speed multiply register MDRQ and Dn.
The instruction determines the range within which the multiplier stored in Dn is significant (determination is made starting LSB and in units of 2 bytes) before performing operation. Only the range within which a significant value is contained is subject to multiply operation. That is, the smaller the content of Dn, the faster the operation result is obtained.

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the low-order 32 bits of the result is "1." "0" in any other case.
Z	+	"1" if the low-order 32 bits of the result are "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MULQIU (unsigned high-speed multiply instruction: immediate to register)

[Instruction format (macro name)]

MULQIU imm, Dn

[Assembler mnemonic]

udfu01 imm8,Dn : imm8 is 0-extended
udfu01 imm16,Dn : imm16 is 0-extended
udfu01 imm32,Dn

[Operation]

This instruction performs high-speed multiply operation by means of the multiplier provided in the extension arithmetic unit.
The instruction multiplies 32-bit data (multiplicand), obtained by 0-extending imm, by the content of Dn (unsigned 32-bit integer: multiplier) and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the high-speed multiply register MDRQ and Dn.
The instruction determines the range within which the multiplier stored in Dn is significant (determination is made starting LSB and in units of 2 bytes) before performing operation. Only the range within which a significant value is contained is subject to multiply operation. That is, the smaller the content of Dn, the faster the operation result is obtained.

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the low-order 32 bits of the result is "1." "0" in any other case.
Z	+	"1" if the low-order 32 bits of the result are "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MAC (signed multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MAC Dm, Dn

[Assembler mnemonic]

udf28 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (signed 32-bit integer: multiplicand) by the content of Dn (signed 32-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 2 or more cycles must be inserted between this instruction and a next extension instruction.

MACI (signed multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACI imm, Dn

[Assembler mnemonic]

udf28 imm8, Dn : imm8 is sign-extended

udf28 imm16, Dn : imm16 is sign-extended

udf28 imm32, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies 32-bit data (multiplicand), obtained by sign-extending imm, by the content of Dn (signed 32-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 2 or more cycles must be inserted between this instruction and a next extension instruction.

MACH (signed halfword data multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MACH Dm, Dn

[Assembler mnemonic]

udf30 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (signed 16-bit integer: multiplicand) by the content of Dn (signed 16-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACIH (signed halfword data multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACIH imm, Dn

[Assembler mnemonic]

udf30 imm8, Dn : imm8 is sign-extended
udf30 imm16, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and adder provided in the extension arithmetic unit.
The instruction multiplies 16-bit data (multiplicand), obtained by sign-extending imm, by the content of Dn (signed 16-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACB (signed byte data multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MACB Dm, Dn

[Assembler mnemonic]

udf32 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (signed 8-bit integer: multiplicand) by the content of Dn (signed 8-bit integer: multiplier), adds this product to the 32-bit accumulative sum that is stored in the multiply and accumulate register MCRL and stores the 32-bit result in the multiply and accumulate register MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 32 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACIB (signed byte data multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACIB imm, Dn

[Assembler mnemonic]

udf32 imm8, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies imm 8-bit data (multiplicand) by the content of Dn (signed 8-bit integer: multiplier), adds this product to the 32-bit accumulative sum that is stored in the multiply and accumulate register MCRL and stores the 32-bit result in the multiply and accumulate register MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 32 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACU (unsigned multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MACU Dm, Dn

[Assembler mnemonic]

udf29 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (unsigned 32-bit integer: multiplicand) by the content of Dn (unsigned 32-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 2 or more cycles must be inserted between this instruction and a next extension instruction.

MACIU (unsigned multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACIU imm, Dn

[Assembler mnemonic]

udfu29 imm8, Dn : imm8 is 0-extended
udfu29 imm16, Dn : imm16 is 0-extended
udfu29 imm32, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies 32-bit data (multiplicand), obtained by 0-extending imm, by the content of Dn (signed 32-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 2 or more cycles must be inserted between this instruction and a next extension instruction.

MACHU (unsigned halfword data multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MACHU Dm, Dn

[Assembler mnemonic]

udf31 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (unsigned 16-bit integer : multiplicand) by the content of Dn (unsigned 16-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the 0 accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACIHU (unsigned halfword data multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACIHU imm, Dn

[Assembler mnemonic]

udfu31 imm8, Dn : imm8 is 0-extended
udfu31 imm16, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and adder provided in the extension arithmetic unit.
The instruction multiplies 16-bit data (multiplicand), obtained by 0-extending imm, by the content of Dn (unsigned 16-bit integer: multiplier), adds this product to the 64-bit accumulative sum whose high-order 32 bits and low-order 32 bits are stored respectively in the multiply and accumulate registers MCRH and MCRL and stores high-order 32 bits and low-order 32 bits of the 64-bit result respectively in the multiply and accumulate registers MCRH and MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 64 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACBU (unsigned byte data multiply and accumulate instruction: register to register)

[Instruction format (macro name)]

MACBU Dm, Dn

[Assembler mnemonic]

udf33 Dm, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies the content of Dm (unsigned 8-bit integer: multiplicand) by the content of Dn (unsigned 8-bit integer: multiplier), adds this product to the 32-bit accumulative sum that is stored in the multiply and accumulate register MCRL and stores the 32-bit result in the multiply and accumulate register MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 32 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

MACIBU (unsigned byte data multiply and accumulate instruction: immediate to register)

[Instruction format (macro name)]

MACIBU imm, Dn

[Assembler mnemonic]

udfu33 imm8, Dn

[Operation]

This instruction performs multiply and accumulate operation by means of the multiplier and the adder provided in the extension arithmetic unit.
The instruction multiplies imm 8-bit data (multiplicand) by the content of Dn (unsigned 8-bit integer: multiplier), adds this product to the 32-bit accumulative sum that is stored in the multiply and accumulate register MCRL and stores the 32-bit result in the multiply and accumulate register MCRL.
The register outputs a multiply and accumulate overflow detection flag “1” to the register MCVF if the accumulative sum data overflows beyond 32 bits during addition of the product and the accumulative sum.

[Flag changes]

Flag	Change	Condition
V	-	
C	-	
N	-	
Z	-	

[Note for programming]

An instruction other than extension instructions that requires 1 or more cycles must be inserted between this instruction and a next extension instruction.

SAT16(16-bit saturation instruction)

[Instruction format (macro name)]

SAT16 imm, Dn

[Assembler mnemonic]

udf04 Dm, Dn

[Operation]

This instruction stores the 16-bit signed positive maximum value (0x00007fff) and the 16-bit signed negative maximum value (0xffff8000) in Dn respectively when Dm is equal to or greater than the positive maximum value (0x00007fff) and equal to or smaller than the negative maximum value (0xffff8000). In any other case, the instruction stores the content of Dm in Dn.

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the operation result is "1." "0" in any other case.
Z	+	"1" if the operation result is "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

SAT24 (24-bit saturation instruction)

[Instruction format (macro name)]

SAT24 Dm, Dn

[Assembler mnemonic]

udf05 Dm, Dn

[Operation]

This instruction stores the 24-bit signed positive maximum value (0x007fffff) and the 24-bit signed negative maximum value (0xff800000) in Dn respectively when Dm is equal to or greater than the positive maximum value (0x007fffff) and equal to or smaller than the negative maximum value (0xff800000). In any other case, the instruction stores the content of Dm in Dn.

[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	+	"1" if the MSB of the operation result is "1." "0" in any other case.
Z	+	"1" if the operation result is "0s." "0" in any other case.

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MCST (8-, 16- and 32-bit saturation instructions for multiply and accumulate result)

[Instruction format (macro name)]

MCST32, MCST16, MCST8

[Assembler mnemonic]

udf02 Dm, Dn
udf02 imm8, Dn : Only 0x20, 0x10 and 0x08 of the imm8 value are valid

[Operation]

This instruction places the content of the multiply and accumulate overflow detection flag register MCVF in the V flag. Note also that the instruction performs the following depending on the Dm value:

1. When Dm is 32 (0x00000020)
   This instruction stores the 32-bit signed positive maximum value (0x7fffffff) and the 32-bit signed negative maximum value (0x80000000) in Dn respectively when the 64-bit multiply and accumulate result, stored in the multiply and accumulate registers MCRH and MCRL, is equal to or greater than the positive maximum value (0x000000007fffffff) and equal to or smaller than the negative maximum value (0xffffffff80000000). In any other case, the instruction stores the content of MCRL in Dn.
2. When Dm is 16 (0x00000010)
   This instruction stores the 16-bit signed positive maximum value (0x00007fff) and the 16-bit signed negative maximum value (0xffff8000) in Dn respectively when the 64-bit multiply and accumulate result, stored in the multiply and accumulate registers MCRH and MCRL, is equal to or greater than the positive maximum value (0x0000000000007fff) and equal to or smaller than the negative maximum value (0xffffffffffff8000). In any other case, the instruction stores the content of MCRL in Dn.
3. When Dm is 8 (0x00000008)
   This instruction stores the positive maximum value (0x7f) and the negative maximum value (0x80) in Dn respectively when the 32-bit multiply and accumulate result, stored in the multiply and accumulate register MCRL, is equal to or greater than the 8-bit signed positive maximum value (0x0000007f) and equal to or smaller than the 8-bit signed negative maximum value (0xffffff80). In any other case, the instruction stores the content of MCRL in Dn.
4. When Dm is any other value
   The value in Dn is undefined.

[Flag changes]

When multiply and accumulate overflow is not detected (MCVF = 0)

Flag	Change	Condition
V	0	Indicates that multiply and accumulate operation is valid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

When multiply and accumulate overflow is detected (MCVF = 1)

Flag	Change	Condition
V	1	Indicates that multiply and accumulate operation is invalid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MCST9 (9-bit saturation and positive-valuing instruction for multiply and accumulate result)

[Instruction format (macro name)]

MCST9 Dn, Dn

[Assembler mnemonic]

udf03 Dn, Dn

[Operation]

This instruction stores the positive maximum value (0xff) and “0” (0x00) in Dn respectively when the 32-bit multiply and accumulate result, stored in the multiply and accumulate register MCRL, is equal to or greater than the 9-bit signed positive maximum value (0x000000ff) and equal to or smaller than the 32-bit signed negative value (0x00000000). In any other case, the instruction places the content of the multiply and accumulate overflow detection flag register MCVF in the V flag.

[Flag changes]

When multiply and accumulate overflow is not detected (MCVF = 0)

Flag	Change	Condition
V	0	Indicates that multiply and accumulate operation is valid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

When multiply and accumulate overflow is detected (MCVF = 1)

Flag	Change	Condition
V	1	Indicates that multiply and accumulate operation is invalid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

MCST48 (48-bit saturation instruction for multiply and accumulate result)

[Instruction format (macro name)]

MCST48 Dn, Dn

[Assembler mnemonic]

udf06 Dn, Dn

[Operation]

This instruction stores the 48-bit signed positive maximum value (0x00007fffffffffff) and the negative maximum value (0xffff 800000000000) in Dn respectively when the 64-bit multiply and accumulate result, stored in the multiply and accumulate registers MCRH and MCRL, is equal to or greater than the 48-bit positive maximum value (0x00007fffffffffff) and equal to or smaller than the negative maximum value (0xffff800000000000). In any other case, the instruction outputs the contents of MCRH and MCRL and stores the values of bit 47 to bit 16 of this output in Dn.Additionally, the instruction places the content of the multiply and accumulate overflow detection flag register MCVF in the V flag.

[Flag changes]

When multiply and accumulate overflow is not detected (MCVF = 0)

Flag	Change	Condition
V	0	Indicates that multiply and accumulate operation is valid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

When multiply and accumulate overflow is detected (MCVF = 1)

Flag	Change	Condition
V	1	Indicates that multiply and accumulate operation is invalid.
C	0	Always "0".
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

BSCH (bit search instruction)

[Instruction format (macro name)]

BSCH Dm, Dn

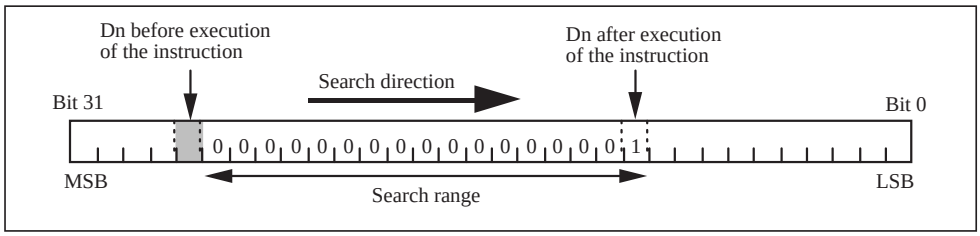
[Assembler mnemonic]

udf07 Dm, Dn

[Operation]

This instruction searches 32-bit string stored in Dm starting with the bit number specified by the content of Dn - 1 in order from larger to smaller bit numbers and stores the bit number, at which the first “1” is found, in Dn.
The instruction makes a search starting with bit 31 in order from larger to smaller bit numbers if the contents of low-order 5 bits of Dn are 0s.
If no “1” is found after search to bit 0, the instruction sets the C flag and sets Dn to “0x00000000” to terminate its execution.

Note that high-order 27 bits of Dn are ignored when the instruction execution is initiated.



[Flag changes]

When search is successful (“1” is found)

Flag	Change	Condition
V	*	Undefined
C	0	Indicates that search is successful.
N	*	Undefined
Z	*	Undefined

When search is not successful (“1” is not found)

Flag	Change	Condition
V	*	Undefined
C	1	Indicates that search is not successful.
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

SWAP (instruction for bytewise exchange of high-order and low-order bytes of 4-byte data)

[Instruction format (macro name)]

SWAP Dm, Dn

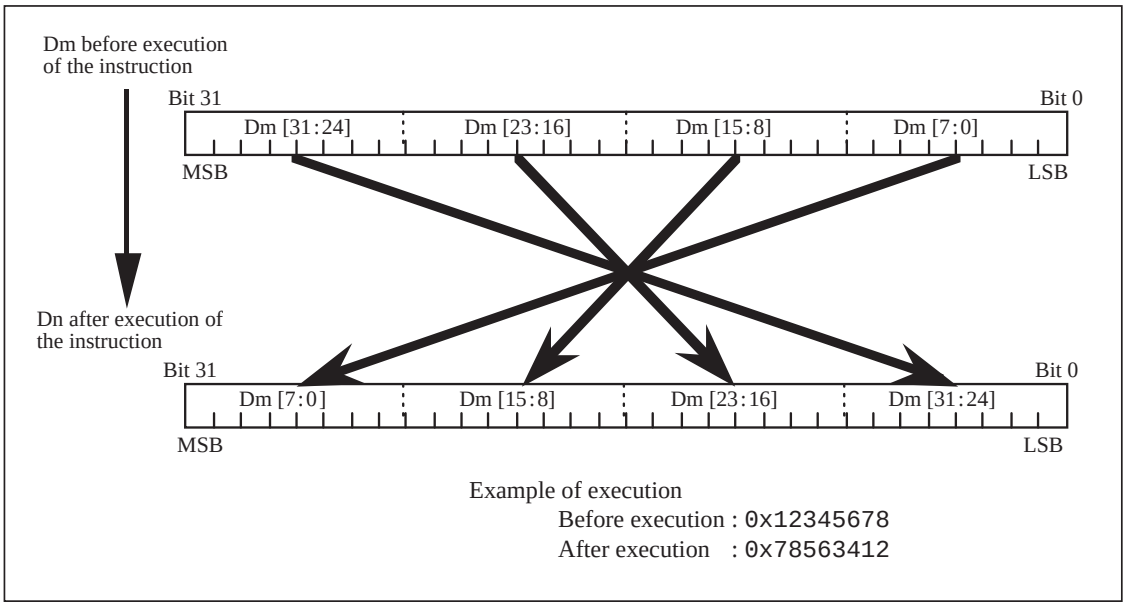
[Assembler mnemonic]

udf08 Dm, Dn

[Operation]

This instruction swaps high-order and low-order 8 bits of each of high-order and low-order 16 bits of the content of 32-bit data stored in Dm, further swaps high-order and low-order 16 bits and stores the resultant data in Dn.

Bit 32 to bit 24 of Dm are stored in bit 7 to bit 0 of Dn while bit 23 to bit 16 of Dm are stored in bit 15 to bit 8 of Dn. Bit 15 to bit 8 of Dm are stored in bit 23 to bit 16 of Dn while bit 7 to bit 0 of Dm are stored in bit 32 to bit 24 of Dn.



[Flag changes]

Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

SWAPH (instruction for exchange of high-order and low-order bytes of 2-byte data)

[Instruction format (macro name)]

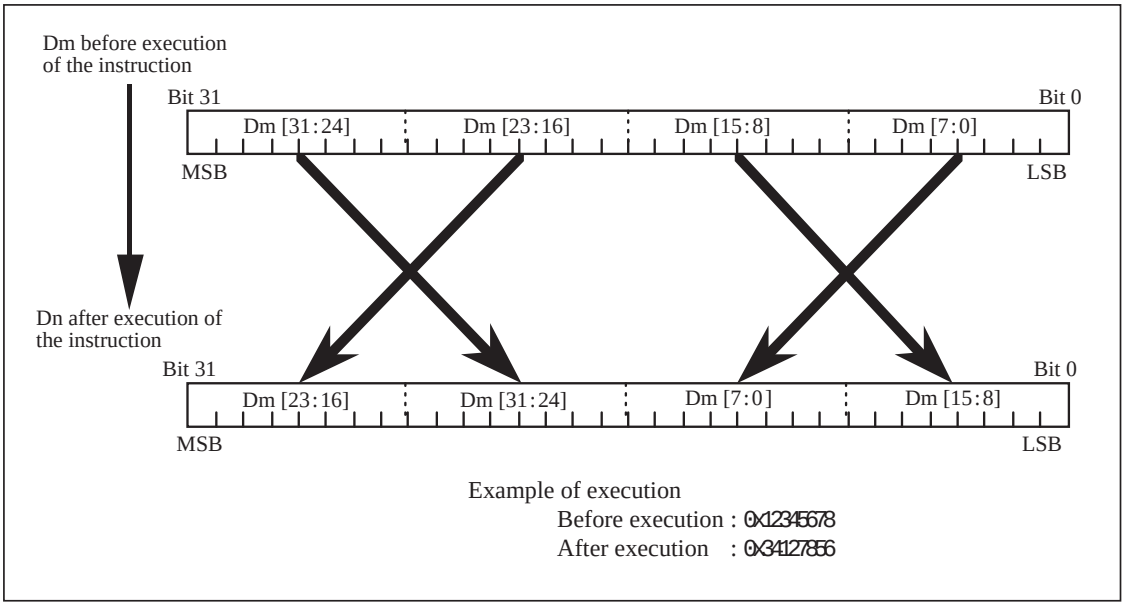
SWAPH Dm, Dn

[Assembler mnemonic]

udf09 Dm, Dn

[Operation]

This instruction exchanges bit 15 to bit 8 and bit 7 to bit 0 of Dm and also exchanges bit 32 to bit 24 and bit 23 to bit 16 and then stores the resultant data in Dn.



Flag	Change	Condition
V	*	Undefined
C	*	Undefined
N	*	Undefined
Z	*	Undefined

[Note for programming]

Updating of the PSW as a result of flag changes is delayed by 1 instruction.
Note, however, that flags can be evaluated for the Bcc and Lcc instructions before flag changes are reflected in the PSW.

■ Precautions for extension arithmetic programming

The extension arithmetic units come equipped with the following registers designed specifically to store high-speed multiply and multiply and accumulate results.

1. Precautions for describing instructions
   This section provides precautions for programming associated with describing, arranging and combining instructions. Failure to observe these precautions may result in malfunction. The following lists such precautions:

Table:16.4.1 List of Precautions

Preceding instruction	Succeeding instruction	Arrangement	Precaution
Word/halfword data multiply and accumulate instructions *1	High-speed multiply instructions *3	Succeeding	Insert 1 or more cycles between instructions.
Word/halfword data multiply and accumulate instructions *1	Multiply and accumulate instructions *4	Succeeding	Insert 2 or more cycles between instructions.
Word/halfword data multiply and accumulate instructions *1	MCRH and MCRL access instructions *5	Succeeding	Insert 3 or more cycles between instructions.
Byte data multiply and accumulate instructions *2	Multiply and accumulate instructions *4	Succeeding	Insert 1 or more cycles between instructions.
Byte data multiply and accumulate instructions *2	MCRH and MCRL access instructions *5	Succeeding	Insert 2 or more cycles between instructions.

*1 The following instructions fall under the category of word/halfword data multiply and accumulate instructions:
MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU and MACIHU instructions

*2 The following instructions fall under the category of byte data multiply and accumulate instructions:
MACB, MACIB, MACBU and MACIBU instructions

*3 The following instructions fall under the category of high-speed multiply instructions:
MULQ, MULQI, MULQU and MULQIU instructions

*4 The following instructions fall under the category of multiply and accumulate instructions:
MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU, MACIHU, MACB, MACIB, MACBU and MACIBU instructions

*5 The following instructions fall under the category of MCRH and MCRL access instructions:
PUTCX, CLRMAC, GETCHX and GETCLX instructions

1) Precautions for describing word/halfword data multiply and accumulate instruction and high-speed multiply instruction

Word/halfword data multiply and accumulate instruction and high-speed multiply instruction are executed by a common arithmetic unit. For this reason, the next high-speed multiply instruction must be activated after the previous word/halfword data multiply and accumulate instruction has completed its operation using a common arithmetic unit. Therefore, it is necessary to provide 1 cycle between the preceding word/halfword data multiply and accumulate instruction and the succeeding high-speed multiply instruction.

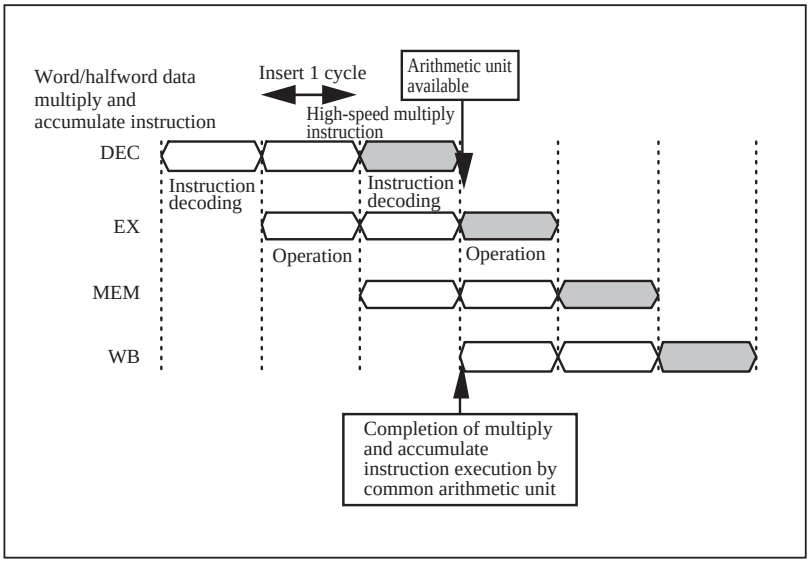


Figure:16.4.3 Drawing of Pipelining for Precaution (1)

This precaution is applicable to the following instructions:

<Word/halfword data multiply and accumulate instructions>

MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU and MACIHU instructions
<High-speed multiply instructions>

MULQ, MULQI, MULQU and MULQIU instructions

2) Precautions for describing word/halfword data multiply and accumulate instruction and multiply and accumulate instruction

When a word/halfword data multiply and accumulate instruction and multiply and accumulate instruction are executed continuously with the former instruction preceding the latter, the result of the word/halfword data multiply and accumulate instruction is used to execute the sequential multiply and accumulate instruction. For this reason, the next multiply and accumulate instruction must be activated after the result of the word/halfword data multiply and accumulate instruction, that is required for the multiply and accumulate instruction, has been output. Therefore, it is necessary to provide 2 cycles between the preceding word/halfword data multiply and accumulate instruction and the succeeding multiply and accumulate instruction.

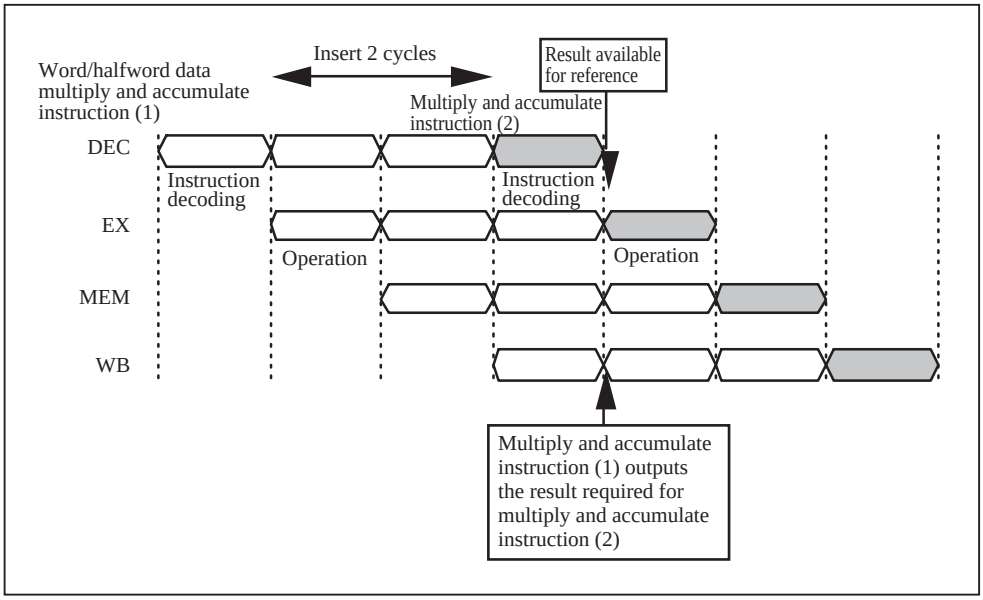


Figure:16.4.4 Drawing of Pipelining for Precaution (2)

This precaution is applicable to the following instructions:
<Word/halfword data multiply and accumulate instructions>

MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU and MACIHU instructions
<Multiply and accumulate instructions>

MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU, MACIHU, MACB, MACIB, MACBU and MACIBU instructions

3) Precautions for describing word/halfword data multiply and accumulate instruction and MCRH and MCRL access instruction

When a word/halfword data multiply and accumulate instruction and MCRH and MCRL access instruction are executed, the result of the word/halfword data multiply and accumulate instruction is used to execute the MCRH and MCRL access instruction. For this reason, the next MCRH and MCRL access instruction must be activated after the result of the word/halfword data multiply and accumulate instruction, that is required for the MCRH and MCRL access instruction, has been output. Therefore, it is necessary to provide 3 cycles between the preceding word/halfword data multiply and accumulate instruction and the succeeding MCRH and MCRL access instruction.

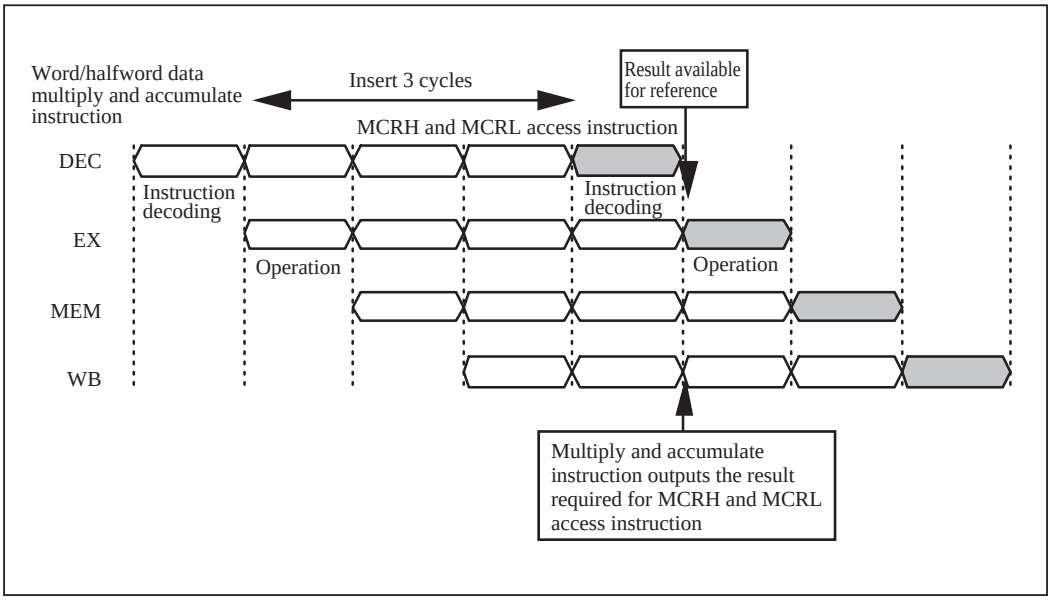


Figure:16.4.5 Drawing of Pipelining for Precaution (3)

This precaution is applicable to the following instructions:

<Word/halfword data multiply and accumulate instructions>

MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU and MACIHU instructions

<MCRH and MCRL access instructions>

PUTCX, CLRMAC, GETCHX and GETCLX instructions

4) Precautions for describing byte data multiply and accumulate instruction and multiply and accumulate instruction

When a byte data multiply and accumulate instruction and multiply and accumulate instruction are executed continuously, the result of the byte data multiply and accumulate instruction is used to execute the multiply and accumulate instruction. For this reason, the next multiply and accumulate instruction must be activated after the result of the byte data multiply and accumulate instruction, that is required for the multiply and accumulate instruction, has been output. Therefore, it is necessary to provide 1 cycle between the preceding byte data multiply and accumulate instruction and the succeeding multiply and accumulate instruction.

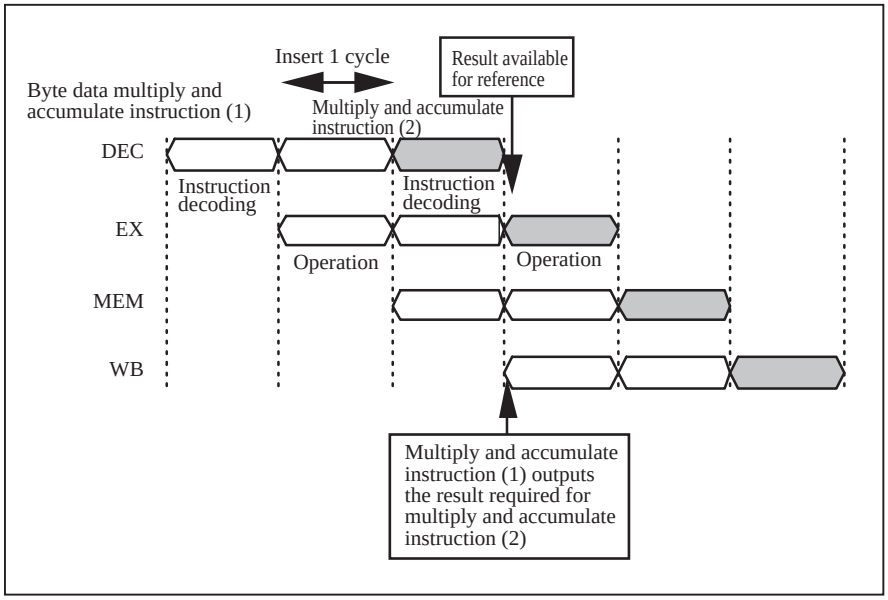


Figure:16.4.6 Drawing of Pipelining for Precaution (4)

This precaution is applicable to the following instructions:

<Byte data multiply and accumulate instructions>

MACB, MACIB, MACBU and MACIBU instructions

<Multiply and accumulate instructions>

MAC, MACI, MACH, MACIH, MACU, MACIU, MACHU, MACIHU, MACB, MACIB, MACBU and MACIBU instructions

5) Precautions for describing byte data multiply and accumulate instruction and MCRH and MCRL access instruction

When a byte data multiply and accumulate instruction and MCRH and MCRL access instruction are executed, the result of the byte data multiply and accumulate instruction is used to execute the MCRH and MCRL access instruction. For this reason, the next MCRH and MCRL access instruction must be activated after the result of the byte data multiply and accumulate instruction, that is required for the MCRH and MCRL access instruction, has been output. Therefore, it is necessary to provide 2 cycles between the preceding byte data multiply and accumulate instruction and the succeeding MCRH and MCRL access instruction.

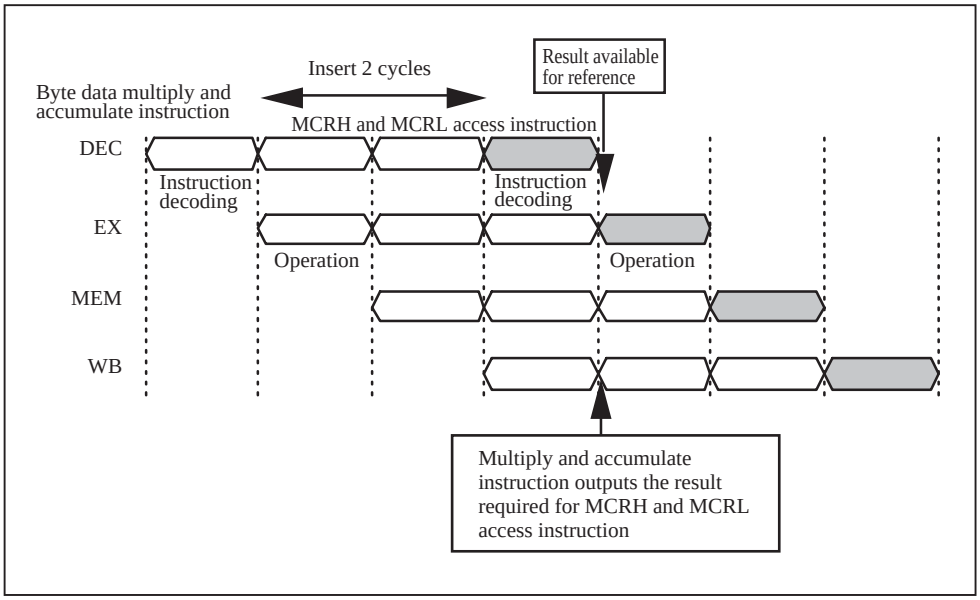


Figure:16.4.7 Drawing of Pipelining for Precaution (5)

This precaution is applicable to the following instructions:

<Byte data multiply and accumulate instructions>

MACB, MACIB, MACBU and MACIBU instructions

<MCRH and MCRL access instructions>

PUTCX, CLRMAC, GETCHX and GETCLX instructions

List of Extension Instructions (Code Length, Cycle Count)

Instruction		Source	Destination	Format	Code length	Cycle count	Remarks
PUTX	PUTX	Dm		D0	2	1	
	PUTCX			D0	2	1	
GETX	GETX		Dn	D0	2	1	
	GETCHX			D0	2	1	
	GETCLX			D0	2	1	
CLRMAC	CLRMAC			D0	2	1	
MULQ	MULQ	Dm	Dn	D0	2	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQI	imm8	Dn	D1	3	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQI	imm16	Dn	D2	4	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQI	imm32	Dn	D4	6	5	Dn can be represented by 2 to 1 byte or Dn = 0
						6	Dn can be represented by 3 to 4 bytes
MULQU	MULQU	Dm	Dn	D0	2	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQIU	imm8	Dn	D1	3	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQIU	imm16	Dn	D2	4	4	Dn can be represented by 2 to 1 byte or Dn = 0
						5	Dn can be represented by 3 to 4 bytes
	MULQIU	imm32	Dn	D4	6	5	Dn can be represented by 2 to 1 byte or Dn = 0
						6	Dn can be represented by 3 to 4 bytes
MAC	MAC	Dm	Dn	D0	2	1	
	MACI	imm8	Dn	D1	3	1	
	MACI	imm16	Dn	D2	4	1	
	MACI	imm32	Dn	D4	6	2	
	MACH	Dm	Dn	D0	2	1	
	MACIH	imm8	Dn	D1	3	1	
	MACIH	imm16	Dn	D2	4	1	
	MACB	Dm	Dn	D0	2	1	
	MACIB	imm8	Dn	D1	3	1	
MACU	MACU	Dm	Dn	D0	2	1	
	MACIU	imm8	Dn	D1	3	1	
	MACIU	imm16	Dn	D2	4	1	
	MACIU	imm32	Dn	D4	6	2	
	MACHU	Dm	Dn	D0	2	1	
	MACIHU	imm8	Dn	D1	3	1	
	MACIHU	imm16	Dn	D2	4	1	
	MACBU	Dm	Dn	D0	2	1	
	MACIBU	imm8	Dn	D1	3	1	
SAT16	SAT16	Dm	Dn	D0	2	2	
SAT24	SAT24	Dm	Dn	D0	2	2	
MCST	MCST	Dm	Dn	D0	2	2	
	MCST9		Dn	D0	2	2	
	MCST48		Dn	D0	2	2	
BSCH	BSCH	Dm	Dn	D0	2	2	
SWAP	SWAP	Dm	Dn	D0	2	1	
	SWAPH	Dm	Dn	D0	2	1	

16.5 Special Function Registers List

Address	Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x00008000	IVAR0	IVAR0 15	IVAR0 14	IVAR0 13	IVAR0 12	IVAR0 11	IVAR0 10	IVAR0 9	IVAR0 8	IVAR0 7	IVAR0 6	IVAR0 5	IVAR0 4	IVAR0 3	IVAR0 2	IVAR0 1	IVAR0 0	V-10
0x00008004	IVAR1	IVAR1 15	IVAR1 14	IVAR1 13	IVAR1 12	IVAR1 11	IVAR1 10	IVAR1 9	IVAR1 8	IVAR1 7	IVAR1 6	IVAR1 5	IVAR1 4	IVAR1 3	IVAR1 2	IVAR1 1	IVAR1 0	V-10
0x00008008	IVAR2	IVAR2 15	IVAR2 14	IVAR2 13	IVAR2 12	IVAR2 11	IVAR2 10	IVAR2 9	IVAR2 8	IVAR2 7	IVAR2 6	IVAR2 5	IVAR2 4	IVAR2 3	IVAR2 2	IVAR2 1	IVAR2 0	V-11
0x0000800C	IVAR3	IVAR3 15	IVAR3 14	IVAR3 13	IVAR3 12	IVAR3 11	IVAR3 10	IVAR3 9	IVAR3 8	IVAR3 7	IVAR3 6	IVAR3 5	IVAR3 4	IVAR3 3	IVAR3 2	IVAR3 1	IVAR3 0	V-11
0x00008010	IVAR4	IVAR4 15	IVAR4 14	IVAR4 13	IVAR4 12	IVAR4 11	IVAR4 10	IVAR4 9	IVAR4 8	IVAR4 7	IVAR4 6	IVAR4 5	IVAR4 4	IVAR4 3	IVAR4 2	IVAR4 1	IVAR4 0	V-11
0x00008014	IVAR5	IVAR5 15	IVAR5 14	IVAR5 13	IVAR5 12	IVAR5 11	IVAR5 10	IVAR5 9	IVAR5 8	IVAR5 7	IVAR5 6	IVAR5 5	IVAR5 4	IVAR5 3	IVAR5 2	IVAR5 1	IVAR5 0	V-11
0x00008018	IVAR6	IVAR6 15	IVAR6 14	IVAR6 13	IVAR6 12	IVAR6 11	IVAR6 10	IVAR6 9	IVAR6 8	IVAR6 7	IVAR6 6	IVAR6 5	IVAR6 4	IVAR6 3	IVAR6 2	IVAR6 1	IVAR6 0	V-11
0x00008040	CPUM	Access prohibited																II-8
0x00008078	ROMCTR	-	-	-	-	Reserved	Reserved	ROMWC1	ROMWC0	-	-	-	Reserved	Reserved	Reserved	-	-	IV-5
0x00008200	WDBC									WDBC7	WDBC6	WDBC5	WDBC4	WDBC3	WDBC2	WDBC1	WDBC0	XI-4
0x00008202	WDCTR									WDCNE	WDRST	-	-	-	WDCK2	WDCK1	WDCK0	XI-5
0x00008204	RSTCTR									-	-	-	-	-	-	-	CHIPRST	XI-6
0x00008280	CKCTR	-	-	-	-	-	-	-	-	Reserved	Reserved	IOCK1	IOCK0	Reserved	Reserved	MCK1	MCK0	III-5
0x00008900	G0ICR (NMICR)	-	-	-	-	-	-	-	-	-	-	-	-	-	SYSEF	WDIF	-	V-12
0x00008908	G2ICR	-	G2LV2	G2LV1	G2LV0	-	-	-	G2IE0	-	-	-	G2IR0	-	-	-	G2ID0	V-15
0x0000890C	G3ICR	-	G3LV2	G3LV1	G3LV0	-	-	G3IE1	G3IE0	-	-	G3IR1	G3IR0	-	-	G3ID1	G3ID0	V-15
0x00008910	G4ICR	-	G4LV2	G4LV1	G4LV0	-	-	G4IE1	G4IE0	-	-	G4IR1	G4IR0	-	-	G4ID1	G4ID0	V-16
0x00008914	G5ICR	-	G5LV2	G5LV1	G5LV0	-	-	G5IE1	G5IE0	-	-	G5IR1	G5IR0	-	-	G5ID1	G5ID0	V-16
0x00008918	G6ICR	-	G6LV2	G6LV1	G6LV0	-	-	G6IE1	G6IE0	-	-	G6IR1	G6IR0	-	-	G6ID1	G6ID0	V-17
0x0000891C	G7ICR	-	G7LV2	G7LV1	G7LV0	-	G7IE2	G7IE1	G7IE0	-	G7IR2	G7IR1	G7IR0	-	G7ID2	G7ID1	G7ID0	V-17
0x00008920	G8ICR	-	G8LV2	G8LV1	G8LV0	-	G8IE2	G8IE1	G8IE0	-	G8IR2	G8IR1	G8IR0	-	G8ID2	G8ID1	G8ID0	V-18
0x00008924	G9ICR	-	G9LV2	G9LV1	G9LV0	-	G9IE2	G9IE1	G9IE0	-	G9IR2	G9IR1	G9IR0	-	G9ID2	G9ID1	G9ID0	V-19
0x00008928	G10ICR	-	G10 LV2	G10 LV1	G10 LV0	-	G10 IE2	G10 IE1	G10 IE0	-	G10 IR2	G10 IR1	G10 IR0	-	G10 ID2	G10 ID1	G10 ID0	V-20
0x0000892C	G11ICR	-	G11 LV2	G11 LV1	G11 LV0	-	G11 IE2	G11 IE1	G11 IE0	-	G11 IR2	G11 IR1	G11 IR0	-	G11 ID2	G11 ID1	G11 ID0	V-21
0x00008930	G12ICR	-	G12 LV2	G12 LV1	G12 LV0	-	G12 IE2	G12 IE1	G12 IE0	-	G12 IR2	G12 IR1	G12 IR0	-	G12 ID2	G12 ID1	G12 ID0	V-22
0x00008934	G13ICR	-	G13 LV2	G13 LV1	G13 LV0	-	-	G13 IE1	G13 IE0	-	-	G13 IR1	G13 IR0	-	-	G13 ID1	G13 ID0	V-23
0x00008938	G14ICR	-	G14 LV2	G14 LV1	G14 LV0	-	-	G14 IE1	G14 IE0	-	-	G14 IR1	G14 IR0	-	-	G14 ID1	G14 ID0	V-23
0x0000893C	G15ICR	-	G15 LV2	G15 LV1	G15 LV0	-	-	G15 IE1	G15 IE0	-	-	G15 IR1	G15 IR0	-	-	G15 ID1	G15 ID0	V-24
0x00008940	G16ICR	-	G16 LV2	G16 LV1	G16 LV0	-	-	G16 IE1	G16 IE0	-	-	G16 IR1	G16 IR0	-	-	G16 ID1	G16 ID0	V-24
0x00008944	G17ICR	-	G17 LV2	G17 LV1	G17 LV0	-	-	G17 IE1	G17 IE0	-	-	G17 IR1	G17 IR0	-	-	G17 ID1	G17 ID0	V-25
0x00008948	G18ICR	-	G18 LV2	G18 LV1	G18 LV0	-	-	-	G18 IE0	-	-	-	G18 IR0	-	-	-	G18 ID0	V-25
0x0000894C	G19ICR	-	G19 LV2	G19 LV1	G19 LV0	-	-	-	G19 IE0	-	-	-	G19 IR0	-	-	-	G19 ID0	V-26
0x00008950	G20ICR	-	G20 LV2	G20 LV1	G20 LV0	-	-	-	G20 IE0	-	-	-	G20 IR0	-	-	-	G20 ID0	V-26
0x00008954	G21ICR	-	G21 LV2	G21 LV1	G21 LV0	-	-	-	G21 IE0	-	-	-	G21 IR0	-	-	-	G21 ID0	V-27
0x00008958	G22ICR	-	G22 LV2	G22 LV1	G22 LV0	-	-	-	G22 IE0	-	-	-	G22 IR0	-	-	-	G22 ID0	V-27
0x0000895C	G23ICR	-	G23 LV2	G23 LV1	G23 LV0	-	-	-	G23 IE0	-	-	-	G23 IR0	-	-	-	G23 ID0	V-28
0x00008960	G24ICR	-	G24 LV2	G24 LV1	G24 LV0	-	-	-	G24 IE0	-	-	-	G24 IR0	-	-	-	G24 ID0	V-28

Address	Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x00008964	G25ICR	-	G25 LV2	G25 LV1	G25 LV0	-	-	-	G25 IE0	-	-	-	G25 IR0	-	-	-	G25 ID0	V-29
0x00008968	G26ICR	-	G26 LV2	G26 LV1	G26 LV0	-	-	G26 IE1	G26 IE0	-	-	G26 IR1	G26 IR0	-	-	G26 ID1	G26 ID0	V-29
0x0000896C	G27ICR	-	G27 LV2	G27 LV1	G27 LV0	-	-	G27 IE1	G27 IE0	-	-	G27 IR1	G27 IR0	-	-	G27 ID1	G27 ID0	V-30
0x00008970	G28ICR	-	G28 LV2	G28 LV1	G28 LV0	-	-	-	G28 IE0	-	-	-	G28 IR0	-	-	-	G28 ID0	V-30
0x00008974	G29ICR	-	G29 LV2	G29 LV1	G29 LV0	-	-	G29 IE1	G29 IE0	-	-	G29 IR1	G29 IR0	-	-	G29 ID1	G29 ID0	V-31
0x00008978	G30ICR	-	G30 LV2	G30 LV1	G30 LV0	-	-	G30 IE1	G30 IE0	-	-	G30 IR1	G30 IR0	-	-	G30 ID1	G30 ID0	V-31
0x00008A00	IAGR	-	-	-	-	-	-	-	-	-	GN4	GN3	GN2	GN1	GN0	-	-	V-32
0x00008A80	EXTMD0	IR7 TG1	IR7 TG0	IR6 TG1	IR6 TG0	IR5 TG1	IR5 TG0	IR4 TG1	IR4 TG0	IR3 TG1	IR3 TG0	IR2 TG1	IR2 TG0	IR1 TG1	IR1 TG0	IR0 TG1	IR0 TG0	V-33
0x00008A84	EXTMD1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	IR8 TG1	IR8 TG0	V-34
0x0000A001	P1OUT									P17O	P16O	Reserved	P14O	P13O	P12O	P11O	P10O	VII-10
0x0000A002	P2OUT									P27O	P26O	P25O	P24O	P23O	P22O	P21O	P20O	VII-13
0x0000A003	P3OUT									P37O	P36O	P35O	P34O	P33O	P32O	P31O	Reserved	VII-15
0x0000A004	P4OUT									P47O	P46O	Reserved	Reserved	P43O	P42O	Reserved	Reserved	VII-17
0x0000A005	P5OUT									P57O	P56O	P55O	P54O	P53O	P52O	P51O	Reserved	VII-20
0x0000A006	P6OUT									P67O	P66O	P65O	P64O	P63O	P62O	Reserved	Reserved	VII-22
0x0000A007	P7OUT									Reserved	Reserved	Reserved	Reserved	P73O	P72O	-	-	VII-24
0x0000A008	P8OUT									Reserved	Reserved	Reserved	Reserved	P83O	P82O	P81O	P80O	VII-26
0x0000A009	P9OUT									P97O	P96O	P95O	P94O	P93O	P92O	P91O	P90O	VII-28
0x0000A00A	PAOUT									PA7O	PA6O	PA5O	PA4O	PA3O	PA2O	PA1O	PA0O	VII-30
0x0000A00B	Reserved																	-
0x0000A011	P1IN									P17I	P16I	Reserved	P14I	P13I	P12I	P11I	P10I	VII-10
0x0000A012	P2IN									P27I	P26I	P25I	P24I	P23I	P22I	P21I	P20I	VII-13
0x0000A013	P3IN									P37I	P36I	P35I	P34I	P33I	P32I	P31I	Reserved	VII-15
0x0000A014	P4IN									P47I	P46I	Reserved	Reserved	P43I	P42I	Reserved	Reserved	VII-17
0x0000A015	P5IN									P57I	P56I	P55I	P54I	P53I	P52I	P51I	Reserved	VII-20
0x0000A016	P6IN									P67I	P66I	P65I	P64I	P63I	P62I	Reserved	Reserved	VII-22
0x0000A017	P7IN									Reserved	Reserved	Reserved	Reserved	P73I	P72I	-	-	VII-24
0x0000A018	P8IN									Reserved	Reserved	Reserved	Reserved	P83I	P82I	P81I	P80I	VII-26
0x0000A019	P9IN									P97I	P96I	P95I	P94I	P93I	P92I	P91I	P90I	VII-28
0x0000A01A	PAIN									PA7I	PA6I	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I	VII-30
0x0000A01B	Reserved																	-
0x0000A021	P1DIR									P17D	P16D	Reserved	P14D	P13D	P12D	P11D	P10D	VII-11
0x0000A022	P2DIR									P27D	P26D	P25D	P24D	P23D	P22D	P21D	P20D	VII-13
0x0000A023	P3DIR									P37D	P36D	P35D	P34D	P33D	P32D	P31D	Reserved	VII-15
0x0000A024	P4DIR									P47D	P46D	Reserved	Reserved	P43D	P42D	Reserved	Reserved	VII-18
0x0000A025	P5DIR									P57D	P56D	P55D	P54D	P53D	P52D	P51D	Reserved	VII-20
0x0000A026	P6DIR									P67D	P66D	P65D	P64D	P63D	P62D	Reserved	Reserved	VII-22
0x0000A027	P7DIR									Reserved	Reserved	Reserved	Reserved	P73D	P72D	-	-	VII-24
0x0000A028	P8DIR									Reserved	Reserved	Reserved	Reserved	P83D	P82D	P81D	P80D	VII-26
0x0000A029	P9DIR									P97D	P96D	P95D	P94D	P93D	P92D	P91D	P90D	VII-28
0x0000A02A	PADIR									PA7D	PA6D	PA5D	PA4D	PA3D	PA2D	PA1D	PA0D	VII-30
0x0000A02B	Reserved																	-
0x0000A031	P1MD									P17M	P16M	Reserved	-	-	-	-	-	VII-11
0x0000A032	P2MD									-	P26M	P25M	-	P23M	P22M	-	P20M	VII-14
0x0000A033	P3MD									P37M	P36M	P35M	P34M	P33M	P32M	P31M	Reserved	VII-16
0x0000A034	P4MD									P47M	P46M	Reserved	Reserved	P43M	P42M	Reserved	Reserved	VII-18
0x0000A035	P5MD									P57M	P56M	P55M	P54M	P53M	P52M	P51M	Reserved	VII-21
0x0000A036	P6MD									P67M	P66M	P65M	P64M	P63M	P62M	-	-	VII-23
0x0000A037	P7MD									Reserved	Reserved	Reserved	Reserved	P73M	P72M	-	-	VII-25
0x0000A038	Reserved																	-
0x0000A039	P9MD									P97M	P96M	P95M	P94M	P93M	P92M	P91M	P90M	VII-29
0x0000A03A	PAMD									PA7M	PA6M	PA5M	PA4M	PA3M	PA2M	PA1M	PA0M	VII-31
0x0000A03B	Reserved																	-
0x0000A041	P1PLU									P17R	P16R	Reserved	P14R	P13R	P12R	P11R	P10R	VII-12
0x0000A042	P2PLU									P27R	P26R	P25R	P24R	P23R	P22R	P21R	P20R	VII-14
0x0000A043	P3PLU									P37R	P36R	P35R	P34R	P33R	P32R	P31R	Reserved	VII-16
0x0000A044	P4PLU									P47R	P46R	Reserved	Reserved	P43R	P42R	Reserved	Reserved	VII-19
0x0000A045	P5PLU									P57R	P56R	P55R	P54R	P53R	P52R	P51R	Reserved	VII-21
0x0000A046	P6PLU									P67R	P66R	P65R	P64R	P63R	P62R	Reserved	Reserved	VII-23

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0x0000A047	P7PLU									Reserved	Reserved	Reserved	Reserved	P73R	P72R	-	-	VII-25
0x0000A048	P8PLU									Reserved	Reserved	Reserved	Reserved	P83R	P82R	P81R	P80R	VII-27
0x0000A049	P9PLU									P97R	P96R	P95R	P94R	P93R	P92R	P91R	P90R	VII-29
0x0000A04A	PAPLU									PA7R	PA6R	PA5R	PA4R	PA3R	PA2R	PA1R	PA0R	VII-31
0x0000A04B	Reserved																	-
0x0000A050	NFCLK0	NFCK 71	NFCK 70	NFCK 61	NFCK 60	NFCK 51	NFCK 50	NFCK 41	NFCK 40	NFCK 31	NFCK 30	NFCK 21	NFCK 20	NFCK 11	NFCK 10	NFCK 01	NFCK 00	V-42
0x0000A052	NFCLK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	NFCK 81	NFCK 80	V-43
0x0000A054	NFCNT	-	-	-	-	-	-	-	NF CNT8	NF CNT7	NF CNT6	NF CNT5	NF CNT4	NF CNT3	NF CNT2	NF CNT1	NF CNT0	V-44
0x0000A056	IRQEDGE SEL	-	-	-	-	-	-	-	IRQ EG8	IRQ EG7	IRQ EG6	IRQ EG5	IRQ EG4	IRQ EG3	IRQ EG2	IRQ EG1	IRQ EG0	V-45
0x0000A100	SC0CTR	SCA0 TEN	SCA0 REN	SCA0 BRE	Reserved	SCA0 PTL	Reserved	SCA0 OD	Reserved	SCA0 LN	SCA0 PTY2	SCA0 PTY1	SCA0 PTY0	SCA0 SB	-	SCA0 S1	SCA0 S0	XII-6
0x0000A104	SC0RB									SCA0 RB7	SCA0 RB6	SCA0 RB5	SCA0 RB4	SCA0 RB3	SCA0 RB2	SCA0 RB1	SCA0 RB0	XII-5
0x0000A109	SC0STR									SCA0 TBSY	SCA0 RBSY	-	SCA0 RXA	-	SCA0 FE	SCA0 PE	SCA0 OE	XII-8
0x0000A10C	SC0TB									SCA0 TB7	SCA0 TB6	SCA0 TB5	SCA0 TB4	SCA0 TB3	SCA0 TB2	SCA0 TB1	SCA0 TB0	XII-5
0x0000A10E	SIFCLK									-	-	SC2 CKS1	SC2 CKS0	SC1 CKS1	SC1 CKS0	SC0 CKS1	SC0 CKS0	XII-10
0x0000A110	SC1CTR	SCA1 TEN	SCA1 REN	SCA1 BRE	Reserved	SCA1 PTL	Reserved	SCA1 OD	Reserved	SCA1 LN	SCA1 PTY2	SCA1 PTY1	SCA1 PTY0	SCA1 SB	-	SCA1 S1	SCA1 S0	XII-7
0x0000A114	SC1RB									SCA1 RB7	SCA1 RB6	SCA1 RB5	SCA1 RB4	SCA1 RB3	SCA1 RB2	SCA1 RB1	SCA1 RB0	XII-5
0x0000A119	SC1STR									SCA1 TBSY	SCA1 RBSY	-	SCA1 RXA	-	SCA1 FE	SCA1 PE	SCA1 OE	XII-9
0x0000A11C	SC1TB									SCA1 TB7	SCA1 TB6	SCA1 TB5	SCA1 TB4	SCA1 TB3	SCA1 TB2	SCA1 TB1	SCA1 TB0	XII-5
0x0000A120	SC2CTR0									SC2 CE1	-	-	SC2 DIR	SC2 STE	SC2 LNG2	SC2 LNG1	SC2 LNG0	XIII-6
0x0000A121	SC2CTR1									SC2 IOM	SC2 SBTS	SC2 SBIS	SC2 SBOS	SC2 CKM	SC2 MST	-	SC2 CMD	XIII-7
0x0000A124	SC2CTR2									SC2 FM1	SC2 FM0	SC2 PM1	SC2 PM0	SC2 NPE	-	SC2 BRKF	SC2 BRKE	XIII-8
0x0000A125	SC2CTR3									SC2 FDC1	SC2 FDC0	-	-	SC2 PSCE	SC2 PSC2	SC2 PSC1	SC2 PSC0	XIII-9
0x0000A128	SC2STR									SC2 TBSY	SC2 RBSY	SC2 TEMP	SC2 REMP	SC2 FEF	SC2 PEK	SC2 ORE	SC2 ERE	XIII-10
0x0000A12C	SC2RB									SC2 RB7	SC2 RB6	SC2 RB5	SC2 RB4	SC2 RB3	SC2 RB2	SC2 RB1	SC2 RB0	XIII-5
0x0000A130	SC2TB									SC2 TB7	SC2 TB6	SC2 TB5	SC2 TB4	SC2 TB3	SC2 TB2	SC2 TB1	SC2 TB0	XIII-5
0x0000A180	TM0MD									TM0 CNE	TM0 LDE	-	-	-	TM0 CK2	TM0 CK1	TM0 CK0	VIII-18
0x0000A181	TM1MD									TM1 CNE	TM1 LDE	-	-	-	TM1 CK2	TM1 CK1	TM1 CK0	VIII-19
0x0000A184	TM2MD									TM2 CNE	TM2 LDE	-	-	-	TM2 CK2	TM2 CK1	TM2 CK0	VIII-20
0x0000A185	TM3MD									TM3 CNE	TM3 LDE	-	-	-	TM3 CK2	TM3 CK1	TM3 CK0	VIII-21
0x0000A188	TM0BR									TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0	VIII-13
0x0000A189	TM1BR									TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0	VIII-13
0x0000A18C	TM2BR									TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0	VIII-13
0x0000A18D	TM3BR									TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0	VIII-13
0x0000A190	TM0BC									TM0 BC7	TM0 BC6	TM0 BC5	TM0 BC4	TM0 BC3	TM0 BC2	TM0 BC1	TM0 BC0	VIII-15
0x0000A191	TM1BC									TM1 BC7	TM1 BC6	TM1 BC5	TM1 BC4	TM1 BC3	TM1 BC2	TM1 BC1	TM1 BC0	VIII-15
0x0000A194	TM2BC									TM2 BC7	TM2 BC6	TM2 BC5	TM2 BC4	TM2 BC3	TM2 BC2	TM2 BC1	TM2 BC0	VIII-16
0x0000A195	TM3BC									TM3 BC7	TM3 BC6	TM3 BC5	TM3 BC4	TM3 BC3	TM3 BC2	TM3 BC1	TM3 BC0	VIII-16
0x0000A198	TM03PSC									TM PSCNE 1	-	-	-	-	-	-	-	VIII-11
0x0000A19C	TMEXPS C8									-	TM16IN	TM14IN	TM6IN	TM4IN	TM2IN	TM0IN	EX PSCNE	VIII-12
0x0000A1A0	TM4MD									TM4 CNE	TM4 LDE	-	-	-	TM4 CK2	TM4 CK1	TM4 CK0	VIII-22

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0x0000A1A1	TM5MD									TM5 CNE	TM5 LDE	-	-	-	TM5 CK2	TM5 CK1	TM5 CK0	VIII-23
0x0000A1A4	TM6MD									TM6 CNE	TM6 LDE	-	-	-	TM6 CK2	TM6 CK1	TM6 CK0	VIII-24
0x0000A1A5	TM7MD									TM7 CNE	TM7 LDE	-	-	-	TM7 CK2	TM7 CK1	TM7 CK0	VIII-25
0x0000A1A8	TM4BR									TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0	VIII-14
0x0000A1A9	TM5BR									TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0	VIII-14
0x0000A1AC	TM6BR									TM6 BR7	TM6 BR6	TM6 BR5	TM6 BR4	TM6 BR3	TM6 BR2	TM6 BR1	TM6 BR0	VIII-14
0x0000A1AD	TM7BR									TM7 BR7	TM7 BR6	TM7 BR5	TM7 BR4	TM7 BR3	TM7 BR2	TM7 BR1	TM7 BR0	VIII-14
0x0000A1B0	TM4BC									TM4 BC7	TM4 BC6	TM4 BC5	TM4 BC4	TM4 BC3	TM4 BC2	TM4 BC1	TM4 BC0	VIII-16
0x0000A1B1	TM5BC									TM5 BC7	TM5 BC6	TM5 BC5	TM5 BC4	TM5 BC3	TM5 BC2	TM5 BC1	TM5 BC0	VIII-16
0x0000A1B4	TM6BC									TM6 BC7	TM6 BC6	TM6 BC5	TM6 BC4	TM6 BC3	TM6 BC2	TM6 BC1	TM6 BC0	VIII-16
0x0000A1B5	TM7BC									TM7 BC7	TM7 BC6	TM7 BC5	TM7 BC4	TM7 BC3	TM7 BC2	TM7 BC1	TM7 BC0	VIII-17
0x0000A1B8	TM47PSC									TM PSCNE 2	-	-	-	-	-	-	-	VIII-11
0x0000A1C0	TM14MD									TM14 CNE	TM14 LDE	-	-	-	TM14 CK2	TM14 CK1	TM14 CK0	VIII-26
0x0000A1C1	TM15MD									TM15 CNE	TM15 LDE	-	-	-	TM15 CK2	TM15 CK1	TM15 CK0	VIII-27
0x0000A1C4	TM16MD									TM16 CNE	TM16 LDE	-	-	-	TM16 CK2	TM16 CK1	TM16 CK0	VIII-28
0x0000A1C5	TM17MD									TM17 CNE	TM17 LDE	-	-	-	TM17 CK2	TM17 CK1	TM17 CK0	VIII-29
0x0000A1C8	TM14BR									TM14 BR7	TM14 BR6	TM14 BR5	TM14 BR4	TM14 BR3	TM14 BR2	TM14 BR1	TM14 BR0	VIII-14
0x0000A1C9	TM15BR									TM15 BR7	TM15 BR6	TM15 BR5	TM15 BR4	TM15 BR3	TM15 BR2	TM15 BR1	TM15 BR0	VIII-15
0x0000A1CC	TM16BR									TM16 BR7	TM16 BR6	TM16 BR5	TM16 BR4	TM16 BR3	TM16 BR2	TM16 BR1	TM16 BR0	VIII-15
0x0000A1CD	TM17BR									TM17 BR7	TM17 BR6	TM17 BR5	TM17 BR4	TM17 BR3	TM17 BR2	TM17 BR1	TM17 BR0	VIII-15
0x0000A1D0	TM14BC									TM14 BC7	TM14 BC6	TM14 BC5	TM14 BC4	TM14 BC3	TM14 BC2	TM14 BC1	TM14 BC0	VIII-17
0x0000A1D1	TM15BC									TM15 BC7	TM15 BC6	TM15 BC5	TM15 BC4	TM15 BC3	TM15 BC2	TM15 BC1	TM15 BC0	VIII-17
0x0000A1D4	TM16BC									TM16 BC7	TM16 BC6	TM16 BC5	TM16 BC4	TM16 BC3	TM16 BC2	TM16 BC1	TM16 BC0	VIII-17
0x0000A1D5	TM17BC									TM17 BC7	TM17 BC6	TM17 BC5	TM17 BC4	TM17 BC3	TM17 BC2	TM17 BC1	TM17 BC0	VIII-17
0x0000A1D8	TM1417PSC									TMPSCNE3	-	-	-	-	-	-	-	VIII-11
0x0000A200	TM8MD	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0	IX-20
0x0000A204	TM8MDA									TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM AO1	TM AO0	IX-26
0x0000A205	TM8MDB									TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM BO1	TM BO0	IX-32
0x0000A208	TM8CA	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0	IX-15
0x0000A20C	TM8CB	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0	IX-18
0x0000A210	TM8BC	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0	IX-13
0x0000A214	TM8PSC									TM PSCNE	-	-	-	-	-	-	-	IX-9
0x0000A218	TMEXPSC16									TM PSCNE	-	-	-	-	-	-	-	IX-11
0x0000A220	TM9MD	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0	IX-21
0x0000A224	TM9MDA									TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM AO1	TM AO0	IX-27
0x0000A225	TM9MDB									TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM BO1	TM BO0	IX-33
0x0000A228	TM9CA	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0	IX-17

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0x0000A22C	TM9CB	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0	IX-18
0x0000A230	TM9BC	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0	IX-14
0x0000A234	TM9PSC									TM PSCNE	-	-	-	-	-	-	-	IX-9
0x0000A240	TM10MD	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0	IX-22
0x0000A244	TM10MDA									TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM AO1	TM AO0	IX-28
0x0000A245	TM10MDB									TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM BO1	TM BO0	IX-34
0x0000A248	TM10CA	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0	IX-17
0x0000A24C	TM10CB	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0	IX-18
0x0000A250	TM10BC	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0	IX-14
0x0000A254	TM10PSC									TM PSCNE	-	-	-	-	-	-	-	IX-10
0x0000A260	TM11MD	TM XF	-	TM TGE	TM ONE	TM CLE	TM CGE	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0	IX-23
0x0000A264	TM11MDA									TM AM1	TM AM0	TM AEG	TM ACE	-	-	TM AO1	TM AO0	IX-29
0x0000A265	TM11MDB									TM BM1	TM BM0	TM BEG	TM BCE	-	-	TM BO1	TM BO0	IX-35
0x0000A268	TM11CA	TM CA15	TM CA14	TM CA13	TM CA12	TM CA11	TM CA10	TM CA9	TM CA8	TM CA7	TM CA6	TM CA5	TM CA4	TM CA3	TM CA2	TM CA1	TM CA0	IX-17
0x0000A26C	TM11CB	TM CB15	TM CB14	TM CB13	TM CB12	TM CB11	TM CB10	TM CB9	TM CB8	TM CB7	TM CB6	TM CB5	TM CB4	TM CB3	TM CB2	TM CB1	TM CB0	IX-18
0x0000A270	TM11BC	TM BC15	TM BC14	TM BC13	TM BC12	TM BC11	TM BC10	TM BC9	TM BC8	TM BC7	TM BC6	TM BC5	TM BC4	TM BC3	TM BC2	TM BC1	TM BC0	IX-14
0x0000A274	TM11PSC									TM PSCNE	-	-	-	-	-	-	-	IX-10
0x0000A280	TM12MD	TMXF	-	TMTGE	TMON E	TMCLE	Reserved	TMUD1	TMUD0	TMCNE	TMLDE	-	-	-	TMCK2	TMCK1	TMCK0	IX-24
0x0000A284	TM12MDA									TMAM1	TMAM0	TMAEG	Reserved	-	-	Reserved	Reserved	IX-30
0x0000A285	TM12MDB									TMBM1	TMBM0	Reserved	Reserved	-	-	Reserved	Reserved	IX-36
0x0000A288	TM12CA	TMCA15	TMCA14	TMCA13	TMCA12	TMCA11	TMCA10	TMCA9	TMCA8	TMCA7	TMCA6	TMCA5	TMCA4	TMCA3	TMCA2	TMCA1	TMCA0	IX-17
0x0000A28C	TM12CB	TMCB15	TMCB14	TMCB13	TMCB12	TMCB11	TMCB10	TMCB9	TMCB8	TMCB7	TMCB6	TMCB5	TMCB4	TMCB3	TMCB2	TMCB1	TMCB0	IX-18
0x0000A290	TM12BC	TMBC15	TMBC14	TMBC13	TMBC12	TMBC11	TMBC10	TMBC9	TMBC8	TMBC7	TMBC6	TMBC5	TMBC4	TMBC3	TMBC2	TMBC1	TMBC0	IX-14
0x0000A294	TM12PSC									TM PSCNE	-	-	-	-	-	-	-	IX-10
0x0000A298	TM12CLKSEL									TM 12CLK	-	-	-	-	-	-	-	IX-12
0x0000A2A0	TM13MD	TM XF	-	TM TGE	TM ONE	TM CLE	Reserved	TM UD1	TM UD0	TM CNE	TM LDE	-	-	-	TM CK2	TM CK1	TM CK0	IX-25
0x0000A2A4	TM13MDA									TM AM1	TM AM0	TM AEG	Reserved	-	-	Reserved	Reserved	IX-31
0x0000A2A5	TM13MDB									TM BM1	TM BM0	Reserved	Reserved	-	-	Reserved	Reserved	IX-36
0x0000A2A8	TM13CA	TMCA15	TMCA14	TMCA13	TMCA12	TMCA11	TMCA10	TMCA9	TMCA8	TMCA7	TMCA6	TMCA5	TMCA4	TMCA3	TMCA2	TMCA1	TMCA0	IX-17
0x0000A2AC	TM13CB	TMCB15	TMCB14	TMCB13	TMCB12	TMCB11	TMCB10	TMCB9	TMCB8	TMCB7	TMCB6	TMCB5	TMCB4	TMCB3	TMCB2	TMCB1	TMCB0	IX-18
0x0000A2B0	TM13BC	TMBC15	TMBC14	TMBC13	TMBC12	TMBC11	TMBC10	TMBC9	TMBC8	TMBC7	TMBC6	TMBC5	TMBC4	TMBC3	TMBC2	TMBC1	TMBC0	IX-14
0x0000A2B4	TM13PSC									TM PSCNE	-	-	-	-	-	-	-	IX-11
0x0000A2B8	TM13CLKSEL									TM 13CLK	-	-	-	-	-	-	-	IX-12
0x0000A300	PWMMD0	-	SYN EN0	SFT EN0	CLK SEL0	TMSTA EN0	TMSTB EN0	SD SELA0	SD SELB0	PCRA EN0	PCRB EN0	INTA EN0	INTB EN0	DT EN0	OR MD0	TC EN0	WAVE MD0	X-5
0x0000A304	OUTMD0	-	-	-	-	-	-	-	-	-	-	PXD TNW0	PXD TW0	PXD TNV0	PXD TV0	PXD TNU0	PXD TU0	X-7
0x0000A308	PWMSEL0	-	-	-	-	PSE LN02	PSEL 02	PSEL N01	PSEL 01	PSEL N00	PSEL 00	OTLV N02	OTLV 02	OTLV N01	OTLV 01	OTLV N00	OTLV 00	X-9
0x0000A30C	PWMSET0	PMSET 0F	PMSET 0E	PMSET 0D	PMSET 0C	PMSET 0B	PMSET 0A	PMSET 09	PMSET 08	PMSET 07	PMSET 06	PMSET 05	PMSET 04	PMSET 03	PMSET 02	PMSET 01	PMSET 00	X-11
0x0000A310	TCMP0A	TCPA 0F	TCPA 0E	TCPA 0D	TCPA 0C	TCPA 0B	TCPA 0A	TCPA 09	TCPA 08	TCPA 07	TCPA 06	TCPA 05	TCPA 04	TCPA 03	TCPA 02	TCPA 01	TCPA 00	X-12

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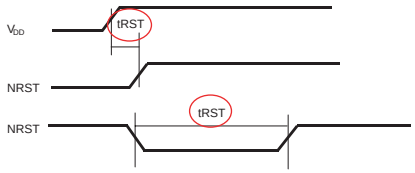
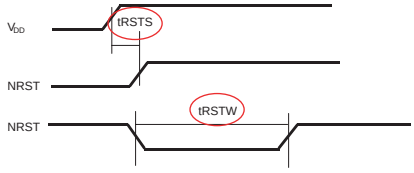
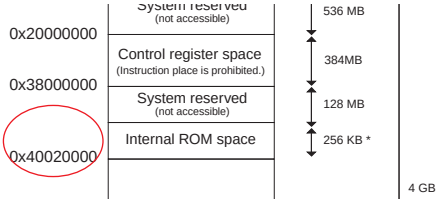
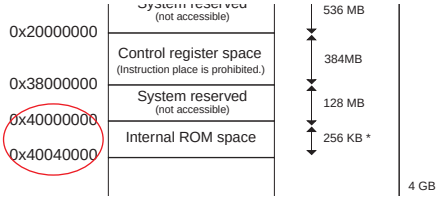
0x0000A314	TCMP0B	TCPB 0F	TCPB 0E	TCPB 0D	TCPB 0C	TCPB 0B	TCPB 0A	TCPB 09	TCPB 08	TCPB 07	TCPB 06	TCPB 05	TCPB 04	TCPB 03	TCPB 02	TCPB 01	TCPB 00	X-12
0x0000A318	TCMP0C	TCPC 0F	TCPC 0E	TCPC 0D	TCPC 0C	TCPC 0B	TCPC 0A	TCPC 09	TCPC 08	TCPC 07	TCPC 06	TCPC 05	TCPC 04	TCPC 03	TCPC 02	TCPC 01	TCPC 00	X-12
0x0000A31C	DTMSET 0	-	-	-	-	-	-	-	-	DTST 07	DTST 06	DTST 05	DTST 04	DTST 03	DTST 02	DTST 01	DTST 00	X-14
0x0000A320	PWMBC0	PWM0 BC15	PWM0 BC14	PWM0 BC13	PWM0 BC12	PWM0 BC11	PWM0 BC10	PWM0 BC09	PWM0 BC08	PWM0 BC07	PWM0 BC06	PWM0 BC05	PWM0 BC04	PWM0 BC03	PWM0 BC02	PWM0 BC01	PWM0 BC00	X-16
0x0000A324	BCSTR0									-	-	-	-	-	-	-	PWM0 STR	X-17
0x0000A328	PWMDCN T0	-	-	-	-	-	-	-	SDIR0	STIMO 7	STIMO 6	STIMO 5	STIMO 4	STIMO 3	STIMO 2	STIMO 1	STIMO 0	X-15
0x0000A330	PWMMD1	-	SYNEN 1	SFTEN 1	CLKSE L1	TMSTA EN1	TMSTB EN1	SDSEL A1	SDSEL B1	PCRAE N1	PCRBE N1	INTAEN 1	INTBE N1	DTEN1	ORMD 1	TCEN1	WAVE MD1	X-6
0x0000A334	OUTMD1	-	-	-	-	-	-	-	-	-	-	PXDTN W1	PXDT W1	PXDTN V1	PXDTV 1	PXDTN U1	PXDTU 1	X-8
0x0000A338	PWMSEL 1	-	-	-	-	PSELN 12	PSEL12	PSELN 11	PSEL11	PSELN 10	PSEL10	OTLVN 12	OTLV12	OTLVN 11	OTLV11	OTLVN 10	OTLV10	X-10
0x0000A33C	PWMSET 1	PWMS ET1F	PWMS ET1E	PWMS ET1D	PWMS ET1C	PWMS ET1B	PWMS ET1A	PWMS ET19	PWMS ET18	PWMS ET17	PWMS ET16	PWMS ET15	PWMS ET14	PWMS ET13	PWMS ET12	PWMS ET11	PWMS ET10	X-11
0x0000A340	TCMP1A	TCPA1 F	TCPA1 E	TCPA1 D	TCPA1 C	TCPA1 B	TCPA1 A	TCPA1 9	TCPA1 8	TCPA1 7	TCPA1 6	TCPA1 5	TCPA1 4	TCPA1 3	TCPA1 2	TCPA1 1	TCPA1 0	X-13
0x0000A344	TCMP1B	TCPB1 F	TCPB1 E	TCPB1 D	TCPB1 C	TCPB1 B	TCPB1 A	TCPB1 9	TCPB1 8	TCPB1 7	TCPB1 6	TCPB1 5	TCPB1 4	TCPB1 3	TCPB1 2	TCPB1 1	TCPB1 0	X-13
0x0000A348	TCMP1C	TCPC1 F	TCPC1 E	TCPC1 D	TCPC1 C	TCPC1 B	TCPC1 A	TCPC1 9	TCPC1 8	TCPC1 7	TCPC1 6	TCPC1 5	TCPC1 4	TCPC1 3	TCPC1 2	TCPC1 1	TCPC1 0	X-13
0x0000A34C	DTMSET 1	-	-	-	-	-	-	-	-	DTST1 7	DTST1 6	DTST1 5	DTST1 4	DTST1 3	DTST1 2	DTST1 1	DTST1 0	X-14
0x0000A350	PWMBC1	PWM1 BC15	PWM1 BC14	PWM1 BC13	PWM1 BC12	PWM1 BC11	PWM1 BC10	PWM1 BC09	PWM1 BC08	PWM1 BC07	PWM1 BC06	PWM1 BC05	PWM1 BC04	PWM1 BC03	PWM1 BC02	PWM1 BC01	PWM1 BC00	X-16
0x0000A354	BCSTR1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PWM1 STR	X-17
0x0000A358	PWMDCN T1	-	-	-	-	-	-	-	SDIR1	STIM17	STIM16	STIM15	STIM14	STIM13	STIM12	STIM11	STIM10	X-15
0x0000A360	PWMOFF	-	Reserved	Reserved	Reserved	IRQ SEL12	IRQ SEL11	IRQ SEL10	IRQ SEL02	IRQ SEL01	IRQ SEL00	Reserved	CLR HZ1	CLR HZ0	Reserved	USE HZ1	USE HZ0	X-15
0x0000A400	AN0CTR0	-	-	-	EXTRG 0	-	AN0CH 2	AN0CH 1	AN0CH 0	AN0EN	AN0OF F	AN0TR G	AN0CK 2	AN0CK 1	AN0CK 0	AN0MD 1	AN0MD 0	XIV-6
0x0000A404	AN0CTR1	-	Reserved	Reserved	Reserved	Reserved	AN0CH 0B2	AN0CH 0B1	AN0CH 0B0	AN0EN B	AN0TR GB	AN0SH C1	AN0SH C0	-	AN0NC H2	AN0NC H1	AN0NC H0	XIV-7
0x0000A408	ADST0									-	AD0BS T2	AD0BS T1	AD0BS T0	-	AD0AS T2	AD0AS T1	AD0AS T0	XIV-12
0x0000A40C	AN0CTR EGA									AN0AC HT3I	AN0AC HT2I	AN0AC HT1I	AN0AC HT0I	AN0AC HT3	AN0AC HT2	AN0AC HT1	AN0AC HT0	XIV-14
0x0000A40D	AN0CTR EGB									AN0BC HT3I	AN0BC HT2I	AN0BC HT1I	AN0BC HT0I	AN0BC HT3	AN0BC HT2	AN0BC HT1	AN0BC HT0	XIV-14
0x0000A410	AN0BUF0 0	-	-	-	-	-	-	AN0BU F09	AN0BU F08	AN0BU F07	AN0BU F06	AN0BU F05	AN0BU F04	AN0BU F03	AN0BU F02	AN0BU F01	AN0BU F00	XIV-17
0x0000A414	AN0BUF0 1	-	-	-	-	-	-	AN0BU F19	AN0BU F18	AN0BU F17	AN0BU F16	AN0BU F15	AN0BU F14	AN0BU F13	AN0BU F12	AN0BU F11	AN0BU F10	XIV-17
0x0000A418	AN0BUF0 2	-	-	-	-	-	-	AN0BU F29	AN0BU F28	AN0BU F27	AN0BU F26	AN0BU F25	AN0BU F24	AN0BU F23	AN0BU F22	AN0BU F21	AN0BU F20	XIV-17
0x0000A41C	AN0BUF0 3	-	-	-	-	-	-	AN0BU F39	AN0BU F38	AN0BU F37	AN0BU F36	AN0BU F35	AN0BU F34	AN0BU F33	AN0BU F32	AN0BU F31	AN0BU F30	XIV-18
0x0000A420	AN0BUF0 4	-	-	-	-	-	-	AN0BU F49	AN0BU F48	AN0BU F47	AN0BU F46	AN0BU F45	AN0BU F44	AN0BU F43	AN0BU F42	AN0BU F41	AN0BU F40	XIV-18
0x0000A424	AN0BUF0 5	-	-	-	-	-	-	AN0BU F59	AN0BU F58	AN0BU F57	AN0BU F56	AN0BU F55	AN0BU F54	AN0BU F53	AN0BU F52	AN0BU F51	AN0BU F50	XIV-18
0x0000A428	Reserved																	-
0x0000A42C	Reserved																	-
0x0000A430	AN0BUF0 B	-	-	-	-	-	-	AN0BU F0B9	AN0BU F0B8	AN0BU F0B7	AN0BU F0B6	AN0BU F0B5	AN0BU F0B4	AN0BU F0B3	AN0BU F0B2	AN0BU F0B1	AN0BU F0B0	XIV-19
0x0000A440	AN1CTR0	-	-	-	EXTRG 1	-	AN1CH 2	AN1CH 1	AN1CH 0	AN1EN	AN1OF F	AN1TR G	AN1CK 2	AN1CK 1	AN1CK 0	AN1MD 1	AN1MD 0	XIV-7
0x0000A444	AN1CTR1	-	Reserved	Reserved	Reserved	Reserved	AN1CH 0B2	AN1CH 0B1	AN1CH 0B0	AN1EN B	AN1TR GB	AN1SH C1	AN1SH C0	-	AN1NC H2	AN1NC H1	AN1NC H0	XIV-10
0x0000A448	ADST1									-	AD1BS T2	AD1BS T1	AD1BS T0	-	AD1AS T2	AD1AS T1	AD1AS T0	XIV-13
0x0000A44C	AN1CTR EGA									AN1AC HT3I	AN1AC HT2I	AN1AC HT1I	AN1AC HT0I	AN1AC HT3	AN1AC HT2	AN1AC HT1	AN1AC HT0	XIV-15
0x0000A44D	AN1CTR EGB									AN1BC HT3I	AN1BC HT2I	AN1BC HT1I	AN1BC HT0I	AN1BC HT3	AN1BC HT2	AN1BC HT1	AN1BC HT0	XIV-15
0x0000A450	AN1BUF0 2	-	-	-	-	-	-	AN1BU F29	AN1BU F28	AN1BU F27	AN1BU F26	AN1BU F25	AN1BU F24	AN1BU F23	AN1BU F22	AN1BU F21	AN1BU F20	XIV-20
0x0000A454	AN1BUF0 3	-	-	-	-	-	-	AN1BU F39	AN1BU F38	AN1BU F37	AN1BU F36	AN1BU F35	AN1BU F34	AN1BU F33	AN1BU F32	AN1BU F31	AN1BU F30	XIV-20

Address	Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x0000A458	AN1BUF04	-	-	-	-	-	-	AN1BUF49	AN1BUF48	AN1BUF47	AN1BUF46	AN1BUF45	AN1BUF44	AN1BUF43	AN1BUF42	AN1BUF41	AN1BUF40	XIV-20
0x0000A45C	AN1BUF05	-	-	-	-	-	-	AN1BUF59	AN1BUF58	AN1BUF57	AN1BUF56	AN1BUF55	AN1BUF54	AN1BUF53	AN1BUF52	AN1BUF51	AN1BUF50	XIV-21
0x0000A460	AN1BUF06	-	-	-	-	-	-	AN1BUF69	AN1BUF68	AN1BUF67	AN1BUF66	AN1BUF65	AN1BUF64	AN1BUF63	AN1BUF62	AN1BUF61	AN1BUF60	XIV-21
0x0000A464	AN1BUF07	-	-	-	-	-	-	AN1BUF79	AN1BUF78	AN1BUF77	AN1BUF76	AN1BUF75	AN1BUF74	AN1BUF73	AN1BUF72	AN1BUF71	AN1BUF70	XIV-21
0x0000A468	AN1BUF08	-	-	-	-	-	-	AN1BUF89	AN1BUF88	AN1BUF87	AN1BUF86	AN1BUF85	AN1BUF84	AN1BUF83	AN1BUF82	AN1BUF81	AN1BUF80	XIV-22
0x0000A46C	AN1BUF09	-	-	-	-	-	-	AN1BUF99	AN1BUF98	AN1BUF97	AN1BUF96	AN1BUF95	AN1BUF94	AN1BUF93	AN1BUF92	AN1BUF91	AN1BUF90	XIV-22
0x0000A470	AN1BUF0B	-	-	-	-	-	-	AN1BUF0B9	AN1BUF0B8	AN1BUF0B7	AN1BUF0B6	AN1BUF0B5	AN1BUF0B4	AN1BUF0B3	AN1BUF0B2	AN1BUF0B1	AN1BUF0B0	XIV-22
0x0000A480	AN2CTR0	-	-	-	EXTRG2	AN2CH3	AN2CH2	AN2CH1	AN2CH0	AN2EN	AN2OFF	AN2TRG	AN2CK2	AN2CK1	AN2CK0	AN2MD1	AN2MD0	XIV-8
0x0000A484	AN2CTR1	-	-	-	-	-	-	-	-	-	-	AN2SHC1	AN2SHC0	AN2NCH3	AN2NCH2	AN2NCH1	AN2NCH0	XIV-11
0x0000A488	ADST2									-	-	-	-	-	AD2AST2	AD2AST1	AD2AST0	XIV-13
0x0000A48C	AN2CTREGA									AN2ACHT3I	AN2ACHT2I	AN2ACHT1I	AN2ACHT0I	AN2ACHT3	AN2ACHT2	AN2ACHT1	AN2ACHT0	XIV-16
0x0000A490	AN2BUF06	-	-	-	-	-	-	AN2BUF69	AN2BUF68	AN2BUF67	AN2BUF66	AN2BUF65	AN2BUF64	AN2BUF63	AN2BUF62	AN2BUF61	AN2BUF60	XIV-23
0x0000A494	AN2BUF07	-	-	-	-	-	-	AN2BUF79	AN2BUF78	AN2BUF77	AN2BUF76	AN2BUF75	AN2BUF74	AN2BUF73	AN2BUF72	AN2BUF71	AN2BUF70	XIV-23
0x0000A498	AN2BUF08	-	-	-	-	-	-	AN2BUF89	AN2BUF88	AN2BUF87	AN2BUF86	AN2BUF85	AN2BUF84	AN2BUF83	AN2BUF82	AN2BUF81	AN2BUF80	XIV-23
0x0000A49C	AN2BUF09	-	-	-	-	-	-	AN2BUF99	AN2BUF98	AN2BUF97	AN2BUF96	AN2BUF95	AN2BUF94	AN2BUF93	AN2BUF92	AN2BUF91	AN2BUF90	XIV-24
0x0000A4A0	AN2BUF10	-	-	-	-	-	-	AN2BUF109	AN2BUF108	AN2BUF107	AN2BUF106	AN2BUF105	AN2BUF104	AN2BUF103	AN2BUF102	AN2BUF101	AN2BUF100	XIV-24
0x0000A4A4	AN2BUF11	-	-	-	-	-	-	AN2BUF119	AN2BUF118	AN2BUF117	AN2BUF116	AN2BUF115	AN2BUF114	AN2BUF113	AN2BUF112	AN2BUF111	AN2BUF110	XIV-24
0x0000A4A8	AN2BUF12	-	-	-	-	-	-	AN2BUF129	AN2BUF128	AN2BUF127	AN2BUF126	AN2BUF125	AN2BUF124	AN2BUF123	AN2BUF122	AN2BUF121	AN2BUF120	XIV-25
0x0000A4AC	AN2BUF13	-	-	-	-	-	-	AN2BUF139	AN2BUF138	AN2BUF137	AN2BUF136	AN2BUF135	AN2BUF134	AN2BUF133	AN2BUF132	AN2BUF131	AN2BUF130	XIV-25
0x0000A4B0	AN2BUF14	-	-	-	-	-	-	AN2BUF149	AN2BUF148	AN2BUF147	AN2BUF146	AN2BUF145	AN2BUF144	AN2BUF143	AN2BUF142	AN2BUF141	AN2BUF140	XIV-25
0x0000A4B4	AN2BUF15	-	-	-	-	-	-	AN2BUF159	AN2BUF158	AN2BUF157	AN2BUF156	AN2BUF155	AN2BUF154	AN2BUF153	AN2BUF152	AN2BUF151	AN2BUF150	XIV-26
0x0000A4B8	Reserved																	-
0x0000A4BC	Reserved																	-
0x0000A4C0	Reserved																	-
0x0000A4C4	Reserved																	-
0x0000A4C8	Reserved																	-
0x0000A4CC	Reserved																	-
0x0000AFF2	PCNT	-	-	-	-	-	-	-	-	-	-	PLLSEL	-	PLLON	-	CKSEL1	CKSEL0	III-3
0x7FF00000	RCRCTR									-	-	-	-	RCMEN	RCCEN	-	RCRWE	VI-4
0x7FF00100	RCR0AR	RC0CEN	-	-	-	-	-	-	-	-	-	-	-	RC0AD19	RC0AD18	RC0AD17	RC0AD16	VI-5
		RC0AD15	RC0AD14	RC0AD13	RC0AD12	RC0AD11	RC0AD10	RC0AD9	RC0AD8	RC0AD7	RC0AD6	RC0AD5	RC0AD4	RC0AD3	RC0AD2	RC0AD1	RC0AD0	
0x7FF00108	RCR0DR	RC0DT63	RC0DT62	RC0DT61	RC0DT60	RC0DT59	RC0DT58	RC0DT57	RC0DT56	RC0DT55	RC0DT54	RC0DT53	RC0DT52	RC0DT51	RC0DT50	RC0DT49	RC0DT48	VI-7
		RC0DT47	RC0DT46	RC0DT45	RC0DT44	RC0DT43	RC0DT42	RC0DT41	RC0DT40	RC0DT39	RC0DT38	RC0DT37	RC0DT36	RC0DT35	RC0DT34	RC0DT33	RC0DT32	
		RC0DT31	RC0DT30	RC0DT29	RC0DT28	RC0DT27	RC0DT26	RC0DT25	RC0DT24	RC0DT23	RC0DT22	RC0DT21	RC0DT20	RC0DT19	RC0DT18	RC0DT17	RC0DT16	
		RC0DT15	RC0DT14	RC0DT13	RC0DT12	RC0DT11	RC0DT10	RC0DT9	RC0DT8	RC0DT7	RC0DT6	RC0DT5	RC0DT4	RC0DT3	RC0DT2	RC0DT1	RC0DT0	
0x7FF00110	RCR1AR	RC1CEN	-	-	-	-	-	-	-	-	-	-	-	RC1AD19	RC1AD18	RC1AD17	RC1AD16	VI-5
		RC1AD15	RC1AD14	RC1AD13	RC1AD12	RC1AD11	RC1AD10	RC1AD9	RC1AD8	RC1AD7	RC1AD6	RC1AD5	RC1AD4	RC1AD3	RC1AD2	RC1AD1	RC1AD0	

Address	Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x7FF00118	RCR1DR	RC1 DT63	RC1 DT62	RC1 DT61	RC1 DT60	RC1 DT59	RC1 DT58	RC1 DT57	RC1 DT56	RC1 DT55	RC1 DT54	RC1 DT53	RC1 DT52	RC1 DT51	RC1 DT50	RC1 DT49	RC1 DT48	VI-8
		RC1 DT47	RC1 DT46	RC1 DT45	RC1 DT44	RC1 DT43	RC1 DT42	RC1 DT41	RC1 DT40	RC1 DT39	RC1 DT38	RC1 DT37	RC1 DT36	RC1 DT35	RC1 DT34	RC1 DT33	RC1 DT32	
		RC1 DT31	RC1 DT30	RC1 DT29	RC1 DT28	RC1 DT27	RC1 DT26	RC1 DT25	RC1 DT24	RC1 DT23	RC1 DT22	RC1 DT21	RC1 DT20	RC1 DT19	RC1 DT18	RC1 DT17	RC1 DT16	
		RC1 DT15	RC1 DT14	RC1 DT13	RC1 DT12	RC1 DT11	RC1 DT10	RC1 DT9	RC1 DT8	RC1 DT7	RC1 DT6	RC1 DT5	RC1 DT4	RC1 DT3	RC1 DT2	RC1 DT1	RC1 DT0	
0x7FF00120	RCR2AR	RC2 CEN	-	-	-	-	-	-	-	-	-	-	-	RC2 AD19	RC2 AD18	RC2 AD17	RC2 AD16	VI-6
		RC2 AD15	RC2 AD14	RC2 AD13	RC2 AD12	RC2 AD11	RC2 AD10	RC2 AD9	RC2 AD8	RC2 AD7	RC2 AD6	RC2 AD5	RC2 AD4	RC2 AD3	RC2 AD2	RC2 AD1	RC2 AD0	
0x7FF00128	RCR2DR	RC2 DT63	RC2 DT62	RC2 DT61	RC2 DT60	RC2 DT59	RC2 DT58	RC2 DT57	RC2 DT56	RC2 DT55	RC2 DT54	RC2 DT53	RC2 DT52	RC2 DT51	RC2 DT50	RC2 DT49	RC2 DT48	VI-9
		RC2 DT47	RC2 DT46	RC2 DT45	RC2 DT44	RC2 DT43	RC2 DT42	RC2 DT41	RC2 DT40	RC2 DT39	RC2 DT38	RC2 DT37	RC2 DT36	RC2 DT35	RC2 DT34	RC2 DT33	RC2 DT32	
		RC2 DT31	RC2 DT30	RC2 DT29	RC2 DT28	RC2 DT27	RC2 DT26	RC2 DT25	RC2 DT24	RC2 DT23	RC2 DT22	RC2 DT21	RC2 DT20	RC2 DT19	RC2 DT18	RC2 DT17	RC2 DT16	
		RC2 DT15	RC2 DT14	RC2 DT13	RC2 DT12	RC2 DT11	RC2 DT10	RC2 DT9	RC2 DT8	RC2 DT7	RC2 DT6	RC2 DT5	RC2 DT4	RC2 DT3	RC2 DT2	RC2 DT1	RC2 DT0	
0x7FF00130	RCR3AR	RC3 CEN	-	-	-	-	-	-	-	-	-	-	-	RC3 AD19	RC3 AD18	RC3 AD17	RC3 AD16	VI-6
		RC3 AD15	RC3 AD14	RC3 AD13	RC3 AD12	RC3 AD11	RC3 AD10	RC3 AD9	RC3 AD8	RC3 AD7	RC3 AD6	RC3 AD5	RC3 AD4	RC3 AD3	RC3 AD2	RC3 AD1	RC3 AD0	
0x7FF00138	RCR3DR	RC3 DT63	RC3 DT62	RC3 DT61	RC3 DT60	RC3 DT59	RC3 DT58	RC3 DT57	RC3 DT56	RC3 DT55	RC3 DT54	RC3 DT53	RC3 DT52	RC3 DT51	RC3 DT50	RC3 DT49	RC3 DT48	VI-10
		RC3 DT47	RC3 DT46	RC3 DT45	RC3 DT44	RC3 DT43	RC3 DT42	RC3 DT41	RC3 DT40	RC3 DT39	RC3 DT38	RC3 DT37	RC3 DT36	RC3 DT35	RC3 DT34	RC3 DT33	RC3 DT32	
		RC3 DT31	RC3 DT30	RC3 DT29	RC3 DT28	RC3 DT27	RC3 DT26	RC3 DT25	RC3 DT24	RC3 DT23	RC3 DT22	RC3 DT21	RC3 DT20	RC3 DT19	RC3 DT18	RC3 DT17	RC3 DT16	
		RC3 DT15	RC3 DT14	RC3 DT13	RC3 DT12	RC3 DT11	RC3 DT10	RC3 DT9	RC3 DT8	RC3 DT7	RC3 DT6	RC3 DT5	RC3 DT4	RC3 DT3	RC3 DT2	RC3 DT1	RC3 DT0	

Record of Changes

MN103SA7D/A7G LSI User's Manual Record of Changes from the 1st Edition 1st Printing dated in April, 2006 to the 1st Edition 2nd Printing dated in February, 2008.

Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
I-6	Timer17	Change	- Interval timer, Timer pulse output, Event count, Baud rate Timer, Cascade connection function (connected to Timer 16)	- Interval timer, Timer pulse output, Event count, Cascade connection function (connected to Timer 16)
I-7	A/D converter	Change	- Minimum conversion time 1.3 msec - 4 channels x 2 converters - 8 channels x 1 converters	- Minimum conversion time 1.0 msec - 16 channels x 3 converters
	Comple-mentary 3-phase PWM output	Change	- Min. resolution: 33.3 nsec	- Min. resolution: 16.7 nsec
I-12	P10 to PA0	Change	8-bit COMS I/O ports. ...	8-bit CMOS I/O ports. ...
I-17	A6 A7	Change	Peak output current ±10 Typ. range output current ±5	Peak output current ±20 Typ. range output current ±10
I-20	C1	Change	DC Characteristics (mask ROM version) Parameter ... Limits (Typ. Max.) Unit C1 Operating supply current (VDD pin) t.b.f t.b.f mA	DC Characteristics (Upper:M-ROM, Lower:Flash) Parameter ... Limits (Typ. Max.) Unit C1 Operating supply current (VDD pin) 60 80 mA 80 120
I-22	D4 D5	Change	Min. Typ. Max. Zero transition voltage t.b.f - t.b.f Full-scale transition voltage t.b.f - t.b.f	Min. Typ. Max. Zero transition voltage -25 - 25 Full-scale transition voltage 4975 - 5025
I-23	Figure 1.5.3	Change		
II-18	Figure 2.6.1	Change		 *Vary by model. Refer to Table2.6.1 Internal ROM/RAM by model.
	Table 2.6.1	Add	-	Table 2.6.1 Internal ROM/RAM by model

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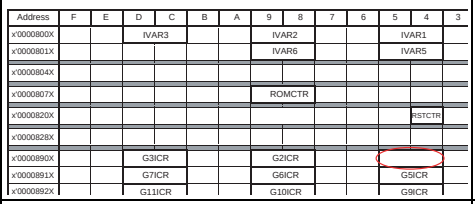
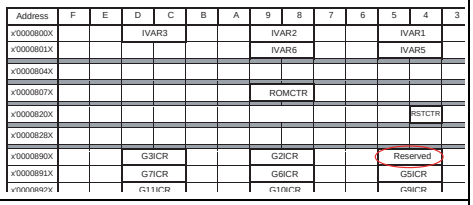
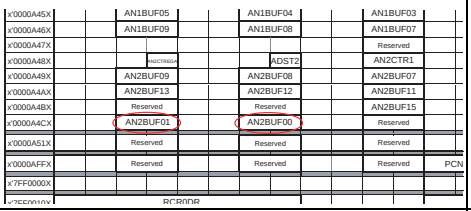
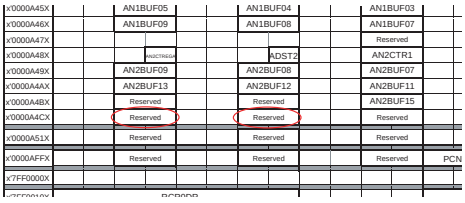
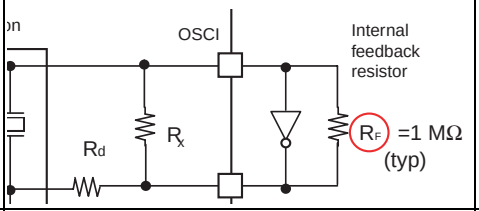
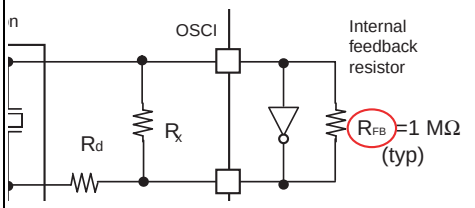
II-19	Table 2.6.2	Change		
II-20	Table 2.6.2	Change		
III-3	■ PLL control register	Change	bp ... Set condition 1-0 ... 11: Setting prohibited	bp ... Set condition 1-0 ... 11: Setting prohibited When changing the PLLON flag... more than 200ms.
III-7	Figure 3.3.1	Change		
	Table 3.3.4	Change	Frequency ... Recommended circuit constant It is described after matching evaluation.	Frequency ... Recommended circuit constant [Hz] ... Load Capacity ... Dumping resistor 5.000M ... (47) ... 0 I 15.000M ... (15) ... 0
IV-5	■Internal ROM Access Control Resister	Change	bp ... Set condition 9-8 ... 01: 2 cycle(2xMCLK) access 10: 3 cycle(2xMCLK) access	bp ... Set condition 9-8 ... 01: 2 cycle(2xMCLK) access If CPU clock ..., it is prohibited. 10: 3 cycle(2xMCLK) access When the CPU clock ..., is switched from “0“ to ”1”.
	Note	Add	-	When the CPU clock ... is not guranteed.
V-8	Accepted group	Change	Resister Address R/W ... IAGR 0x00008A00 R/W ...	Resister Address R/W ... IAGR 0x00008A00 R ...
V-21	bp 10,9,6,5	Change	G11IE2 Timer12 compare/capture B interrupt enable flag G11IE1 Timer12 compare/capture A interrupt enable flag G11IR2 Timer12 compare/capture B interrupt request flag G11IR1 Timer12 compare/capture A interrupt request flag	G11IE2 Timer12 compare B interrupt enable flag G11IE1 Timer12 compare A interrupt enable flag G11IR2 Timer12 compare B interrupt request flag G11IR1 Timer12 compare A interrupt request flag

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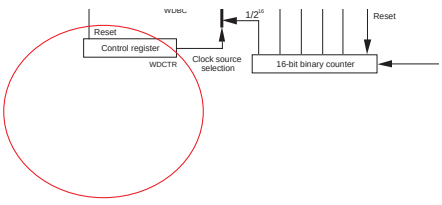
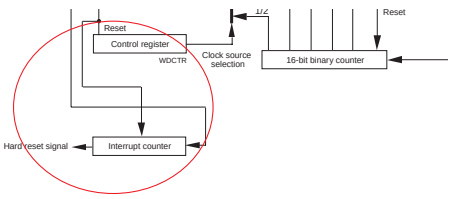
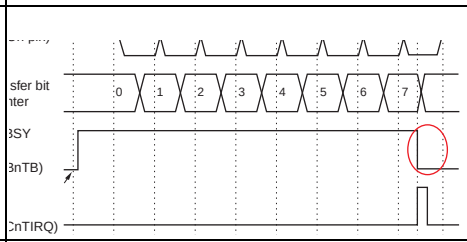
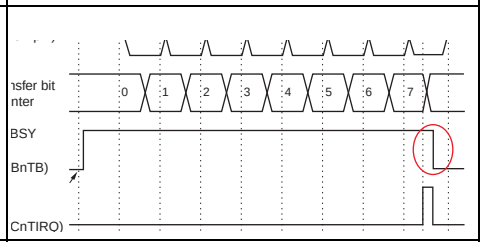
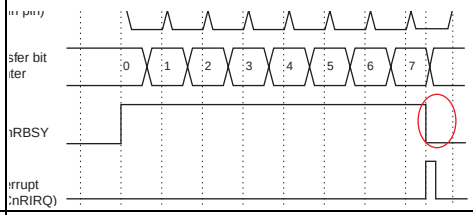
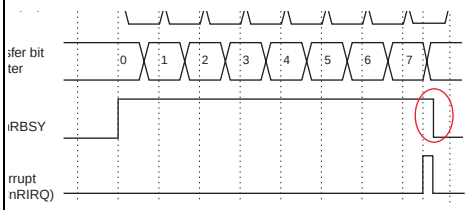
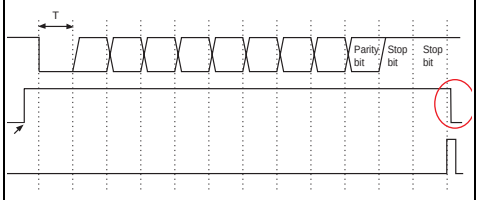
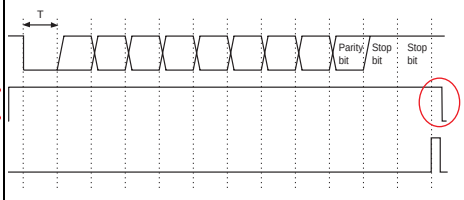
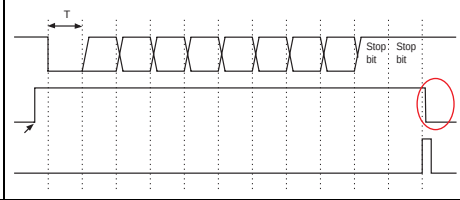
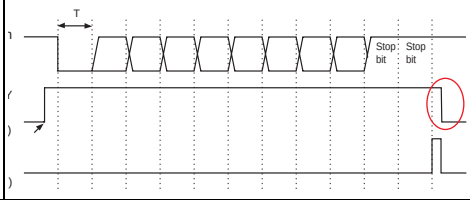
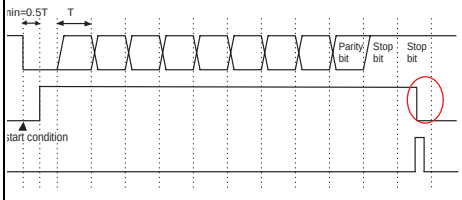
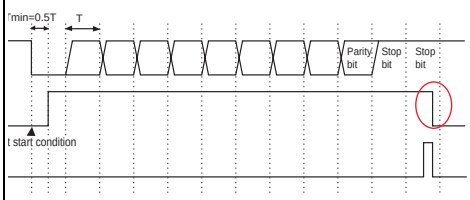
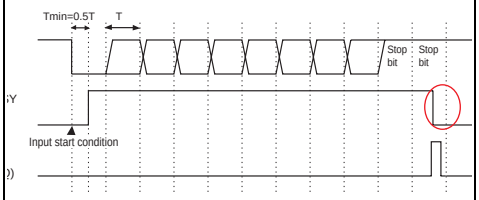
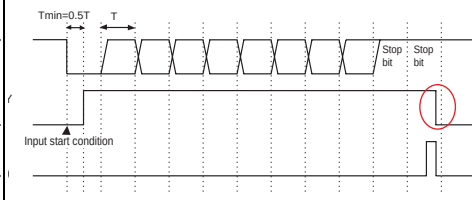
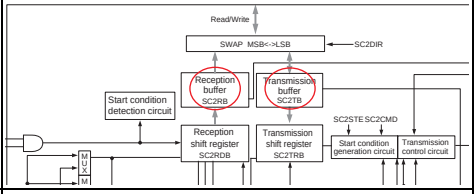
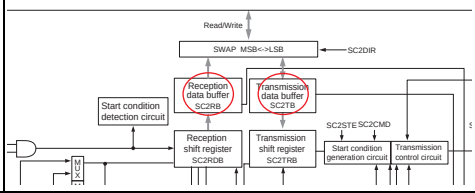
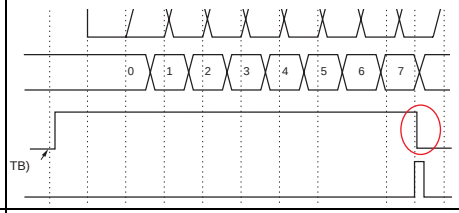
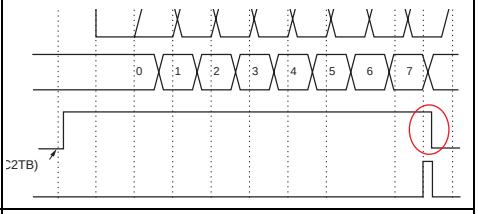
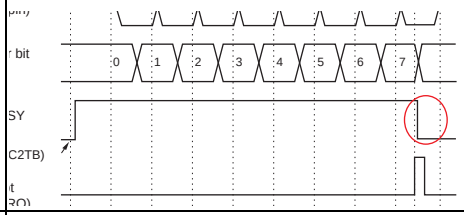
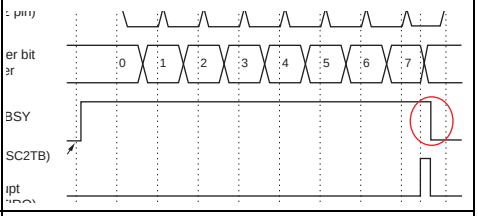
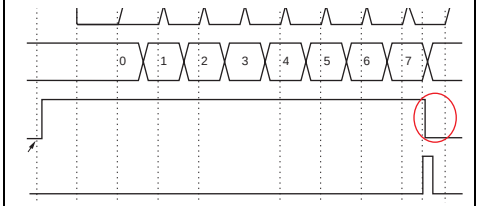
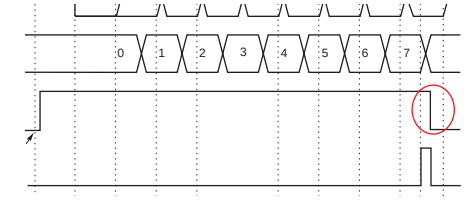
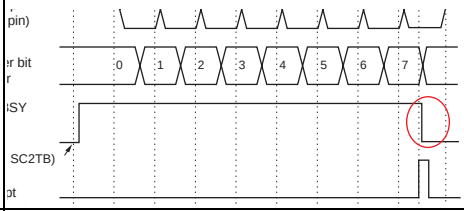
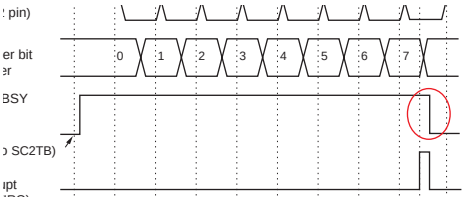
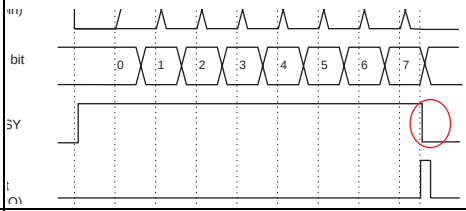
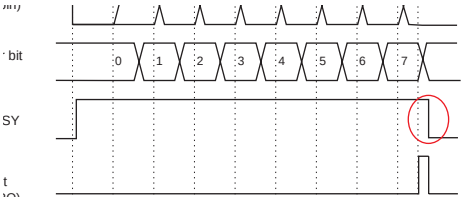
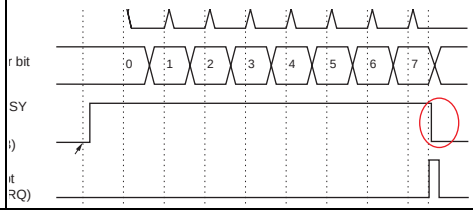
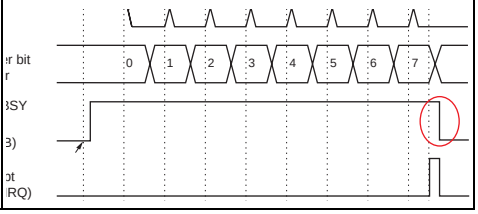
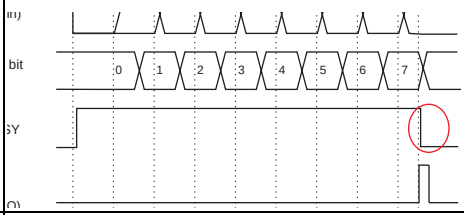
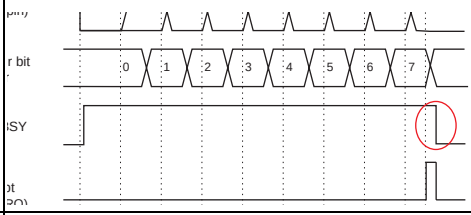
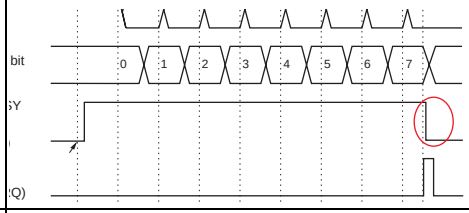
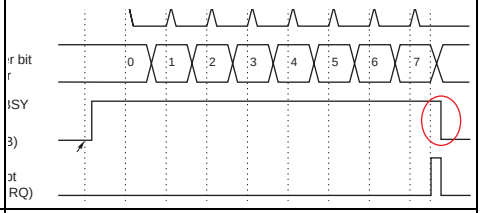
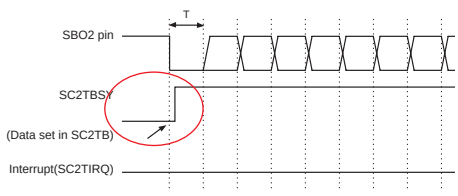
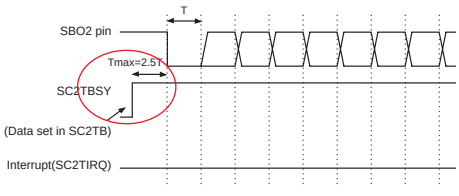
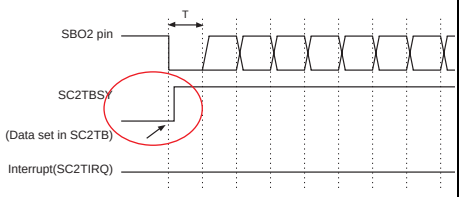
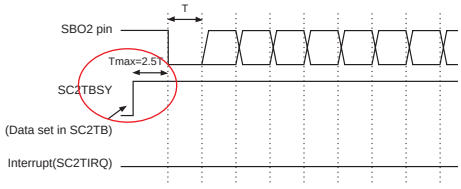
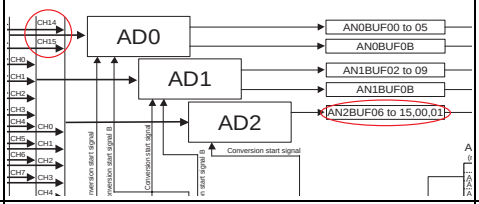
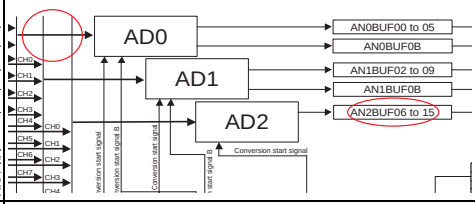
V-22	bp 10,9,6,5, 2,1	Change	G12IE2 Timer13 compare/capture B interrupt enable flag G12IE1 Timer13 compare/capture A interrupt enable flag G12IR2 Timer13 compare/capture B interrupt request flag G12IR1 Timer13 compare/capture A interrupt request flag G12ID2 Timer13 compare/capture B interrupt detection flag G12ID1 Timer13 compare/capture A interrupt detection flag	G12IE2 Timer13 compare B interrupt enable flag G12IE1 Timer13 compare A interrupt enable flag G12IR2 Timer13 compare B interrupt request flag G12IR1 Timer13 compare A interrupt request flag G12ID2 Timer13 compare B interrupt detection flag G12ID1 Timer13 compare A interrupt detection flag
V-45	Note	Add	-	If operationg the edge detection register... , and use as a port for monitor.
VIII -43	Note	Add	-	In reading out value of... Stop the timer in order to read out the corrrect value.
IX-2	Table 9.1.1	Change	Timer 12 Timer 13 Up/down count - -	Timer 12 Timer 13 Up/down count O O
IX-62	Setup Proce-dure (9)	Change	bp1-0: TMB1-0=11	bp1-0: TMB1-0=00
IX-65	Setup Proce-dure (8)	Change	bp5: TMAEG=1	bp5: TMAEG=0
	Descripti on (8)	Change	(8) Set the TMAEG flag of the TM8MDA regis-ter to "1" to select the rising edge.	(8) Set the TMAEG flag of the TM8MDA regis-ter to "0" to select the rising edge.
X-5	bp12	Change	CLKSEL0 0:IOCLK 1:Setting disabled	CLKSEL0 0:IOCLK 1:MCLK
X-6	bp12	Change	CLKSEL1 0:IOCLK 1:Setting disabled	CLKSEL1 0:IOCLK 1:MCLK
X-27	■Setting PWM Output Timing	Change	... The relationship between ...	... Set the SETENn flag of the PWMMDn regis-ter to "1" to valid shift function of PWM output timing. The relationship between ...
XI-2	Line 2	Change	This LSI has an internal 24-bit binary counter... used as an oscillation stabilization wait timer.	This LSI has an internal 24-bit binary counter... used as an oscillation stabilization wait timer.
	Table 11.1.1	Add	-	Forced-reset function
	Figure 11.1.1	Change		

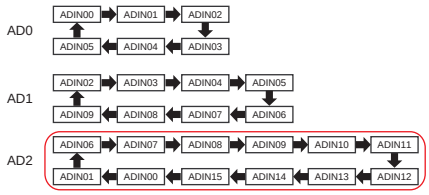
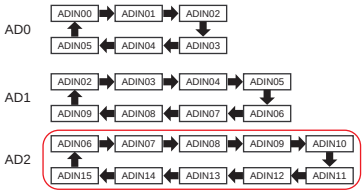
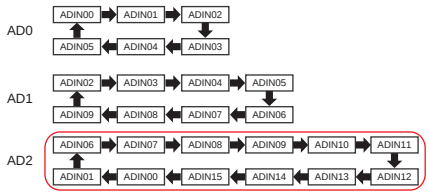
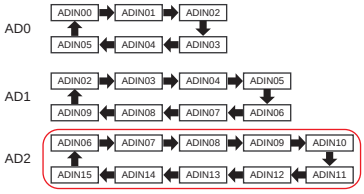
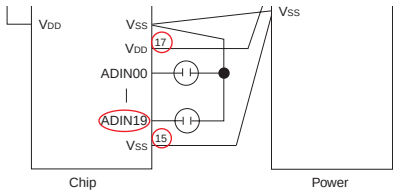
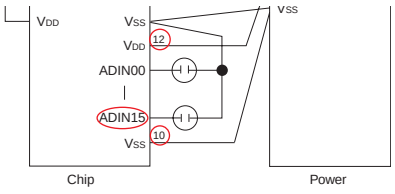
Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XII-14	Figure 12.3.3	Change		
	Figure 12.3.4	Change		
XII-21	Figure 12.3.7	Change		
	Figure 12.3.8	Change		
XII-22	Figure 12.3.9	Change		
	Figure 12.3.10	Change		
XIII-2	Table 13.1.1	Change	Interrupt SC2TIRQ 1-channel communication - SBO2	Interrupt SC2TIRQ (at completion of transmission) 1-channel communication - O SBO2

Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XIII-3	Figure 13.1.1	Change		
XIII-4	Note	Add	-	Whe changing the setting value ... registers are set to “0“.)
XIII-7	bp7	Change	SC2IOM Serial data input selection	SC2IOM Serial data input pin selection
	bp5	Change	SC2SBIS 0: ”1” input 1: Serial input	SC2SBIS 0: ”1” input fix 1: Serial data input
	Note	Add	-	Whe changing the setting value ... registers are set to “0“.)
XIII-11	■Activation Factors for Communication	Change	However, the external clock should be fed after more than 2.5 transfer clock ...	However, the external clock should be fed after more than 3.5 transfer clock ...
	■Transmission Data Buffer	Change	... into the internal shift register. ... into the internal shift register. 2.5 transfer clock cycles ...	... into the transmission shift register. ... into the internal shift register. 3.5 transfer clock cycles ...
XIII-12	■Reception Data Buffer	Change	... the received data by the internal shift register. After the communication complete interrupt SC2TIRQ is generated, data stored in the internal shift register ...	... the received data by the reception shift register. After the communication complete interrupt SC2TIRQ is generated, data stored in the reception shift register ...
	Note 4	Change	Wait more than 2.5 transfer clocks for ...	Wait more than 3.5 transfer clocks for ...
	■Setting Start Condition	Change	... before change the start condition edge.	... before change the start condition edge. Then, select "without start condition" when performing transmission and reception at the same time. It may not be operated properly.
XIII-15	Table 13.3.4	Change	At slave [1-bit data length of external clock x 1/2]+[Internal clock cycle x (1 to 2)]	At slave [1-bit data length of external clock x 1/2]+[Internal clock cycle x (1/2 to 3/2)]
XIII-16	Note	Add	-	In using synchronous serial interface, ... GI5IR0 is not generated.
	■Reception Buffer Empty Flag Operation	Change	... stored from the internal shift register into SC2RB. ...	... stored from the reception shift register into SC2RB. ...
	■Transmission Buffer Empty Flag Operation	Change	... is generated after data is load into the internal shift register), ...	... is generated after data is load into the transmission shift register), ...

Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XIII -17	■Continuous Transmission	Change	■Continuous Communication This serial is equipped with a continuous communication function. ... data is loaded to the internal shift register and ...	■Continuous Transmission This serial is equipped with a continuous transmission function. ... data is loaded to the transmission shift register and ...
XIII -18	Figure 13.3.5	Change		
	Figure 13.3.6	Change		
XIII -19	Figure 13.3.7	Change		
	Figure 13.3.8	Change		
XIII -20	Figure 13.3.9	Change		
	Figure 13.3.10	Change		

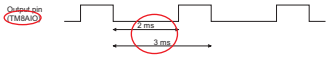
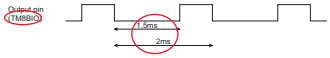
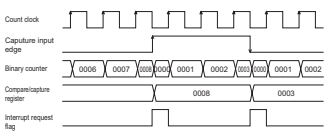
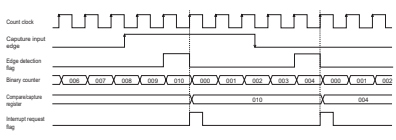
Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XIII -21	Figure 13.3.11	Change		
	Figure 13.3.12	Change		
XIII -22	■ Transmission and Reception	Change	In order to operate transmission and reception ... so many cause improper operation.	As data is received at the opposite edge ... so may cause improper communication.
XIII -25	■ Activation Factor for Communication	Change	At reception, reception is started by receiving a start condition. In reception, when the data length of "L" for start bit is equal to or longer than 0.5 bit, that is recognized as a start condition.	At reception, reception is started by receiving a start bit. In reception, when the data length of "L" for input data is equal to or longer than 0.5 bit, that is recognized as a start bit.
	■ Reception	Change	When a start condition is recognized, ...	When a start bit is recognized, ...
XIII -28	■ Reception Buffer Empty Flag Operation	Change	When the reception complete interrupt SC2RIRQ is generated, data is automatically stored from the internal shift register to SC2RB. ...	When the reception complete interrupt SC2RIRQ is generated, data is automatically stored from the reception shift register to SC2RB. ...
	■ Transmission Buffer Empty Flag Operation	Change	If data is set in SC2TB during communication (till the communication complete interrupt SC2TIRQ is generated after data is load into the internal shift register), ...	If data is set in SC2TB during communication (till the communication complete interrupt SC2TIRQ is generated after data is load into the transmission shift register), ...
	■ Reception BUSY Flag Operation	Change	The SC2RBSY flag of the SC2STR register is set to "1" when a start condition is recognized. ...	The SC2RBSY flag of the SC2STR register is set to "1" when a start bit is recognized. ...
XIII -29	Figure 13.3.18	Change		

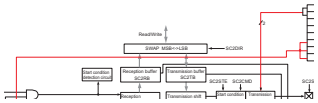
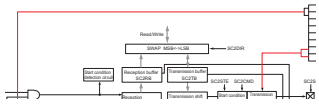
Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XIII -30	Figure 13.3.19	Change		
XIV -2	Table 14.1.1	Change	Numbers of analog input pins AD2 Max. 10 pins	Numbers of analog input pins AD2 Max. 12 pins
XIV -3	Figure 14.1.1	Change		
XIV -4	Table 14.2.1	Change	AD0 AN0BUF00 .. R/W to AN0BUF0B .. R/W AD1 AN1CTR0 .. R/W AN1BUF02 .. R/W to AN0BUF0B .. R/W AD2 AN2CTREG .. R/W AN2BUF06 .. R/W to AN2BUF01 .. R/W	AD0 AN0BUF00 .. R to AN0BUF0B .. R AD1 AN1CTR0 .. R AN1BUF02 .. R to AN0BUF0B .. R AD2 AN2CTREGA .. R/W AN2BUF06 .. R to AN2BUF15 .. R
		Deletion	AD2 AN2BUF00 .. AN2BUF01 ..	-
XIV -6	bp 4-2	Change	AN0CK2 101: 16 dividing of IOCLK AN0CK1 AN0CK0	AN0CK2 101: 16 dividing of IOCLK AN0CK1 110: setting prohibited AN0CK0 111: setting prohibited
XIV -7	bp 4-2	Change	AN1CK2 101: 16 dividing of IOCLK AN1CK1 AN1CK0	AN1CK2 101: 16 dividing of IOCLK AN1CK1 110: setting prohibited AN1CK0 111: setting prohibited
XIV -8	bp 10-8	Change	AN2CH3 1110: ADIN00 AN2CH2 1111: ADIN01 AN2CH1 AN2CH0	AN2CH3 1110: setting prohibited AN2CH2 1111: setting prohibited AN2CH1 AN2CH0
	bp 4-2	Change	AN2CK2 101: 16 dividing of IOCLK AN2CK1 AN2CK0	AN2CK2 101: 16 dividing of IOCLK AN2CK1 110: setting prohibited AN2CK0 111: setting prohibited
XIV -9	bp 10-8	Change	* The result of this channel conversion is stored in AN0BUF0B0: x0000A430.	* The result of this channel conversion is stored in AN0BUF0B: x0000A430.
XIV -10	bp 10-8	Change	* The result of this channel conversion is stored in AN1BUF0B0: x0000A470.	* The result of this channel conversion is stored in AN1BUF0B: x0000A470.
XIV -11	bp 3-0	Change	AN2NCH3 1110: ADIN00 AN2NCH2 1111: ADIN01 AN2NCH1 AN2NCH0	AN2NCH3 1110: setting prohibited AN2NCH2 1111: setting prohibited AN2NCH1 AN2NCH0

Page	Section	Definition	Previous Edition (Ver.1.1)	New Edition (Ver.1.2)
XIV -26	■ A/D2 Conver-sion Data Buffer 0	Deletion	■ A/D2 Conversion Data Buffer 0	-
	■ A/D2 Conver-sion Data Buffer 1	Deletion	■ A/D2 Conversion Data Buffer 1	-
XIV -28	Table 14.3.3	Change	Start Trigger ... ANnTRG (ANnCTR0)	Start Trigger ... ANnTRGB (ANnCTR1)
XIV -30	Note	Change		
XIV -32	Note	Change		
XIV -44	Note	Change		

MN103SA7D/A7G LSI User's Manual Record of Changes from the 1st Edition dated in March, 2005 to the 1st Edition 1st Printing dated in April, 2006.

Page	Section	Definition	Previous Edition (Ver.1)	New Edition (Ver.1.1)
1-8	Line 29	Change	External interrupt 8 pins	External interrupt 9 pins
8-18	Table Set condition	Change	TM0BR value is loaded into TM0BC. Timer output 0 is set to “L” level.	TM0BR value is loaded into TM0BC.
8-24	Table Set condition	Change	TM6BR value is loaded into TM6BC. Timer output 6 is set to “L” level.	TM6BR value is loaded into TM6BC.
8-26	Table Set condition	Change	TM14BR value is loaded into TM14BC. Timer output 14is set to “L” level.	TM14BR value is loaded into TM14BC.
8-27	Table Set condition	Change	TM15BR value is loaded into TM15BC. Timer output 15 is set to “L” level.	TM15BR value is loaded into TM15BC.
8-28	Table Set condition	Change	TM16BR value is loaded into TM16BC. Timer output 16 is set to “L” level.	TM16BR value is loaded into TM16BC.
8-37	Table Description (3)	Change	··· The setting value is 149 due to 200KHz. ···	··· The setting value is 149 (0x95) due to 200KHz. ···
9-20	Upper table	Change	15 TMXF 0 R/W 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 0 R/W	15 TMXF 0 R 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 1 R/W
9-21	Upper table	Change	15 TMXF 0 R/W 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 0 R/W	15 TMXF 0 R 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 1 R/W
9-22	Upper table	Change	15 TMXF 0 R/W 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 0 R/W	15 TMXF 0 R 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 1 R/W
9-23	Upper table	Change	15 TMXF 0 R/W 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 0 R/W	15 TMXF 0 R 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 1 R/W
9-24	Upper table	Change	15 TMXF 0 R/W 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 0 R/W	15 TMXF 0 R 14 - 0 R 13 TMTGE 0 R/W 12 TMONE 0 R/W 11 TMCLE 1 R/W

Page	Section	Definition	Previous Edition (Ver.1)	New Edition (Ver.1.1)
9-25	Upper table	Change	15 14 13 12 11 TMXF - TMTGE TMONE TMCLE 0 0 0 0 0 R/W R R/W R/W R/W	15 14 13 12 11 TMXF - TMTGE TMONE TMCLE 0 0 0 0 1 R R R/W R/W R/W
9-38	Table Setup Proce-dure (2)	Change	Set the compare/capture register TM8CA(0x0000A208)=0x09C3	Set the compare/capture register TM8CA(0x0000A208)=0x0EA5
	Descrip-tion(2)	Change	··· The setting is 2499 (0x09C3) due to 2500 counts.	··· The setting is 3749 (0x0EA5) due to 3750 counts.
9-41	Table Setup Proce-dure (3)	Change	Set the interrupt generation cycle TM8CA(0x0000A208)=0x4E1F	Set the interrupt generation cycle TM8CA(0x0000A208)=0x752F
	Descrip-tion(3)	Change	··· The setting is 19999 (0x4E1F) due to 20000 counts.	··· The setting is 29999 (0x752F) due to 30000 counts.
9-55	Table Setup Proce-dure (2)	Change	Set the interrupt generation cycle TM8CA(0x0000A208)=0x4E1F	Set the interrupt generation cycle TM8CA(0x0000A208)=0x752F
	Descrip-tion(2)	Change	··· The setting is 19999 (0x4E1F) due to 20000 counts.	··· The setting is 29999 (0x752F) due to 30000 counts.
9-61	Line 3 to 6	Change	The output pin (TM8AIO) using timer 8 outputs waveforms as shown below (repeating “L” output for 2 ms and “H” output for the next 1 ms). IOCLK is selected as clock source to match the binary counter and the compare/capture A register for every 2 ms and to match the binary counter and the compare/cap-ture B register for every 3 ms.	The output pin (TM8AIO) using timer 8 outputs waveforms as shown below (repeating “L” output for 1.5 ms and “H” output for the next 0.5 ms). IOCLK is selected as clock source to match the binary counter and the compare/capture B register for every 1.5 ms and to match the binary counter and the compare/cap-ture A register for every 2 ms.
	Figure 9.8.3	Change		
	Table Setup Proce-dure (2)	Change	Set the repeating cycle TM8CA(0x0000A208)=0x9C3F	Set the repeating cycle TM8CB(0x0000A20C)=0xAFC7
	Descrip-tion(2)	Change	··· The setting is 39999 (0x9C3F) due to 40000 counts.	··· The setting is 44999 (0xAFC7) due to 45000 counts.
9-64	Figure 9.9.1	Change		

Page	Section	Definition	Previous Edition (Ver.1)	New Edition (Ver.1.1)
9-67	Table Setup Proce-dure (2)	Change	Set the count cycle TM8CA(0x0000A208)=0x4E1F	Set the count cycle TM8CA(0x0000A208)=0x752F
	Descrip-tion(2)	Change	··· Due to 20000 counts, the setting value is 19999 (0x4E1F).	··· Due to 30000 counts, the setting value is 29999 (0x752F).
9-70	Table Setup Proce-dure (2)	Change	Set the repeating cycle TM8CA(0x0000A208)=0x4E1F	Set the repeating cycle TM8CA(0x0000A208)=0x752F
	Descrip-tion(2)	Change	··· The setting value is 19999 (0x4E1F) due to 20000 counts.	··· The setting value is 29999 (0x752F) due to 30000 counts.
13-3	Figure 13.1.1	Change		

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